5. Harmonic Content

5.1. Development Notes

The Power Factor Correction circuit, based upon the UCC28019AD integrated circuit exhibited a current oscillation at the peak of the mains at high load. This was visible on the input current.
It appeared that the internal over current protection of the control IC was being operated shortly after FET turn on.
A number of investigations were conducted:

5.1.1. Reducing Gate Drive resistor

It was suspected that the gate drive was too slow, to the point where turn-on discharges were being detected after the leading edge blanking period. The gate drive resistor was reduced to 10R, allowing the maximum peak current from the IC. The problem was apparently unchanged.

5.1.2. Altering the gate drive current path

The 0V connection to the PCB was lifted at the connector and then connection was made to the IC direct via a stiff copper wire. No change was observed.

5.1.3. Altering the grounding of the Input Voltage sense

The filter capacitors of the input voltage sense (that has a shut-down capability) share a common path with the current sense filter capacitors. The voltage sense capacitors were lifted and their ground connection re-routed. No change to the problem detected.

5.1.4. Switching spike from the Auxiliary Regulator

It was possible that the auxiliary regulator was causing misbehaviour. The fuse to the aux regulator from V_{HT} was lifted and the circuit powered from a bench supply. No change to the problem.

5.1.5. Double pole filter

Adding an extra 220R resistor and 1.5nF capacitor (direct to pin 1 of the IC) produced a reduction of the problem, but did not eliminate it.

5.1.6. Circuit constants

It became clear that the way the IC controls its output drive train is at the heart of the matter.

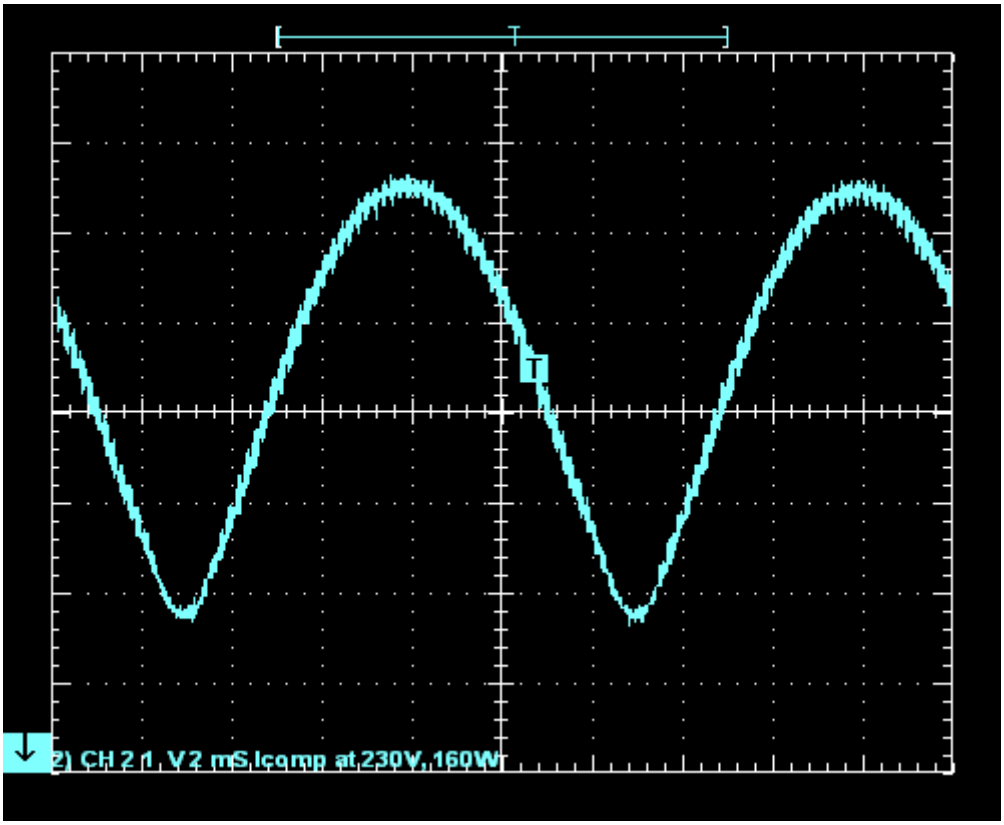

Figure 5.5.1.6.1.6.1 Icomp voltage at 230V input, 160W load

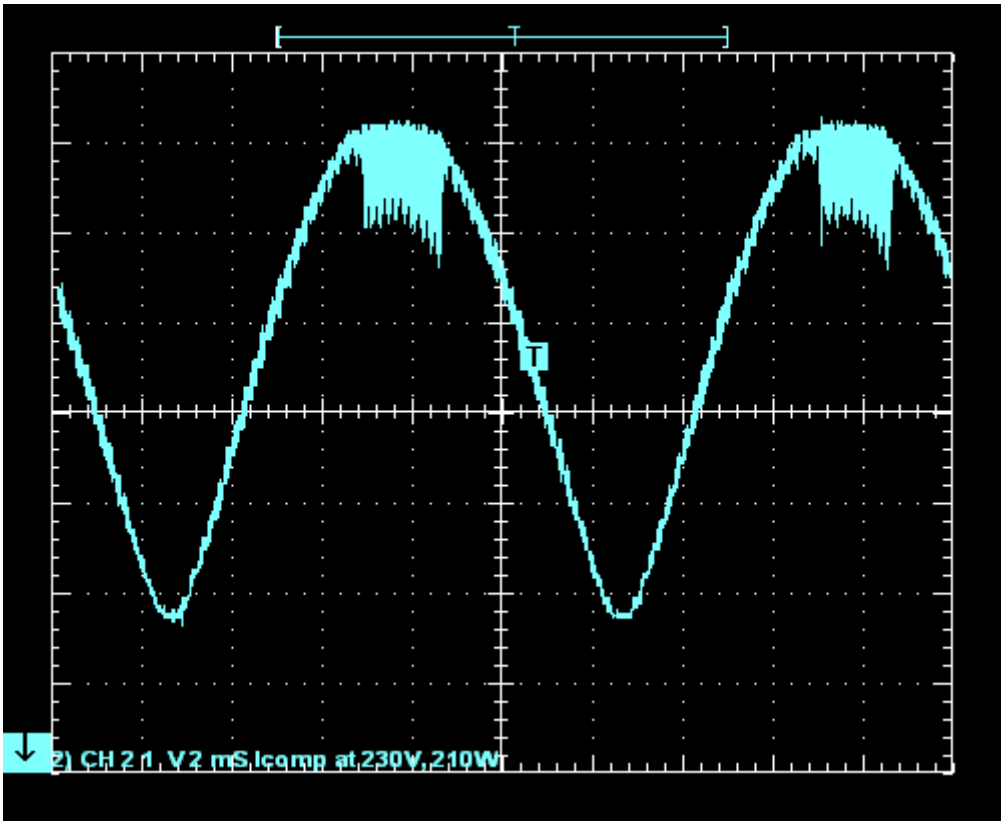

Figure 5.1.6.2 Icomp voltage at 230V 210W

The figure above shows the disturbance to the signal on Icomp that causes missing pulses in the drive train, that cause a disturbance on Isense, resulting in a disturbance on Icomp: positive feedback.

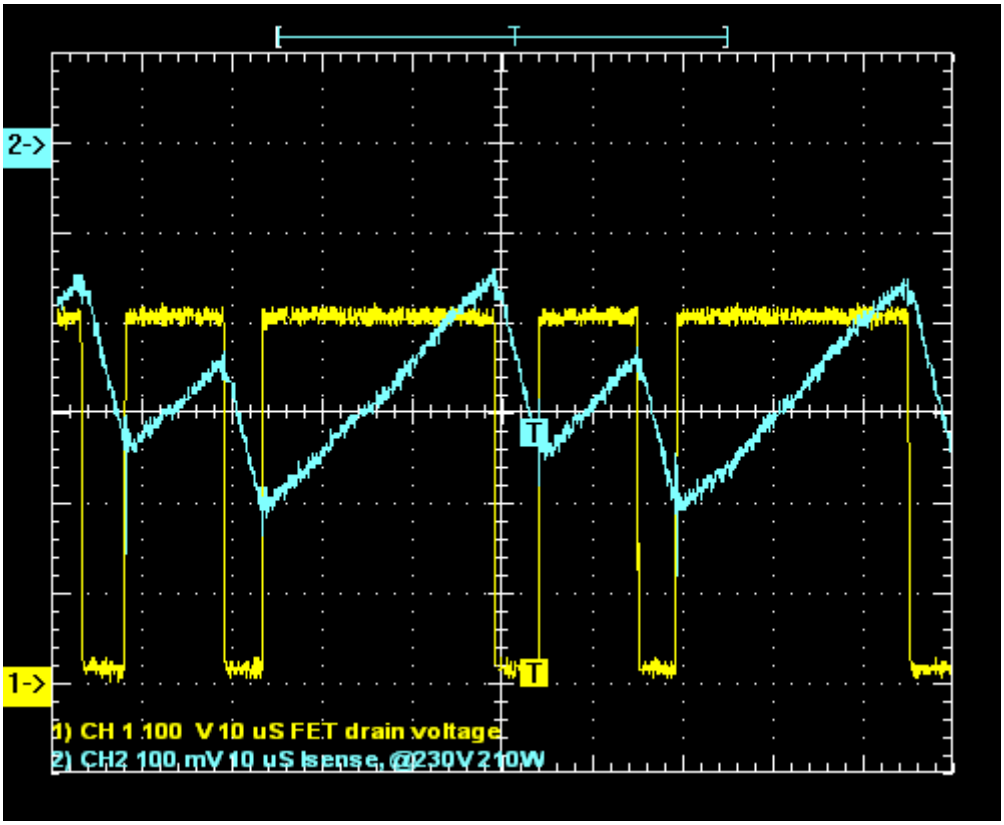

Figure 5.1.6.3 Isense voltage Vs Fet drain

Note that in the trace above the I sense signal is free of spikes and is well away from the peak protection level of -0.7V.

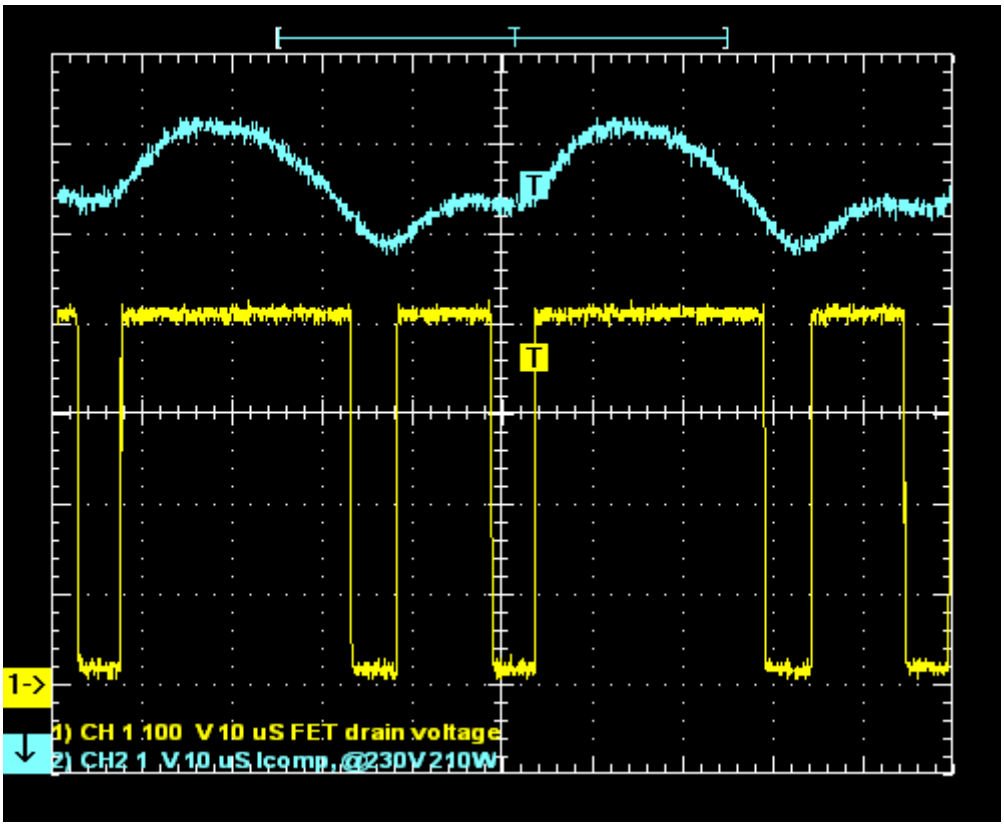

Figure 5.1.6.4 Icomp vs FET drain signal