

DDR3 Power Solutions

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TPS51116 – 3V-28Vin controller + 3A LDO for DDRI/II/III

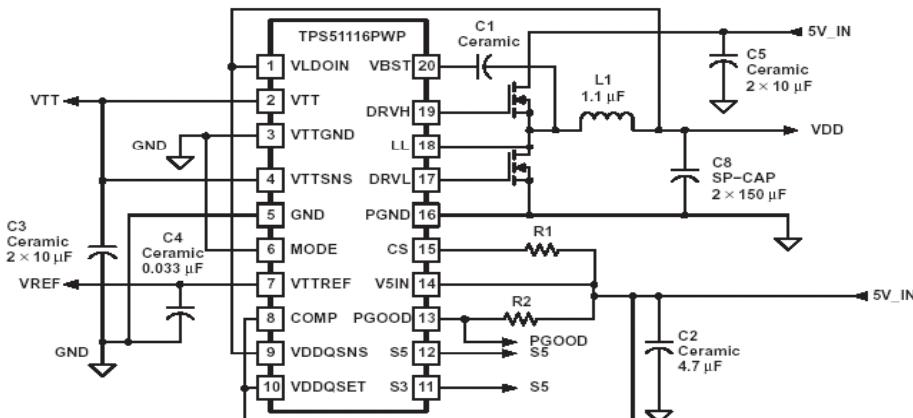
Features

- Adaptive On-Time Current Mode control
- D-CAP™ Mode for Integrated Loop Compensation
- Selectable Current Mode Option
- Integrated sleep state control for S3/S4/S5 States
- Current Sensing from both RDSon or Resistor
- Configurable for 2.5V (DDR), 1.8V (DDR II), 1.5V (DDR3), 1.35V (LPDDR3), or Adj.
- LDO Input Available
- Capable to Sink and Source 3A Peak
- Requires only **20uF Ceramic Output Capacitor**
- Buffered Low Noise 10mA VTTREF Output
- Accuracy +/-20mV for both VTT and VTTREF
- OVP, UVP, Thermal Shutdown, Power Good

ONE OF THE WORLD'S MOST POPULAR
DDR POWER SOLUTIONS

Benefits

- Fastest Transient Response, lowest output ripple
- No loop compensation makes easier to use
- Supports all output cap. types including ceramic
- Supports High-Z in S3 and Discharge in S4/S5
- High efficiency or high current sense accuracy
- Flexibility to support all DDR systems
- Reduces total power dissipation
- Can power high-current DDR termination
- Low BOM cost, small PCB area
- Meets JEDEC DDR Power requirements
- Meets JEDEC DDR Power requirements
- Full suite of system protection



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Schedule of New DDR Power Products

| Part Number | Application | Package | Eng. Sample Date | RTM Date |
|----------------|--|--|------------------|----------|
| TPS51216/59216 | DCAP/DCAP2 DDR3 or LPDDR3 controller with VTT LDO (1x 10uF) for 1.5V or other rail | 20-pin 3x3 mm QFN 0.4mm pitch (RUK) | 9/2010 | Now |
| TPS51206 | VTTLDO: 1A TDC/2A Imax/3A OCL | 10-pin 2x2 mm SON 0.5mm pitch (DSQ) | 10/2010 | 04/2011 |

TPS51216 - New DDR2/3/3L Solution

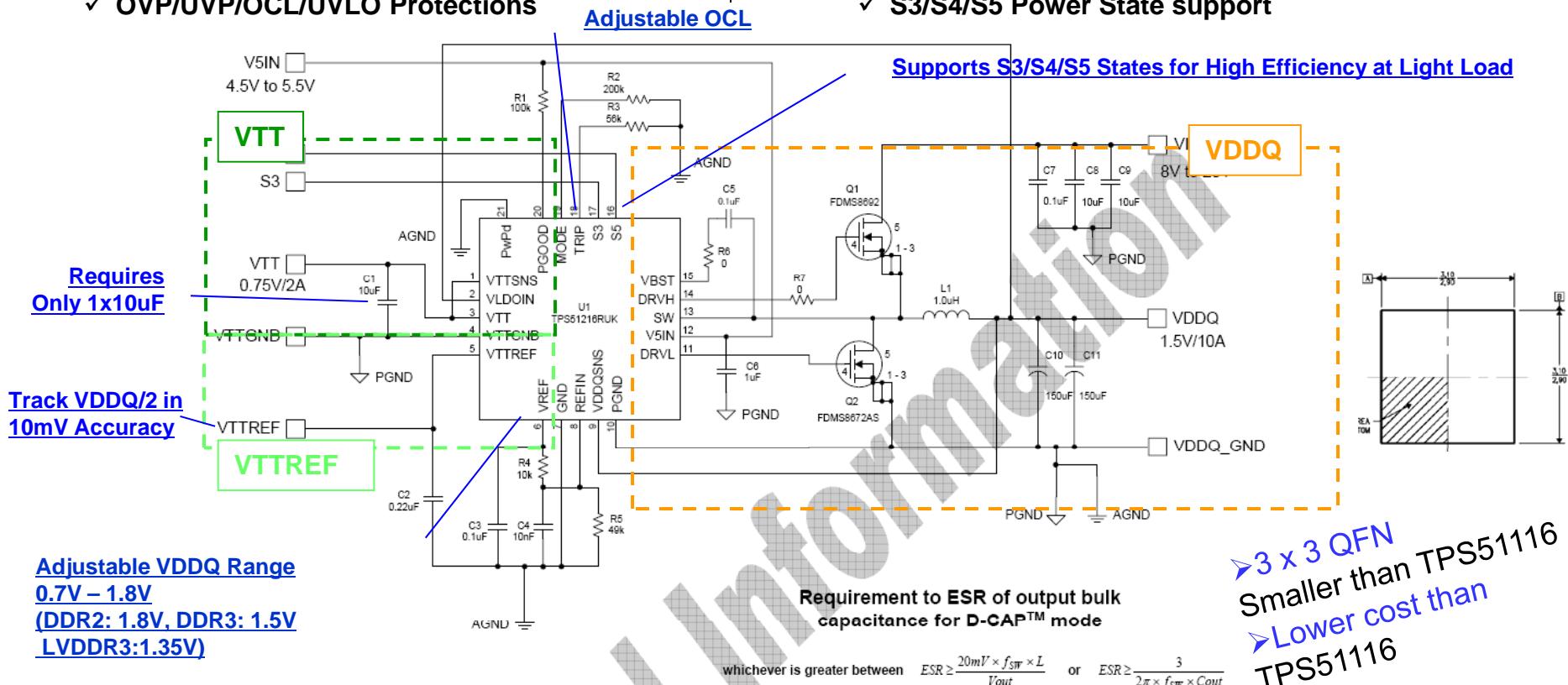
Features

- Synchronous Buck Controller (VDDQ)

- ✓ VIN:3V-28V, VDDQ:0.7V-1.8V
- ✓ 0.8% VREF Accuracy
- ✓ Selectable D-CAP™ 300kHz, 400kHz Fsw Architectures
- ✓ No External Compensation Required
- ✓ OVP/UVP/OCL/UVLO Protections

- ±2A LDO (VTT), Buffered Reference (VTTREF)

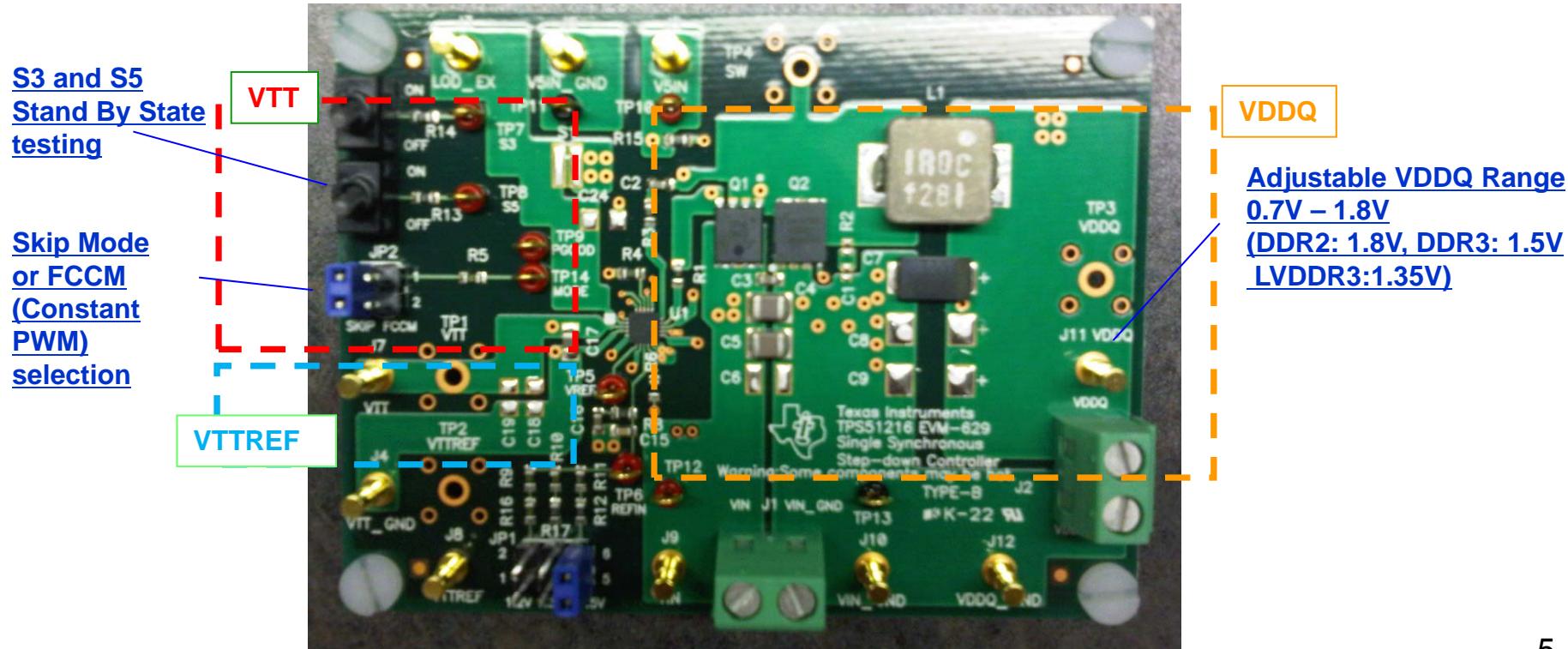
- ✓ 2A Peak Sink/Source Current (VTT)
- ✓ 10mA Buffered Low Noise Reference (VTTREF)
- ✓ LDO Input for Higher Efficiency
- ✓ 0.8% VTTREF, and 20mV VTT Accuracy
- ✓ Require Only 1x10uF Capacitor for VTT
- ✓ S3/S4/S5 Power State support



TPS51216 EVM - New DDR2/3/3L Solution

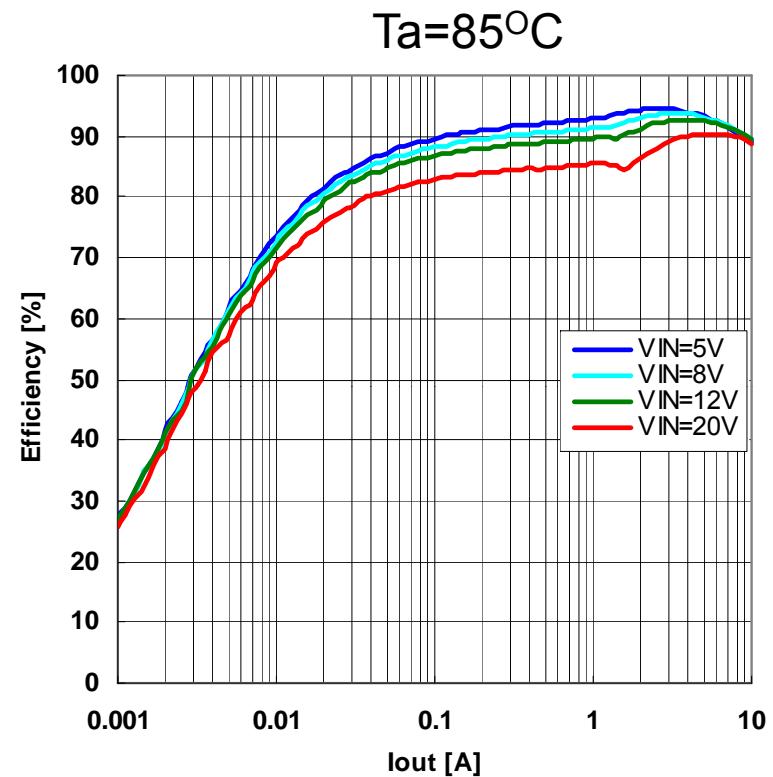
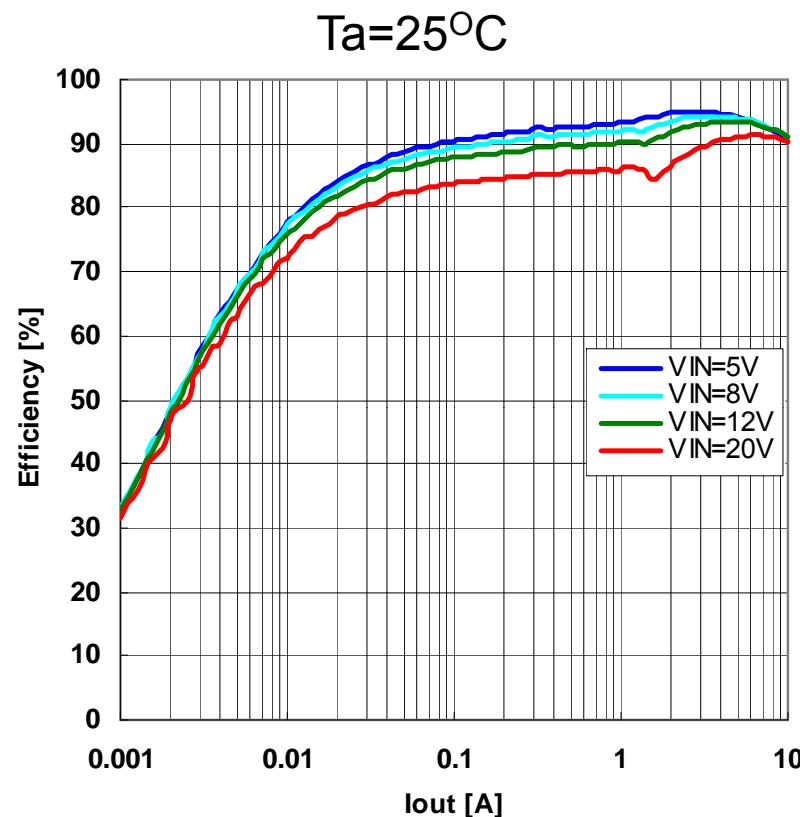
Features

- Complete DDR/DDR2/DDR3/LVDDR3 evaluation platform
- VIN, VOUT connections and all DDR-relevant test points



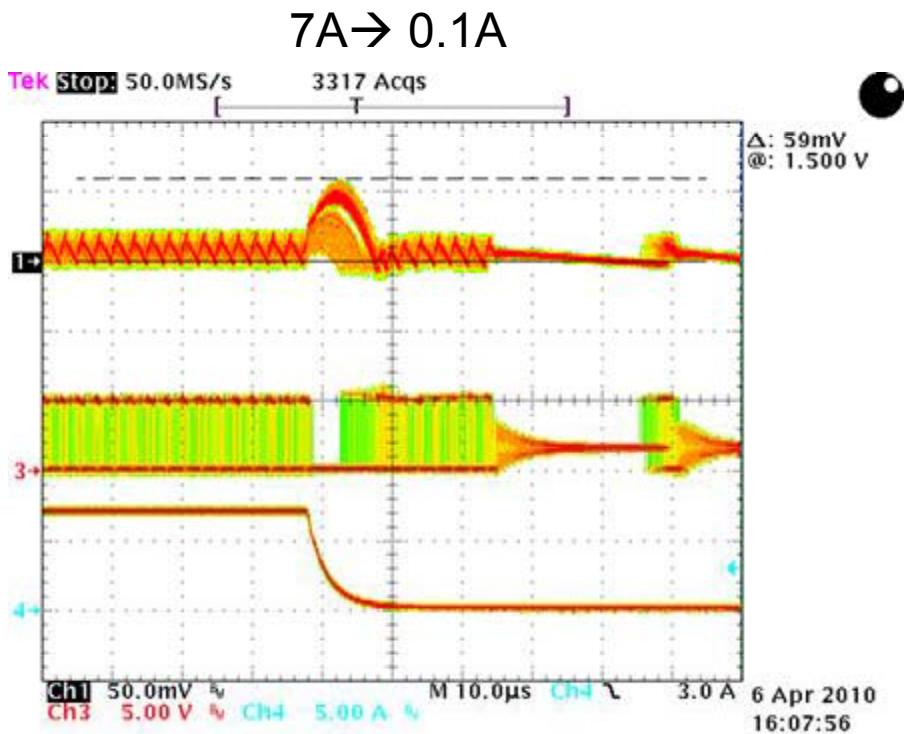
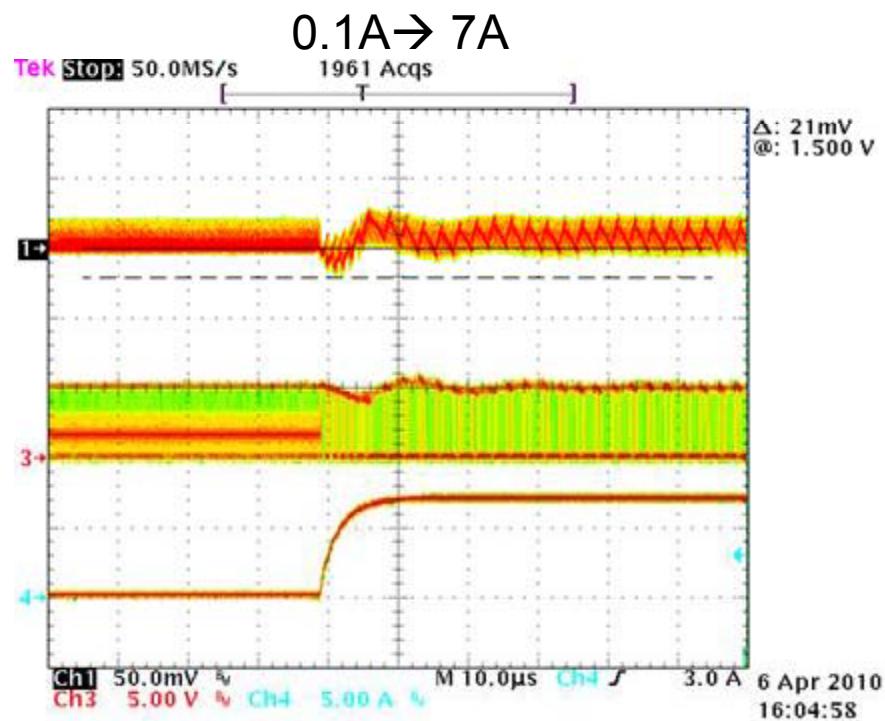
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Efficiency Performance at 1.5V_{OUT}



| | | | |
|----|-------|---------------------|--------------|
| Lx | 1.0uH | 1.0uH, 2.3mΩ, 18.5A | MPC1055L1R0C |
| C7 | 150uF | 150uF, 15mΩ, 6.3V | EEFCX0J151R |
| C8 | 150uF | 150uF, 15mΩ, 6.3V | EEFCX0J151R |
| Q1 | | 30V, 28A, 9.0mΩ | FDMS8692 |
| Q2 | | 30V, 28A, 5.0mΩ | FDMS8672AS |

Load Transient Performance



TPS51116 / TPS51216 Comparison

| | TPS51116 | TPS51216 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------------|--|---|-----------------|-------------------------------------|----------|---|----------|----------------------------------|-----|---|------------------|-----------------|-------------------------------------|---|---|----------|----------------------------------|-----|---|--|-----|-----|----------|-----|-----|-----|-----|-----|-----|
| Package | 4x4mm- 24 pin, 0.5mm pitch | 3x3 mm- 20pin, 0.4mm pitch | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Switching Frequency | D-cap, 400kHz | D-cap: 300kHz/400kHz | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VTTLDO | 2 x 10uF decoupling | 1 x 10uF decoupling | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Voltage Feedback | Resistor divider of output voltage | Voltage reference divider; less jitter, voltage dynamic change support | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Gate Drive | <table border="1"> <tr> <td rowspan="2">R_{ORH}</td> <td rowspan="2">DRVH resistance</td> <td>Source, I_{DRVH} = -100 mA</td> <td>3</td> <td>6</td> <td rowspan="2">Ω</td> </tr> <tr> <td>Sink, I_{DRVH} = 100 mA</td> <td>0.9</td> <td>3</td> </tr> </table> <table border="1"> <tr> <td rowspan="2">R_{ORL}</td> <td rowspan="2">DRVL resistance</td> <td>Source, I_{DRVL} = -100 mA</td> <td>3</td> <td>6</td> <td rowspan="2">Ω</td> </tr> <tr> <td>Sink, I_{DRVL} = 100 mA</td> <td>0.9</td> <td>3</td> </tr> </table> | R _{ORH} | DRVH resistance | Source, I _{DRVH} = -100 mA | 3 | 6 | Ω | Sink, I _{DRVH} = 100 mA | 0.9 | 3 | R _{ORL} | DRVL resistance | Source, I _{DRVL} = -100 mA | 3 | 6 | Ω | Sink, I _{DRVL} = 100 mA | 0.9 | 3 | <table border="1"> <tr> <td>1.7</td> <td>3.0</td> <td rowspan="4">Ω</td> </tr> <tr> <td>0.6</td> <td>1.5</td> </tr> <tr> <td>0.9</td> <td>2.0</td> </tr> <tr> <td>0.5</td> <td>1.2</td> </tr> </table> | 1.7 | 3.0 | Ω | 0.6 | 1.5 | 0.9 | 2.0 | 0.5 | 1.2 |
| R _{ORH} | DRVH resistance | | | Source, I _{DRVH} = -100 mA | 3 | 6 | | Ω | | | | | | | | | | | | | | | | | | | | | |
| | | Sink, I _{DRVH} = 100 mA | 0.9 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | |
| R _{ORL} | DRVL resistance | Source, I _{DRVL} = -100 mA | 3 | 6 | Ω | | | | | | | | | | | | | | | | | | | | | | | | |
| | | Sink, I _{DRVL} = 100 mA | 0.9 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1.7 | 3.0 | Ω | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.6 | 1.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.9 | 2.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0.5 | 1.2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Zero Cross Detection | +6mV max comparator offset | Auto zero comparator | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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Smallest VTT LDO: TPS51206 (Sijimi)

Features

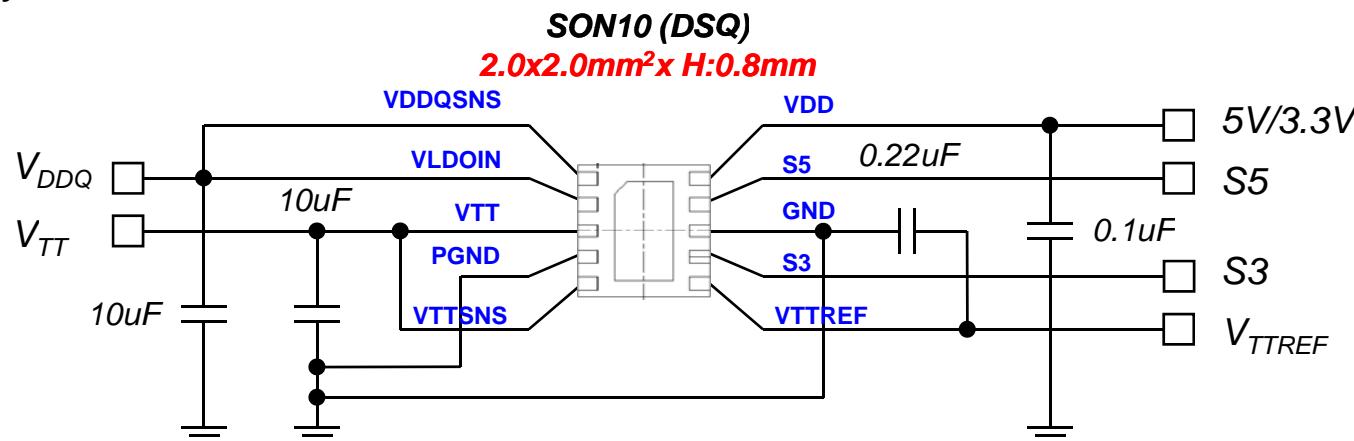
VTT / VTTREF

- 1A TDC, 2A peak sink/source VTT LDO
- 10mA buffered VTTREF LDO
- Supports high-Z in S3, soft-off discharge in S4/S5
- **1x10uF VTT output capacitance**
- Supports 5V and 3.3V Vdd
- **2.0x2.0mm SON Package**
- Pin Integrity with TPS51100

Benefits

VTT / VTTREF

- Compact solution size
- Support DDR2, DDR3, LPDDR3
- **50% reduction of VTT Cap footprint & cost**
- Flexible for many platforms
- **73% reduction of IC footprint vs. TPS51100**



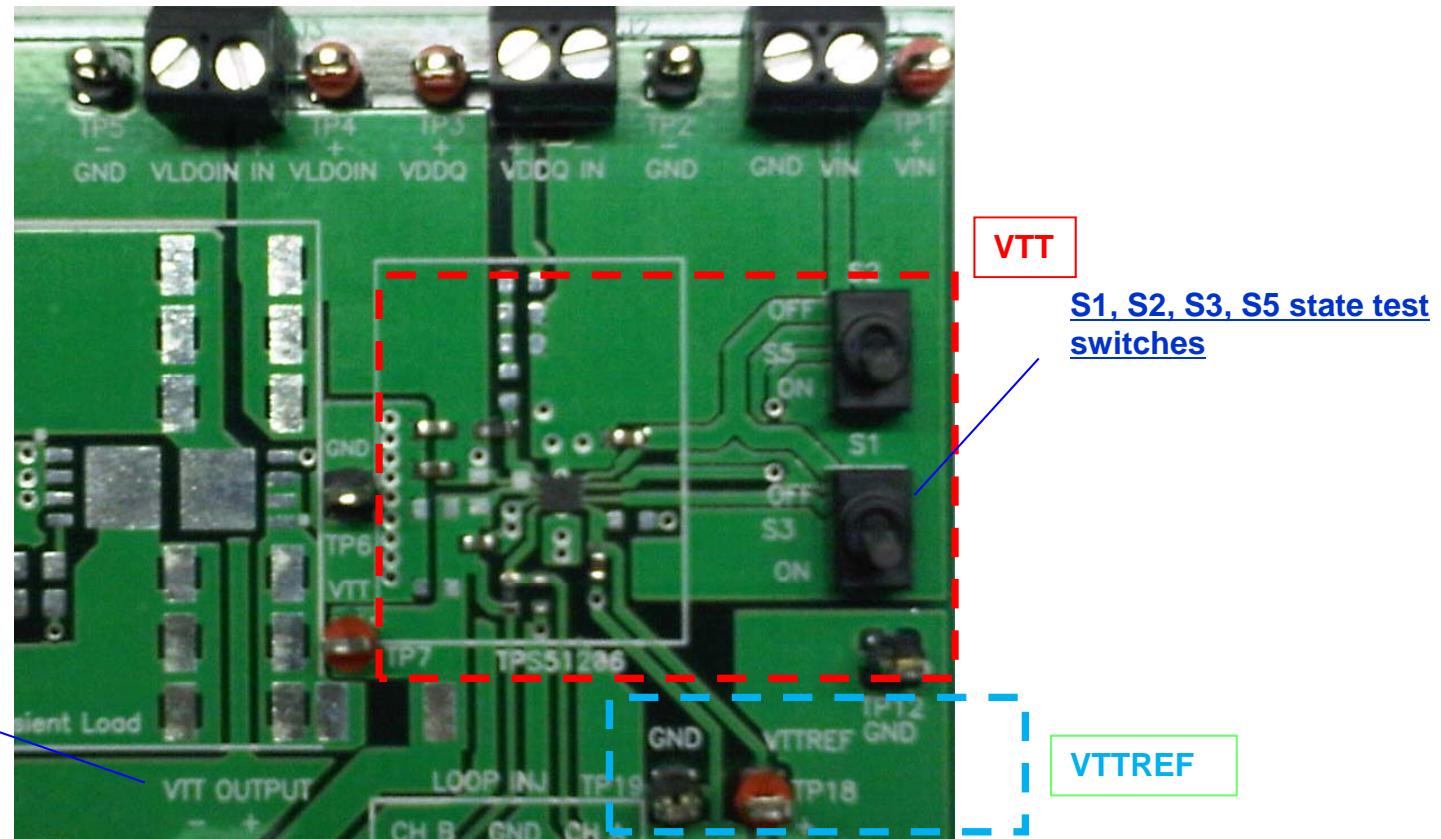
| STATE | S3 | S5 | VTTREF | VTT |
|-------|----|----|--------------------|-----------------|
| S0 | H | H | ON | ON |
| S3 | L | H | ON | OFF (high-Z) |
| S4/S5 | L | L | OFF (discharge) | OFF (discharge) |

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TPS51206 EVM - New DDR2/3/3L +/-2A VTT Solution

Features

- Complete DDR2/DDR3/LVDDR3 VTT (termination) evaluation platform
- VIN, VLDOIN, VDDQ IN, VOUT connections and all DDR VTT-relevant test points



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