

Understanding TPS61175's Pulse-Skipping Function

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ABSTRACT

This application report explains how TPS61175 behaves in Pulse-Skipping mode and how the frequency of the pulse skipping varies with change in different components.

Pulse-Skipping Mode of TPS61175

The TPS61175 is 3A high voltage boost converter with soft start and programmable switching frequency. The TPS61175 regulates the output voltage with current mode pulse width modulation (PWM) control. Once the PWM switch is turned on, the TPS61175 has minimum ON pulse width of 60-ns. This sets the limit of the minimum duty cycle of the PWM switch, and it is independent of the set switching frequency. As the output current drops, the boost converter enters discontinuous conduction mode (DCM). In DCM, the on time is a function of load current. If a very light load current only requires the switch on time to be less than 60 ns typical (110 ns maximum), the IC enters pulse-skipping mode. In this mode, the device prevents the switch from turning on for one or more switching cycles to prevent the output voltage from rising above the regulated voltage. Compared to normal PWM operation, the output ripple in pulse skipping will be larger.

In a device without pulse skipping, the PWM cycle starts at the rising edge of the clock whenever the PWM comparator output is low. The PWM cycle ends when PWM comparator output goes high. (see cycles T1, T2 and T4 in Figure 1).

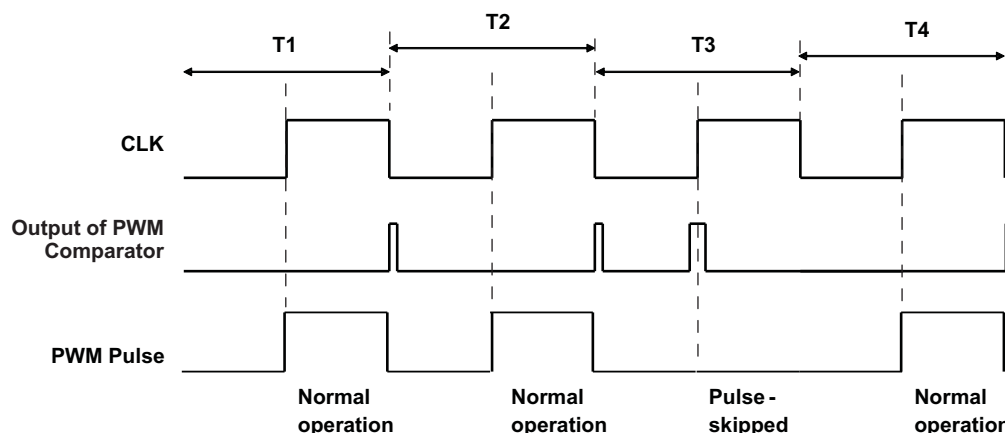


Figure 1. Operation of TPS61175

The TPS61175's pulse skip circuitry operates by checking the output of the PWM comparator just before the CLK rising edge. If the PWM comparator output is high at this moment then one cycle (or pulse) is skipped. The exact relationship between pulse skip frequency and load current is a complex function of L, Co, Vin, Vo and the control loop. Since one input to the PWM comparator is the output of the error amplifier (i.e., the IC's COMP pin), changing the compensation components changes not only the time between switching bursts in pulse skip mode (i.e. the pulse skip frequency) but also the number of pulses within each burst. Specifically, the pulse skipping frequency, f_{PS} varies inversely with the compensation capacitance value and directly with the compensation resistance value. In other words, f_{PS} varies directly with the loop bandwidth of the converter.

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Table 1. Waveform Legend (continued)

Channel	Corresponding Waveform	Vertical Scale	Time Scale
Channel 2 (Red)	AC-coupled output voltage waveform	200 mV/div	1 ms/div
Channel 3 (Blue)	Voltage waveform on COMP pin	200 mV/div	1 ms/div
Channel 4 (Green)	Load Current waveform	200 mA/div	1 ms/div

1. For Output current = 220 μ A

a. $R3 = 3.09 \text{ k}\Omega$, $C4 = 33 \text{ nF} \rightarrow f_{PS} \approx 599.91 \text{ Hz}$

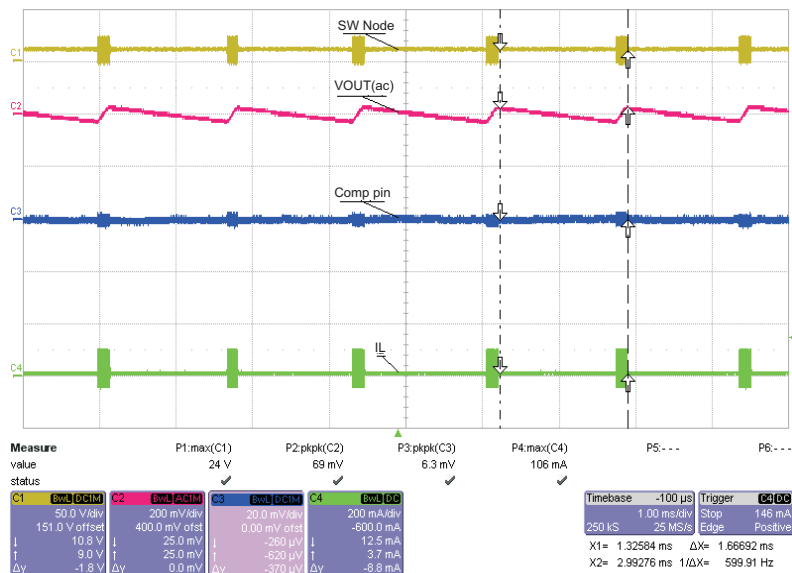


Figure 3. Test Condition 1(a)

b. Same $R3 = 3.09 \text{ k}\Omega$, larger $C4 = 68 \text{ nF}$, lower loop crossover $\rightarrow$ lower $f_{PS} = 755.171 \text{ Hz}$

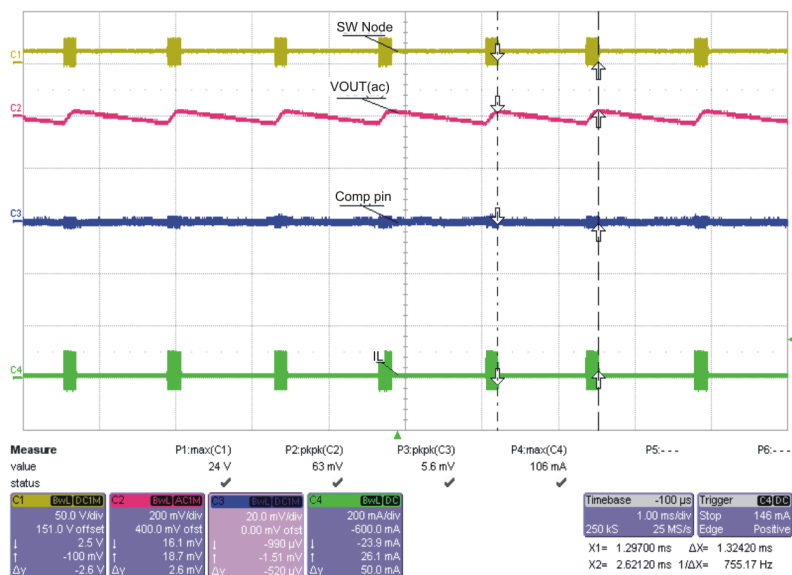


Figure 4. Test Condition 1(b)

c. Smaller $R3 = 1 \text{ k}\Omega$, same $C4 = 33 \text{ nF}$, lower loop crossover $\rightarrow$ lower $f_{PS} = 314.039 \text{ Hz}$

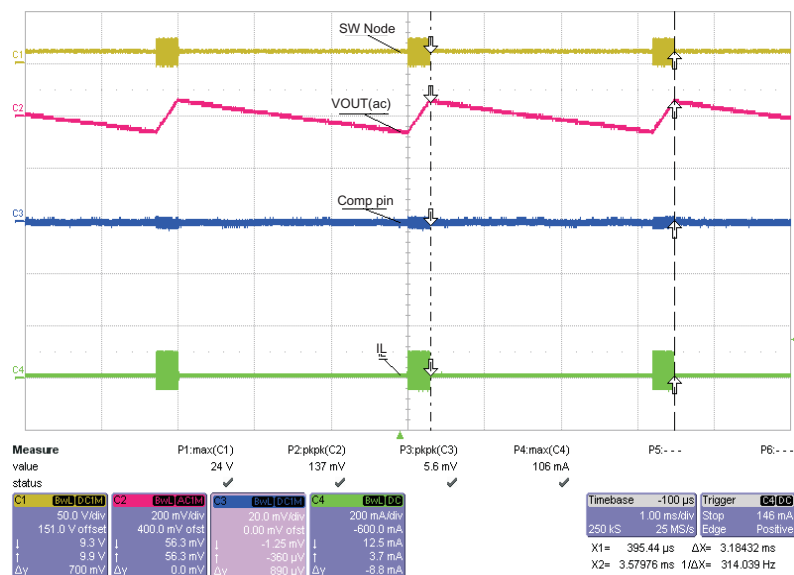


Figure 5. Test Condition 1(c)

2. For Output current = 110 μA

a. $R3 = 3.09 \text{ k}\Omega$, $C4 = 33 \text{ nF} \rightarrow f_{PS} = 340.532 \text{ Hz}$

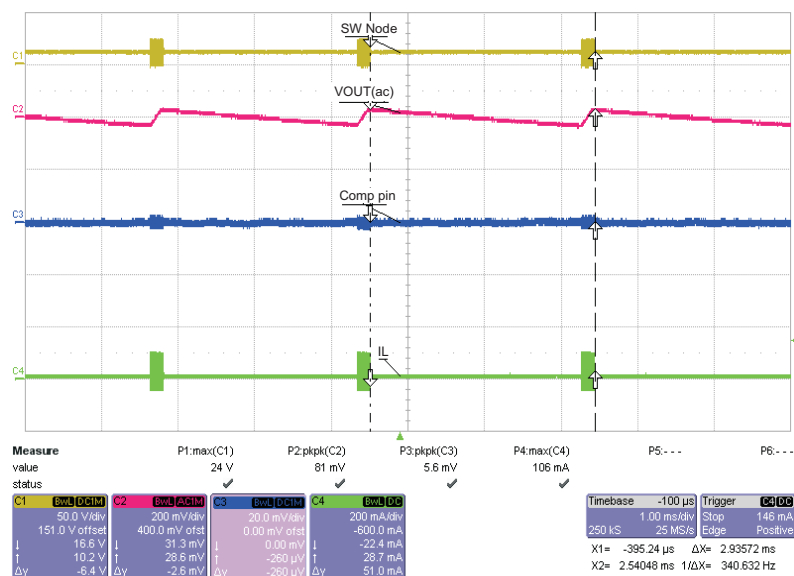


Figure 6. Test Condition 2(a)

b. Same $R3 = 3.09 \text{ k}\Omega$, larger $C4 = 68 \text{ nF}$, lower loop cross over $\rightarrow$ slower $f_{PS} = 533.15 \text{ Hz}$

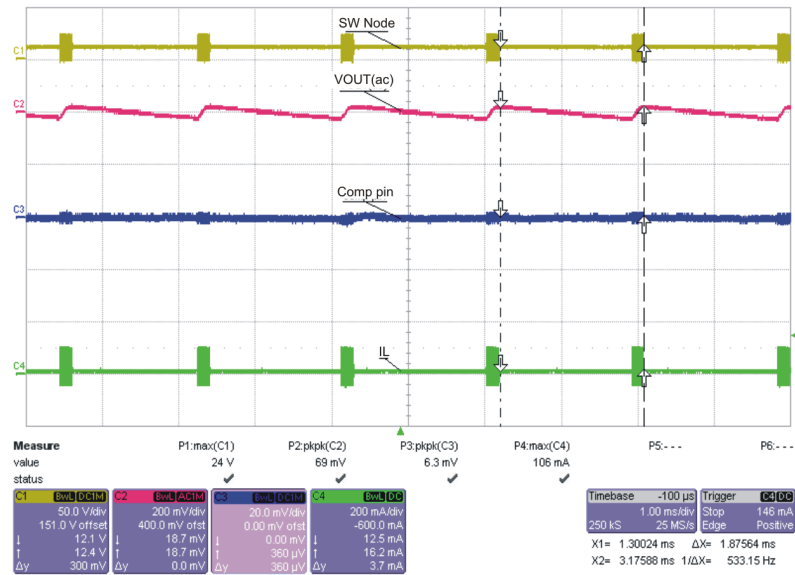


Figure 7. Test Condition 2(b)

c. Smaller R3 = 1 kΩ, same C4 = 33 nF, lower loop crossover → lower $f_{PS} = 230.352$ Hz

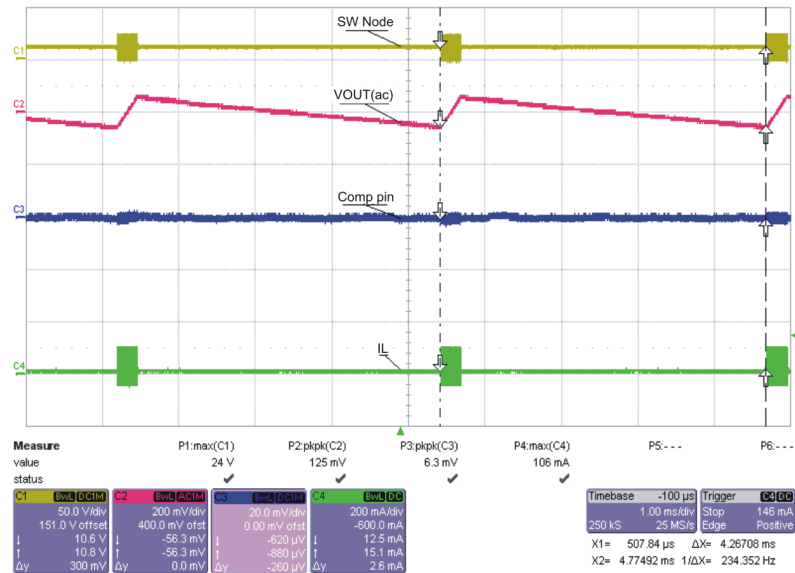


Figure 8. Test Condition 2(c)

Conclusion

The TPS61175 pulse skipping feature operates by simply blanking out the clock pulse, thereby not turning on the FET, if the PWM comparator output is high at the beginning of each clock cycle. The skip cycle threshold can be found using the on time equation in DCM mode; however, the frequency between pulse skip operation bursts varies inversely with the compensation capacitance value and directly with the compensation resistance value. In other words, it varies directly with the loop bandwidth of the converter.

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