TPS56221EVM-579 Evaluation Module

The Texas Instruments TPS56221EVM-579 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.2-V output at up to 25 A from a 12-V input bus. The EVM is designed to start up from a single supply; so, no additional bias voltage is required for start-up. The module uses the TPS56221 High-Current, Synchronous Buck Converter with integrated MOSFETs.

The TPS56221 integrates TI's high-performance controller technology with TI's industry-leading MOSFET technology in a standard QFN package to meet the demands of modern, high-current, space-constrained applications.

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1 Introduction

1.1 Description

TPS56221EVM-579 is designed to use a regulated 12-V (8-V to 14-V) bus voltage to provide a regulated 1.2-V output at up to 25 A of load current. TPS56221EVM-579 is designed to demonstrate the TPS56221 high-current integrated, FET converter in a typical space-limited 12-V bus to low-voltage point-of-load application.

1.2 Applications

- High-current, low-voltage FPGA or microcontroller core supplies
- High-current, point-of-load modules
- Telecommunications equipment
- Computer peripherals

1.3 Features

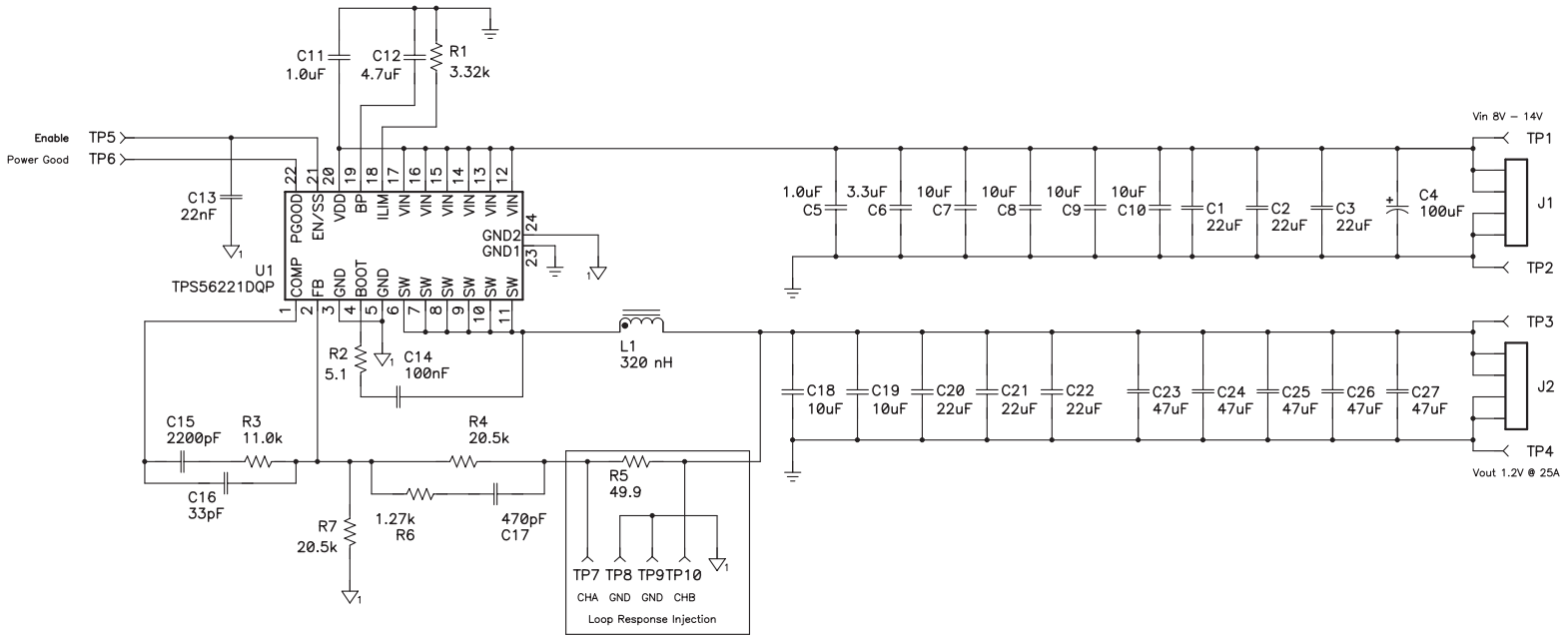
- 8-V to 14-V input voltage rating
- 1.2-V ±2% output voltage rating
- Less than 400-mm^2 active PCB area (excluding bulk input and output capacitors)
- 25-A steady-state load current
- 500-kHz switching frequency
- Simple access to IC features including Power Good, Enable, Soft-Start, and Error Amplifier
- Convenient test points for simple, non-invasive measurements of converter performance.

2 TPS56221EVM-579 Electrical Performance Specifications

Table 1. TPS56221EVM-579 Electrical and Performance Specifications

Parameter		Notes and Conditions	Min	Typ	Max	Unit
Input Characteristics						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = 12 V, I_{OUT} = 25 A	–	2.8	3.2	A
	No-load input current	V_{IN} = 12 V, I_{OUT} = 0 A	–	35	50	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = 10 A		4.2		V
Output Characteristics						
V_{OUT1}	Output Voltage 1	V_{IN} = 12 V, I_{OUT} = 12 A	1.17	1.2	1.23	V
	Line regulation	V_{IN} = 8 V to 14 V	–	–	0.5%	
	Load regulation	I_{OUT} = 0 A to 25 A	–	–	1%	
V_{OUT_ripple}	Output voltage ripple	V_{IN} = 12, I_{OUT} = 25	–	–	24	mVpp
I_{OUT1}	Output Current 1	V_{IN} = 8 to 14	0		25	A
Systems Characteristics						
F_{SW}	Switching frequency		450	500	550	kHz
ηpk	Peak efficiency	V_{IN} = 12 V, I_{OUT} = 12 A	–	92%	–	
η	Full-load efficiency	V_{IN} = 12 V, I_{OUT} = 25 A	–	89%	–	

3 TPS56221EVM-579 Schematic



NOTE: For Reference Only, See Table 3.

Figure 1. TPS56221EVM-579 Schematic

4 Connector and Test Point Descriptions

4.1 Enable/SS Test Point – TP5

TPS56221EVM-579 is designed with a test point at the Enable/Soft-Start point (TP5). Shorting TP5 to GND connects the EN/SS pin to GND, discharges the soft-start capacitor, and disables the TPS56221 converter. This forces the output into a high-impedance state (approximately 40 kΩ to GND).

4.2 Test Point Descriptions

Table 2. Test Point Descriptions

Test Point	Label	Use	Section
TP1	VIN	Measurement Test Point for Input Voltage	Section 4.2.1
TP2	GND	Ground Test Point for Input Voltage	Section 4.2.1
TP3	VOUT	Measurement Test Point for Output Voltage	Section 4.2.2
TP4	GND	Ground Test Point for Output Voltage	Section 4.2.2
TP5	Enable	Measurement Test Point for Enable/Soft-Start	Section 4.2.3
TP6	Power Good	Measurement Test Point for Power Good	Section 4.2.4
TP7	CHA	Measurement Test Point for Channel A of Loop Response	Section 4.2.5
TP8	SGND	Ground Test Point for Channel A of Loop Response	Section 4.2.5
TP9	SGND	Ground Test Point for Channel A of Loop Response	Section 4.2.5
TP10	CHB	Measurement Test Point for Channel B of Loop Response	Section 4.2.5

4.2.1 Input Voltage Monitoring – TP1 and TP2

The TPS56221EVM-579 provides two test points for measuring the input voltage applied to the module. This allows the user to measure the actual input module voltage without losses from input cables and connectors. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive input to TP1 and input terminal to TP2.

4.2.2 Output Voltage Monitoring – TP3 and TP4

The TPS56221EVM-579 provides two test points for measuring the output voltage generated by the module. This allows the user to measure the actual module output voltage without losses from input cables and connectors. All input voltage measurements should be made between TP3 and TP4. To use TP3 and TP4, connect a voltmeter positive input to TP3 and negative input to TP4.

4.2.3 Enable/Soft-Start Monitoring – TP5

The TPS56221EVM-579 provides a test point for measuring the Enable/Soft-Start voltage of the TPS56221 converter. This test point can be externally shorted to GND to disable the TPS56221 controller or monitored to observe the start-up calibration waveform, soft-start ramp, or fault time-out timing.

The Enable/Soft-Start test point can be externally shorted to GND but must not be actively driven from an external circuit, such as a logic output of another power supply.

4.2.4 Power Good Monitoring – TP6

The TPS56221EVM-579 provides a test point for connecting the Power Good output of the TPS56221 converter with an external circuit. To maintain compatibility with the TPS56221EVM-579 Enable/Soft-Start testing point and allow two TPS56221EVM-579 modules to be easily sequenced, the Power Good test point does not include an onboard pullup resistor.

When connecting to another TPS56221EVM-579 module, the Power Good test point (TP6) of one module can be directly connected to the Enable/Soft-Start test point (TP5) of a second module to provide simple sequential start-up sequencing.

If the Power Good test point must be connected to an external logic circuit or monitored for power-on sequence testing, an external pullup may be required.

4.2.5 Loop Response Testing – TP7, TP8, TP8, TP10, and R5

The TPS56221EVM-579 provides four test points (two signal and two ground) for measuring the control loop frequency response. This allows the user to measure the actual module loop response without modifying the evaluation board. A transformer-isolated signal up to 30 mV can be injected between TP7 and TP10. The injected signal amplitude can be measured by the ac-coupled amplitude at CHA (TP7), and the resulting output voltage deviation can be measured at CHB (TP10). See Figure 4 for additional detail.

5 Test Setup

5.1 Equipment

5.1.1 Voltage Source

V_{IN}: The input voltage source (V_{IN}) must be a 0-V to 15-V variable dc source capable of supplying 3.5 Adc.

5.1.2 Meters

A1: Input current meter. 0-Adc to 5-Adc ammeter

V1: Input voltage meter. 0-V to 15-V voltmeter

V2: Output voltage meter. 0-V TO 2-V voltmeter

5.1.3 Loads

LOAD1: Output load. Electronic load set for constant current or constant resistance capable of 0-Adc to 25-Adc at 1.2 Vdc

5.1.4 Oscilloscope

For Output Voltage Ripple: Oscilloscope must be an analog or digital oscilloscope set for ac-coupled measurement with 20-MHz bandwidth limiting. Use 20-mV/division vertical resolution, 1-µs/division horizontal resolution.

For Switching Waveforms: Oscilloscope must be an analog or digital oscilloscope set for dc-coupled measurement with 20-MHz bandwidth limiting. Use 2-V/division or 5-V/division vertical resolution and 1-µs/division horizontal resolution.

5.1.5 Recommended Wire Gauge

VIN to J1
The connection between the source voltage (VIN) and J1 of TPS56221EVM-579 can carry as much as 3.5 Adc of current. The minimum recommended wire size is AWG 16 with the total length of wire less than 2 feet (1-foot input, 1- foot return)

J2 to LOAD1
The connection between the source voltage (VIN) and J1 of TPS56221EVM-579 can carry as much as 25 Adc of current. The minimum recommended wire size is 2x AWG 14 with the total length of wire less than 2 feet (1-foot input, 1-foot return).

NOTE: J2 is a 4 position terminal jack using positions for each VOUT and GND. Each position is rated to support 15A of output current. When delivering more than 15A of current, both VOUT and both GND positions should be used.

5.1.6 Thermal

FAN
The TPS56221EVM-579 evaluation module includes components that can become hot to the touch when operating. Because this evaluation module is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 lfm is recommended to reduce component temperatures when operating.

5.2 Equipment Setup

Shown in Figure 2 is the basic test setup recommended to evaluate the TPS56221EVM-579. Note that although the return for J1 and JP2 are the same system ground, the connections must remain separate as shown in Figure 2.

5.2.1 Procedure

1. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Wearing an electrostatic smock and safety glasses is also recommended.
2. Prior to connecting the dc input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 4 A maximum. Ensure that $_{VIN}$ is initially set to 0 V and connected as shown in Figure 2.
3. Connect VIN to J1 as shown in Figure 2.
4. Connect ammeter A1 between VIN and J1 as shown in Figure 2.
5. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 2.
6. Connect voltmeter V2 to TP3 and TP4 as shown in Figure 2.
7. Connect Oscilloscope Probes to desired test points per Table 2.
8. Locate the fan as shown in Figure 2 and turn it on, ensuring that the air blows directly across the evaluation module.

5.2.2 Diagram

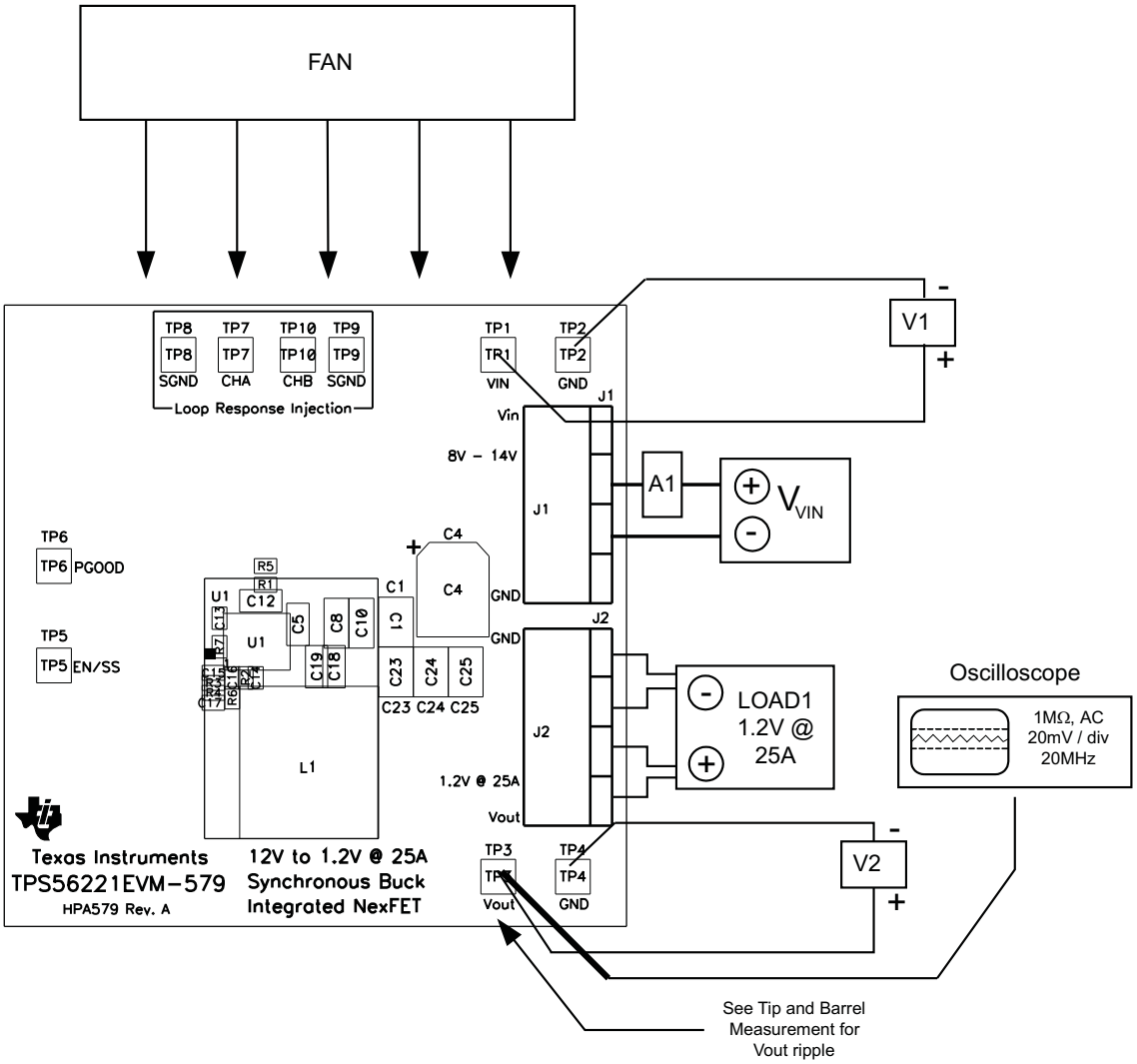


Figure 2. TPS56221EVM-579 Recommended Test Setup

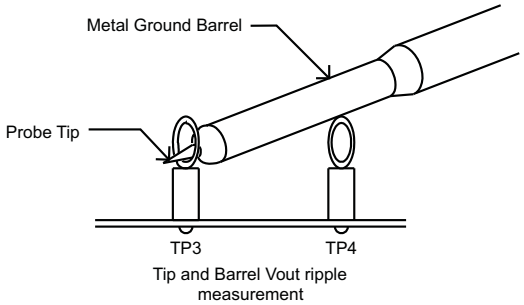


Figure 3. Output Ripple Measurement – Tip and Barrel Using TP3 and TP4

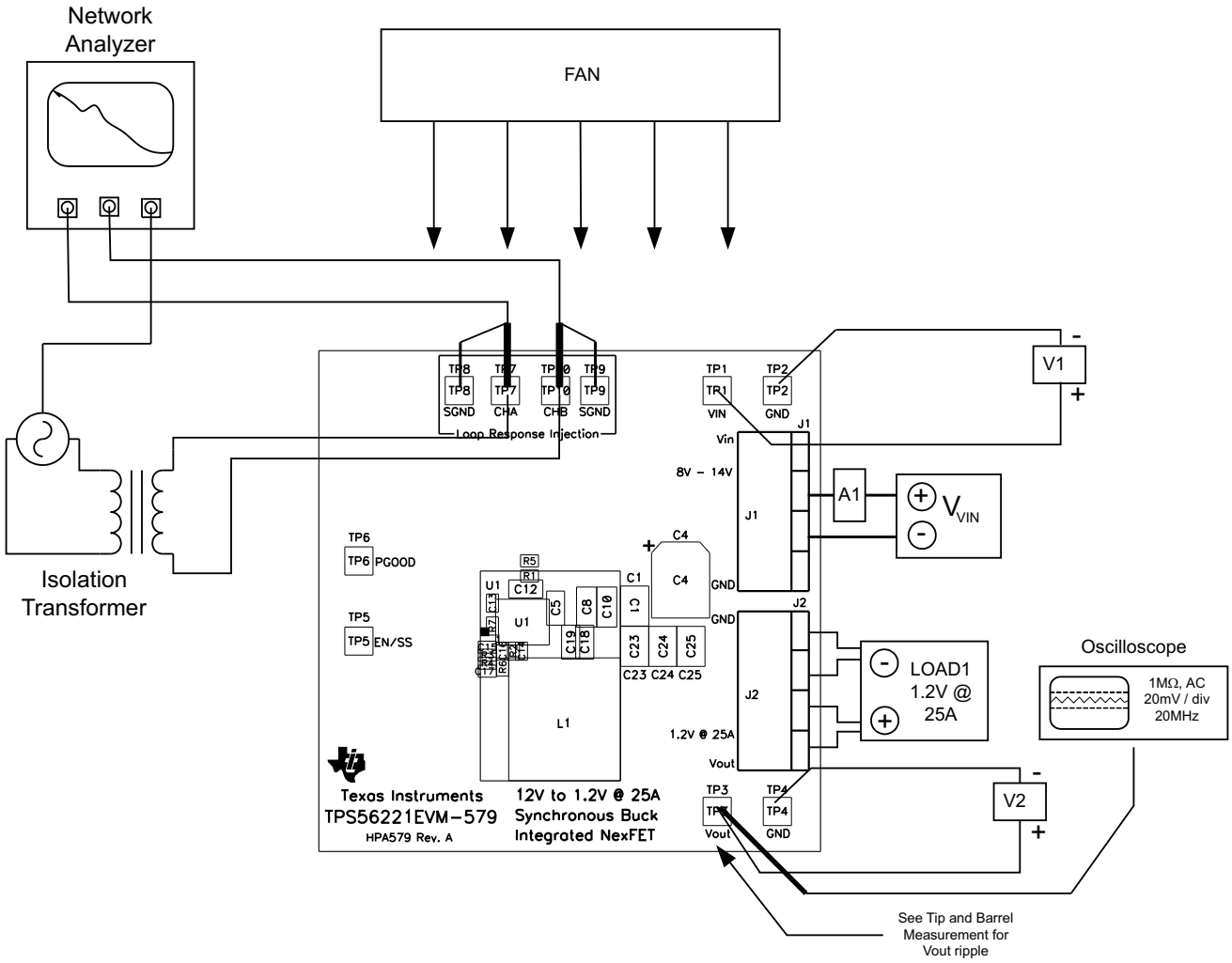


Figure 4. Control Loop Measurement Setup

5.3 Start-Up/Shutdown Procedure

1. Increase VIN from 0 Vdc to 12 Vdc.
2. Vary LOAD1 from 0 Adc to 25 Adc.
3. Vary VIN from 8 V to 14 V.
4. Decrease VIN to 0 V.
5. Decrease LOAD1 to 0 A.

5.4 Output Ripple Voltage Measurement Procedure

1. Follow Section 5.3 Steps 1-5 to set VIN and LOAD1 to desired operating condition
2. Connect Oscilloscope Probe with exposed metal barrel to TP3 and TP4 per Figure 3
3. Set oscilloscope per Oscilloscope For Output Voltage Ripple measurement in Section 5.1.4.
4. Follow Steps 4 and 5 in Section 5.3 to power down.

5.5 Control Loop Gain and Phase Measurement Procedure

1. Follow Steps 1-5 in Section 5.3 to set Vin and LOAD1 to desired operating condition.
2. Connect a 1-kHz to 1-MHz isolation transformer to TP5 and TP7 as shown in Figure 4.
3. Connect input signal amplitude measurement probe (Channel A) to TP7 as shown in Figure 4.
4. Connect output signal amplitude measurement probe (Channel B) to TP5 as shown in Figure 4.
5. Connect ground lead of Channel A and Channel B to TP6 and TP8 as shown in Figure 4.
6. Inject a 30-mV or less signal across R3 through the isolation transformer.
7. Sweep the frequency from 1 kHz to 1 MHz with a 10-Hz or lower post filter.
8. The control loop gain can be measured by $20 \times \text{LOG}\left(\frac{\text{ChannelB}}{\text{ChannelA}}\right)$
9. The control loop phase can be measured by the phase difference between Channel A and Channel B.
10. Follow Steps 4 and 5 in Section 5.3 to power down.

5.6 Equipment Shutdown

1. Shut down oscilloscope.
2. Shut down LOAD1.
3. Shut down VIN.
4. Shut down fan.

6 TPS56221EVM-579 Test Data

Figure 5 through Figure 8 present typical performance curves for the TPS56221EVM-579. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

6.1 Efficiency

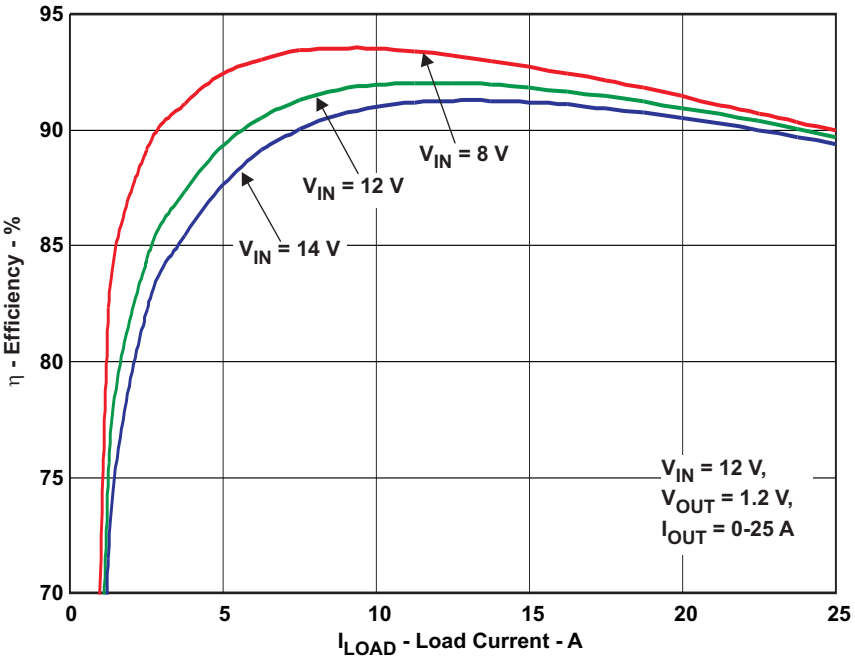


Figure 5. TPS56221EVM-579 Efficiency vs Load Current

6.2 Line and Load Regulation

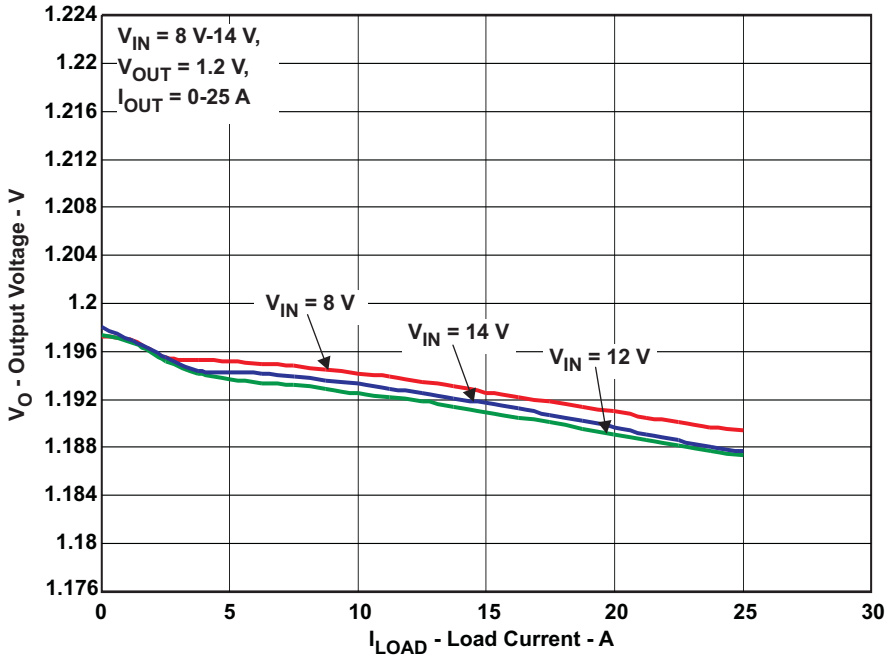


Figure 6. TPS56221EVM-579 Output Voltage vs Load Current

6.3 Output Voltage Ripple

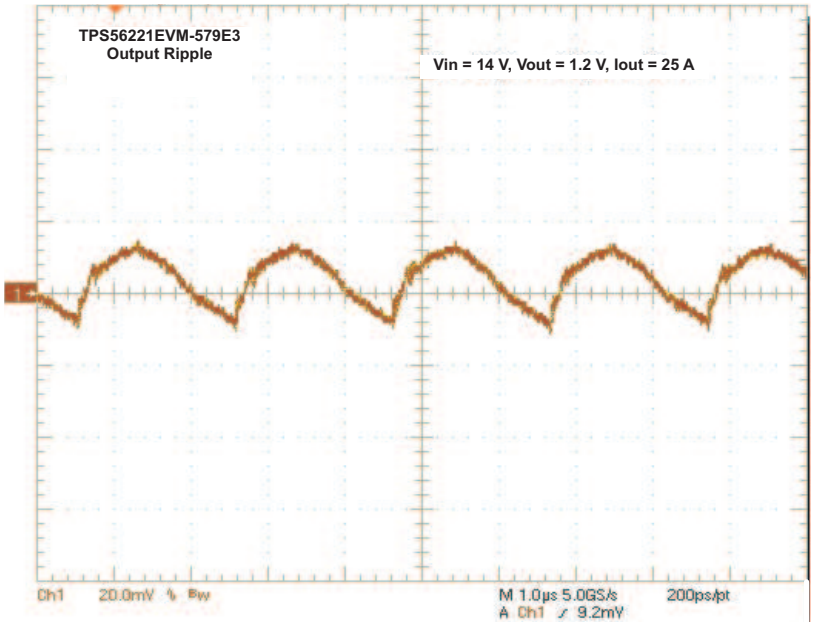


Figure 7. TPS56221EVM-579 Output Voltage Ripple

6.4 Switch Node

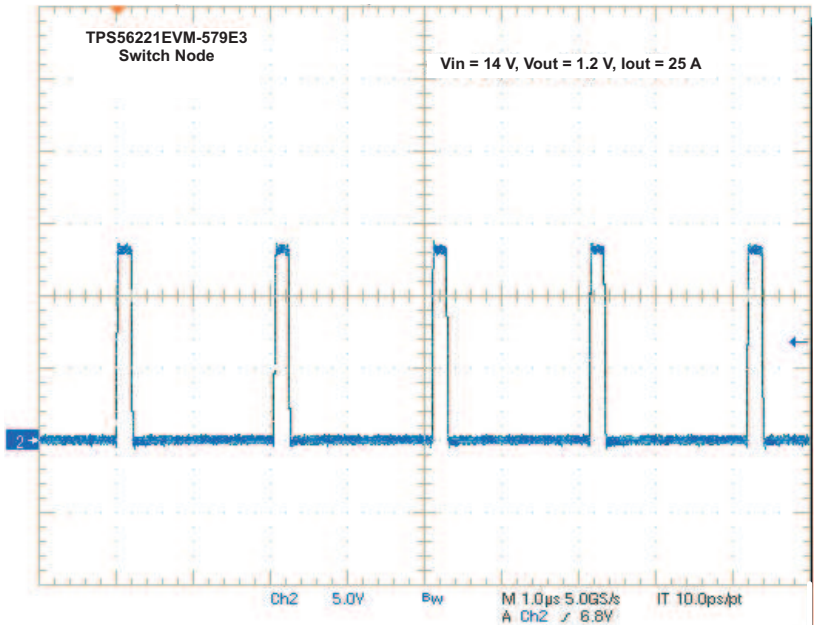


Figure 8. TPS56221EVM-579 Switching Waveform

6.5 Control Loop Bode Diagram

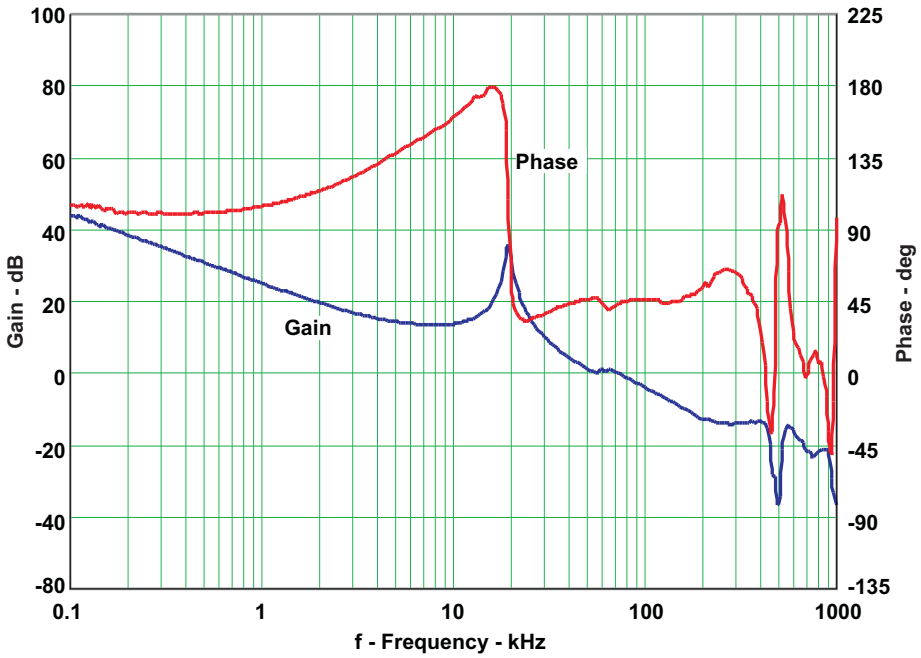


Figure 9. TPS56221EVM-579 Gain and Phase vs Frequency

7 TPS56221EVM-579 Assembly Drawings and Layout

Figure 10 through Figure 15 show the design of the TPS56221EVM-579 printed circuit board. The EVM has been designed using a 4-Layer, 2oz copper-clad circuit board 2.5” x 2.5” with components on both sides of the PCB to allow the user to view, probe and evaluate the TPS56221 high current converter with integrated FET in a small form factor, high-current application.

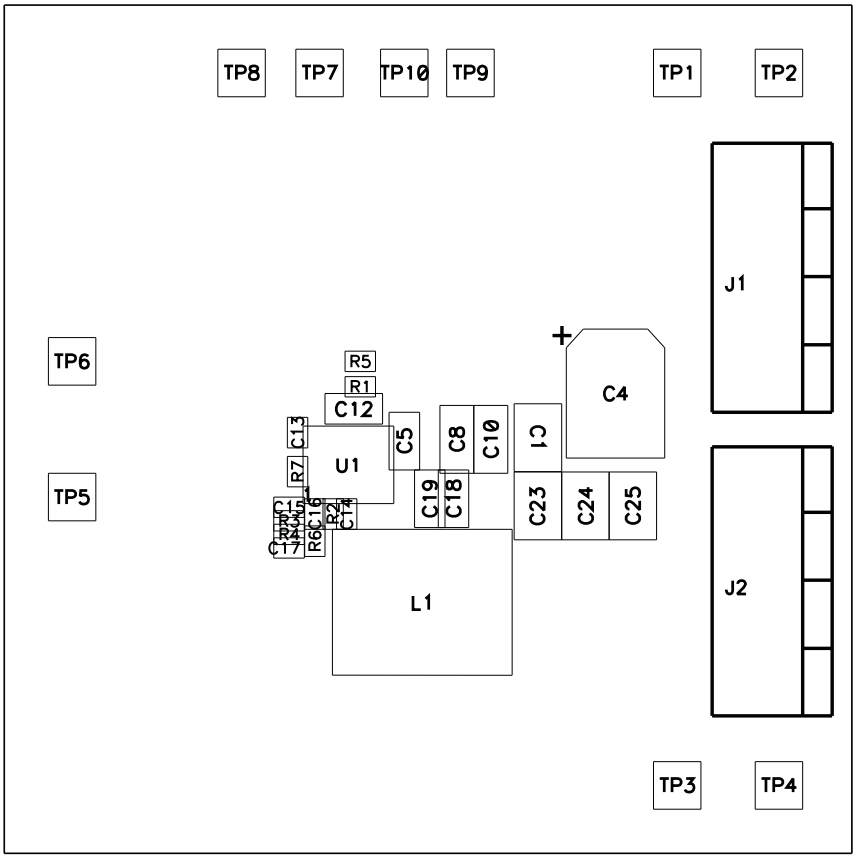


Figure 10. TPS56221EVM-579 Component Placement, Viewed From Top

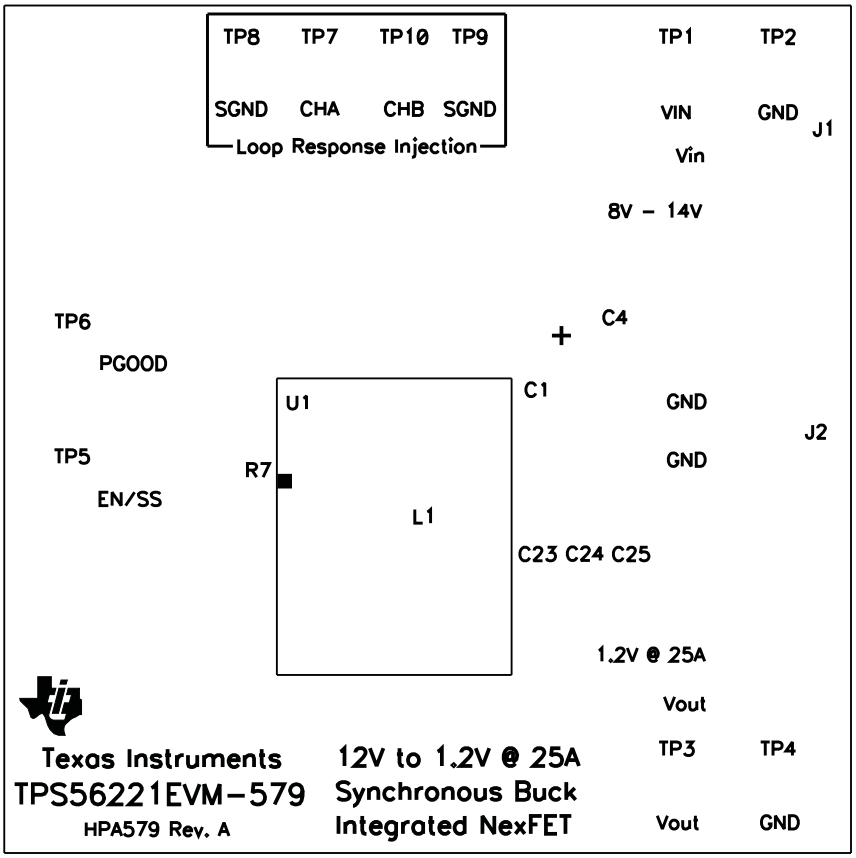


Figure 11. TPS56221EVM-579 Silk Screen, Viewed From Top

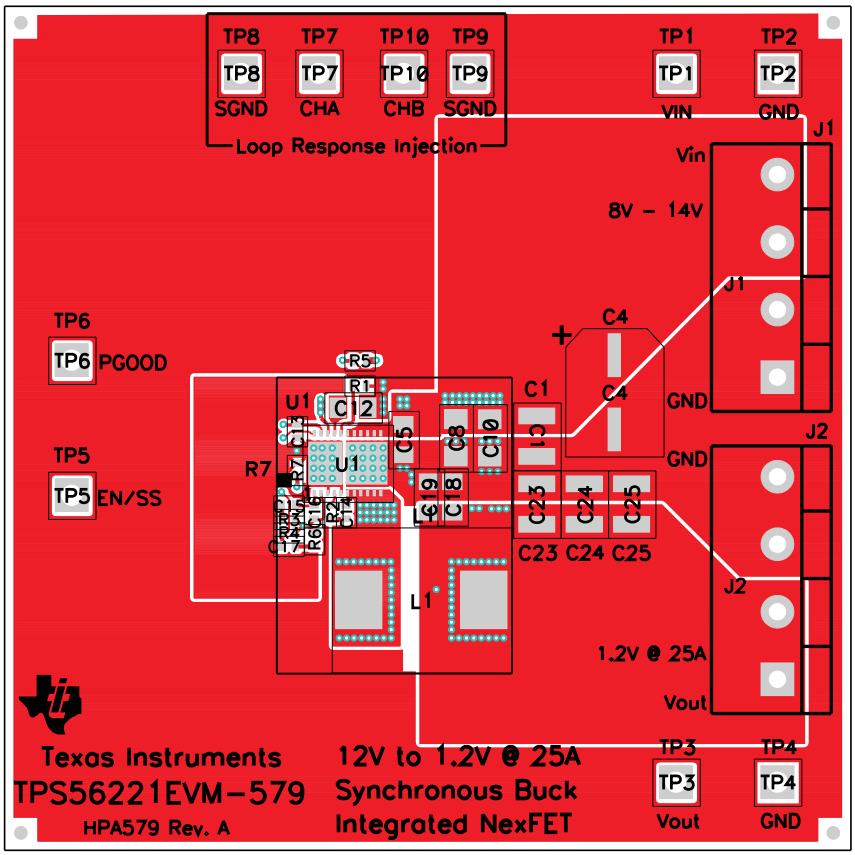


Figure 12. TPS56221EVM-579 Top Copper, Viewed From Top

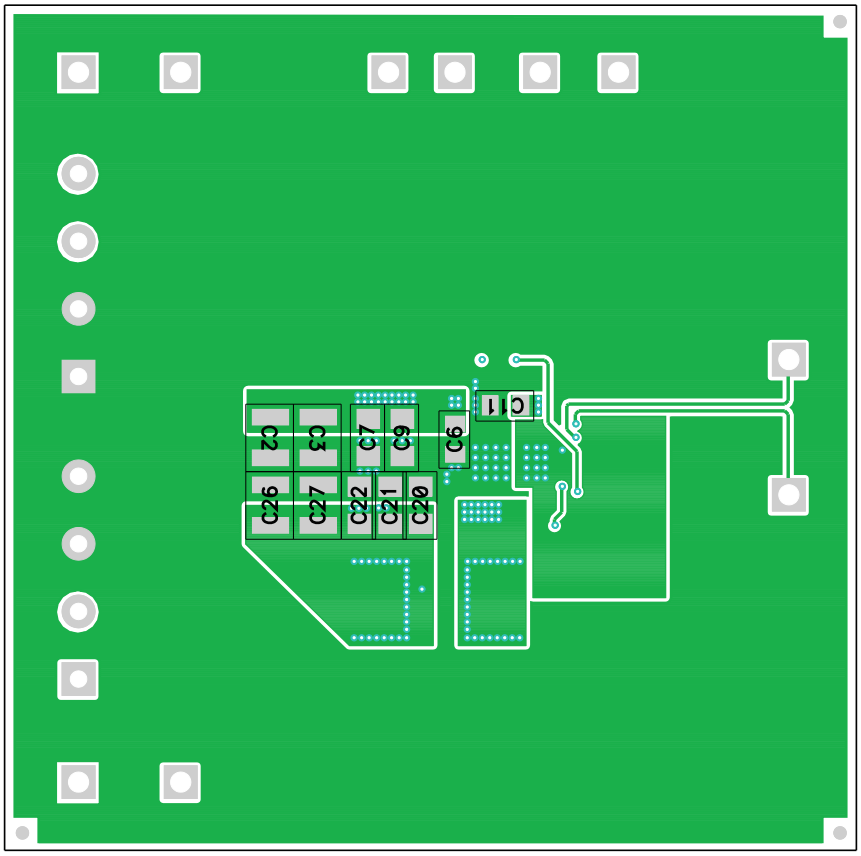


Figure 13. TPS56221EVM-579 Bottom Copper, Viewed From Bottom

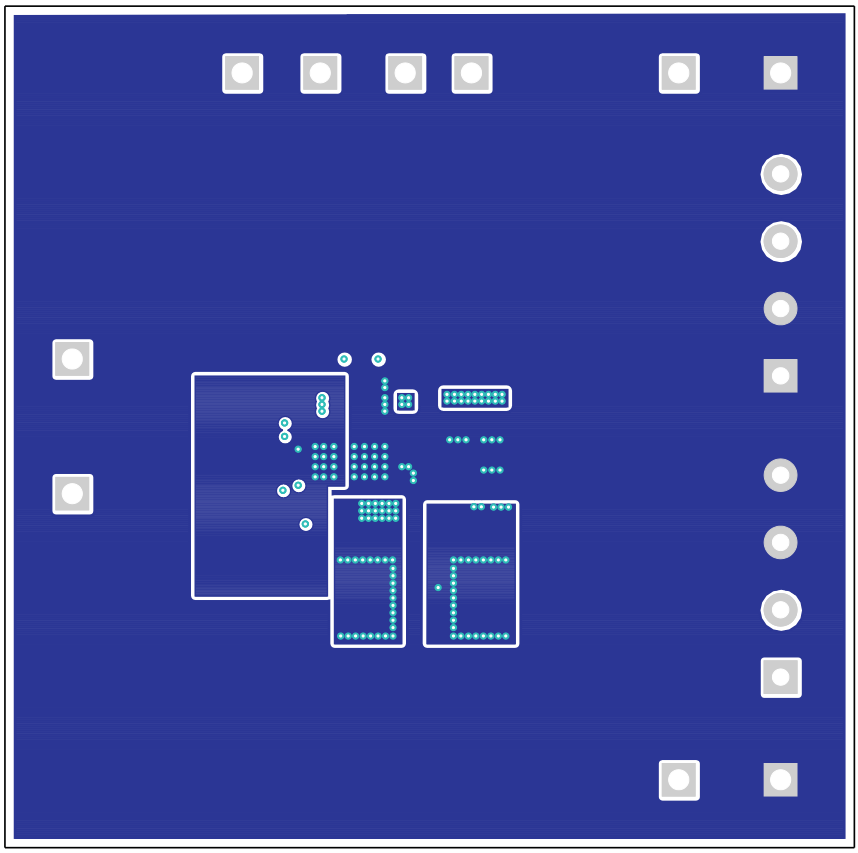


Figure 14. TPS56221EVM-579 Internal 1, X-Ray Viewed From Top

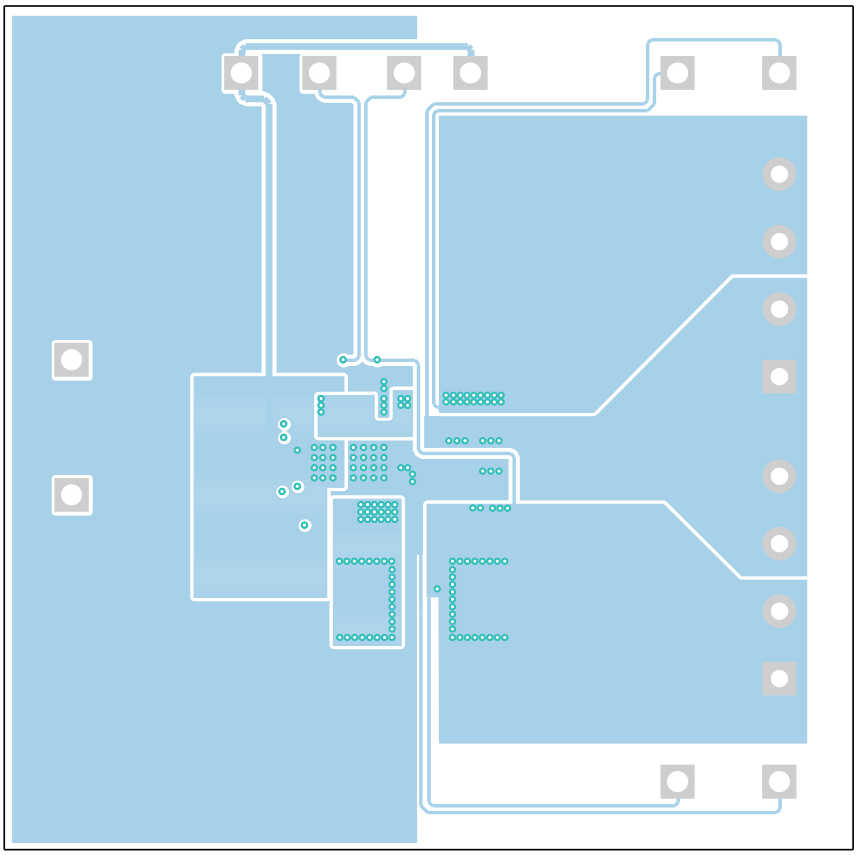


Figure 15. TPS56221EVM-579 Internal 2, X-Ray Viewed From Top

8 TPS56221EVM-579 Bill of Materials

Table 3. TPS56221EVM-579 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
3	C1, C2, C3	22 µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
1	C11	1.0 µF	Capacitor, Ceramic, 25V, X5R, 20%	0805	Std	Std
1	C12	4.7 µF	Capacitor, Ceramic, 10V, X5R, 20%	0805	Std	Std
1	C13	22 nF	Capacitor, Ceramic, 16V, X7E, 20%	0402	Std	Std
1	C14	100 nF	Capacitor, Ceramic, 16V, X7R, 20%	0402	Std	Std
1	C15	2200 pF	Capacitor, Ceramic, 25V, X7R, 10%	0402	Std	Std
1	C16	33 pF	Capacitor, Ceramic, 25V, C0G, 10%	0402	Std	Std
1	C17	470 pF	Capacitor, Ceramic, 25V, C0G, 10%	0402	Std	Std
2	C18, C19	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	Std	Std
3	C20, C21, C22	22 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	Std	Std
5	C23, C24, C25, C26, C27	47 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	Std	Std
1	C4	100 µF	Capacitor, Aluminum, 16VDC, ±20%	Code D8	EEEFP1C101AP	Panasonic
1	C5	1.0 µF	Capacitor, Ceramic, 25V, X7R, 20%	0805	Std	Std
1	C6	3.3 µF	Capacitor, Ceramic, 25V, X7R, 20%	0805	Std	Std
4	C7, C8, C9, C10	10 µF	Capacitor, Ceramic, 25V, X7R, 20%	1206	Std	Std
2	J1, J2	ED120/4DS	Terminal Block, 4-pin, 15-A, 5.1mm	0.80 x 0.35 inch	ED120/4DS	OST
1	L1	320nH	IND, SMT Power ±15%	0.394 x 0.476 inch	PA2202-321NL	Pulse Eng
1	R1	3.31k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R2	5.1	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R3	11.0k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
2	R4, R7	20.5k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R5	49.9	Resistor, Chip, 1/16W, 5%	0402	Std	Std
1	R6	1.27k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
2	TP1, TP3	5010	Test Point, Red, Thru Hole	0.125 x 0.125 inch	5010	Keystone
4	TP2, TP4, TP8, TP9	5011	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
2	TP5, TP6	5014	Test Point, Yellow, Thru Hole	0.125 x 0.125 inch	5014	Keystone
2	TP7, TP10	5012	Test Point, White, Thru Hole	0.125 x 0.125 inch	5012	Keystone
1	U1	TPS56221DQP	IC, 25A 600kHz Synchronous BUCK Converter	QFN-22 6X5 mm	TPS56221DQP	TI
1	–		PCB, 2.5 In x 2.5 In x 0.063 In		HPA579	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 5 V to 14 V and the output voltage range of 0.9 V to 1.8 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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