If a network measurement tool is available, the most accurate compensation design can be achieved following this procedure. The power stage frequency response is first measured using a network analyzer at the 3.6 V input and maximum 2.1 A load. This measurement is shown in Figure 16. In this design only one pole and one zero are used, so the maximum phase increase from the compensation will be 180 degrees. For a 60 degree phase margin, the power stage phase must be –120 degrees at its lowest point. Based on the target 10 kHz bandwidth, the measured power stage gain, $K_{PS}(f_{BW})$, is 13.3 dB and the phase is –87 degrees.

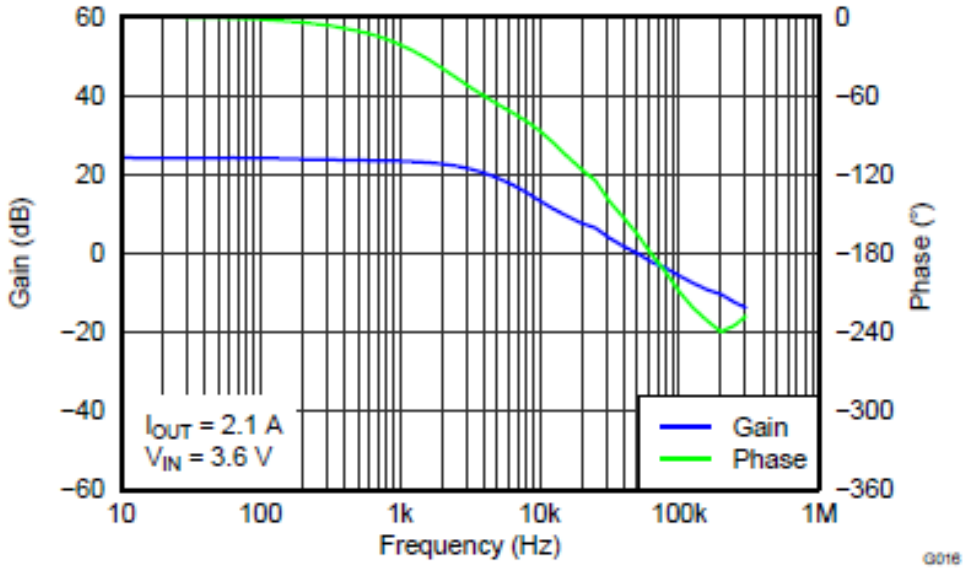

Figure 16. Power Stage Gain and Phase of the Boost Converter

R3 is then chosen to set the compensation gain to be the reciprocal of the power stage gain at the target bandwidth using Equation 38. C4 is then chosen to place a zero at 1/10 the target bandwidth with Equation 39. In this case R3 is calculated to be 1.87 kΩ, the nearest standard value 1.87 kΩ is used. C4 is calculated at 0.085 µF and the nearest standard value 0.10 µF is used. Although not necessary because this design uses all ceramic capacitors, a 270 pF capacitor is selected for C5 to add a high frequency pole at a frequency 100 times the target bandwidth.

$$R3 = \frac{1}{\left(Gea \times \frac{R1}{(R1+R2)} \times 10^{\frac{K_{PS}(f_{BW})}{20}} \right)} \quad (38)$$

Could you tell weather it become R3=1.87kΩ , If which value is used here?