

PMP4660RevD1 Test Results

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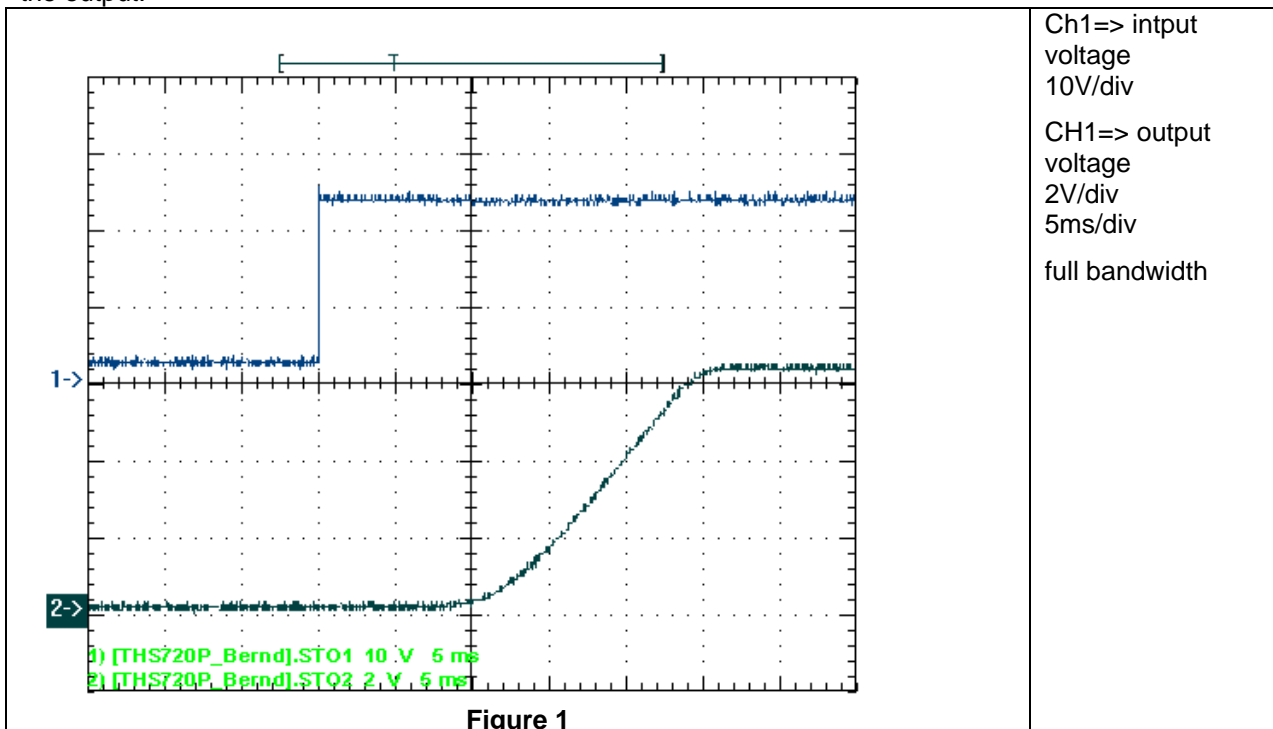
Please note:

**This test report was done w/ HS FET / LS FET SiR426DP;
SiR422DP wasn't available fast enough.
W/ LS FET SiR422DP efficiency will increase a bit !**

PMP4660RevD1 Test Results

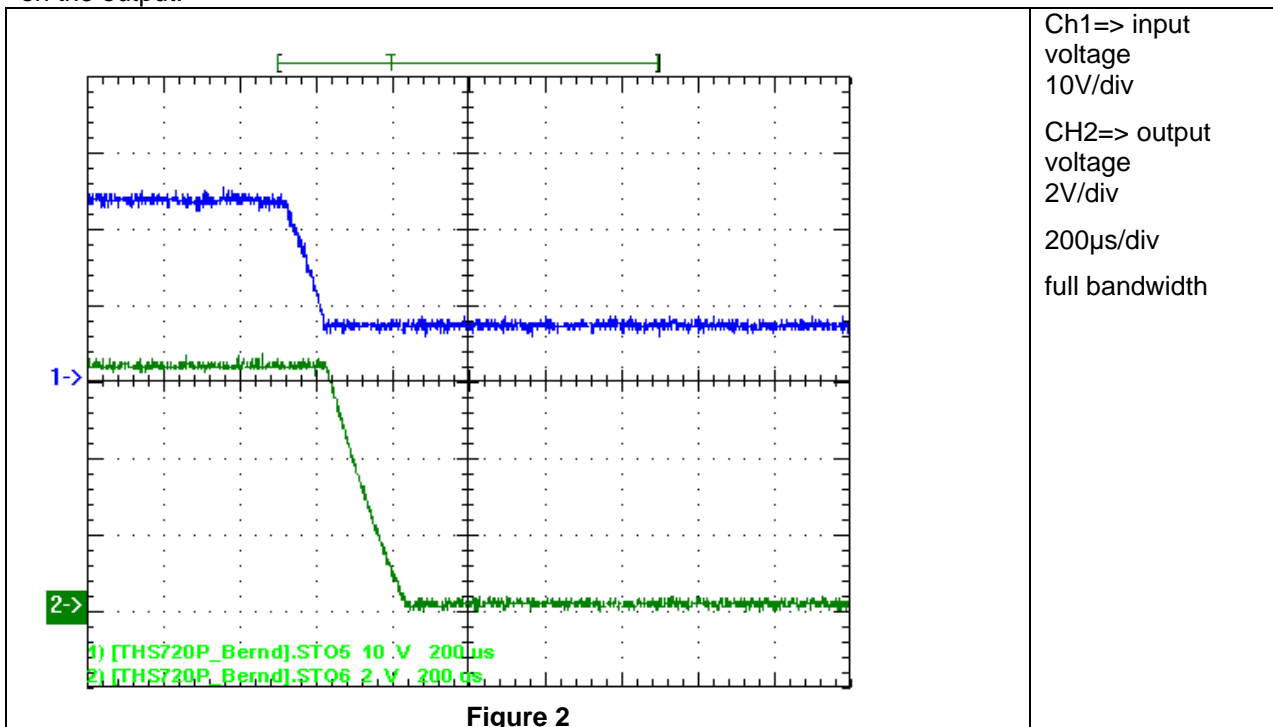
1. Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 24V, with 4A load on the output.



2. Shutdown

The shutdown waveform is shown in the Figure 2. The input voltage was set at 24V, with 4A load on the output.



3. Efficiency

The efficiency is shown in the Figure 3 below. The input voltage was set to 24V.

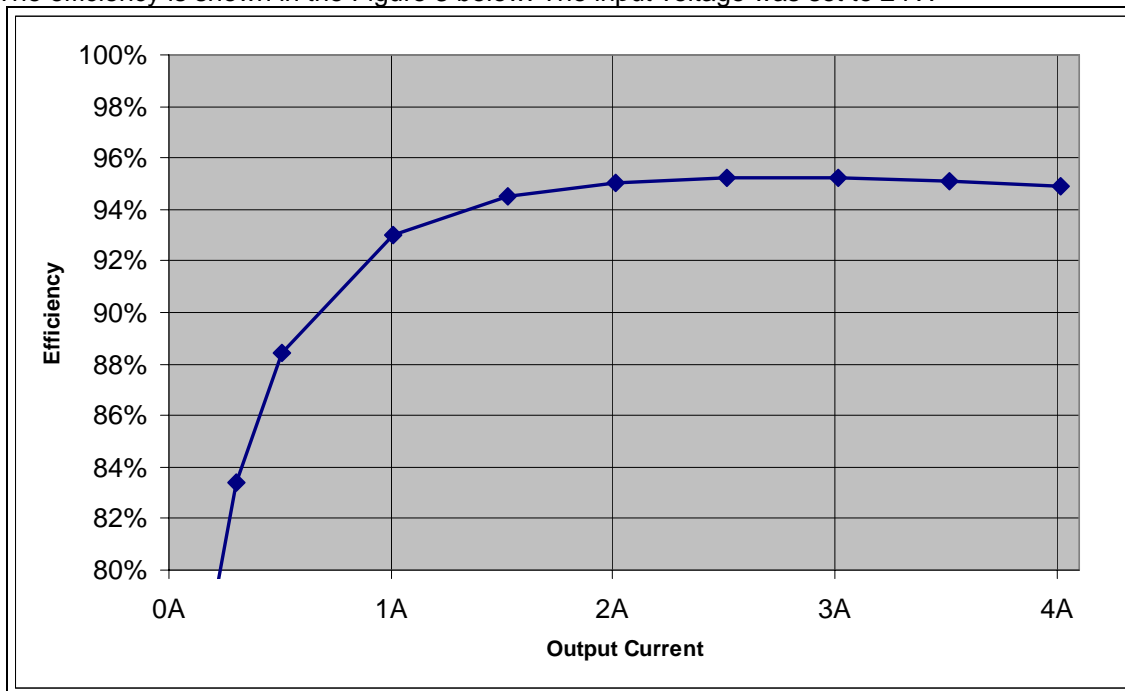


Figure 3

4 Load Regulation

The load regulation of the output is shown in the Figure 4 below. The input voltage was set to 24V.

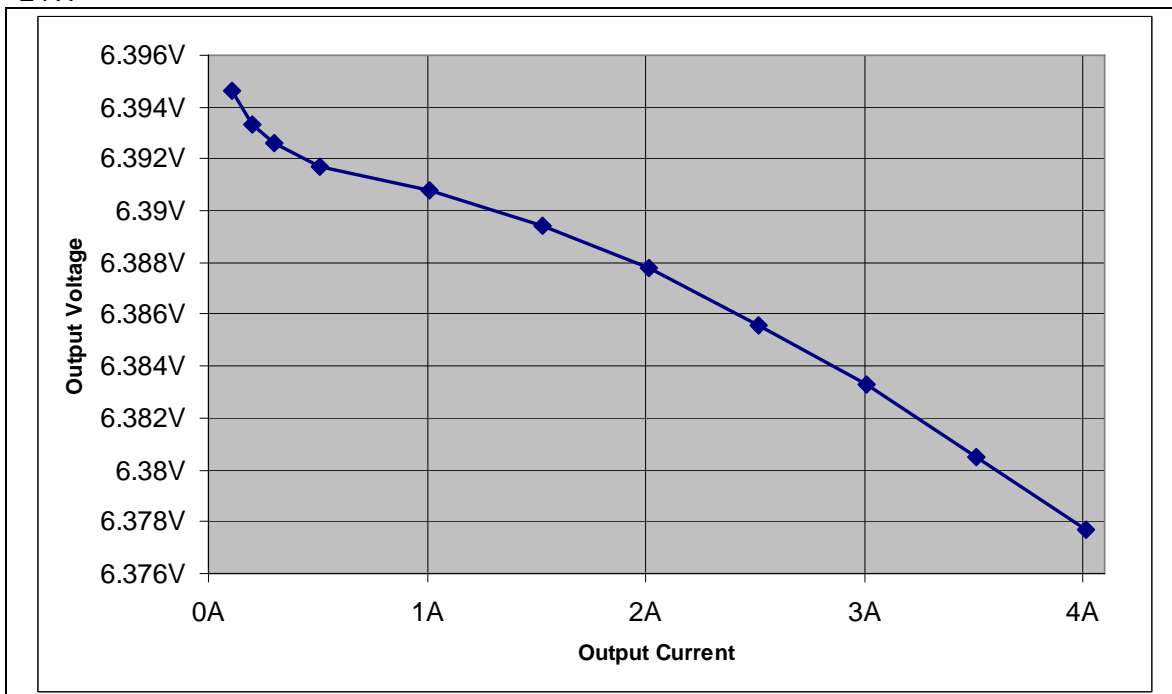


Figure 4

4. Line Regulation

The line regulation with 4A output current is shown in Figure 5.

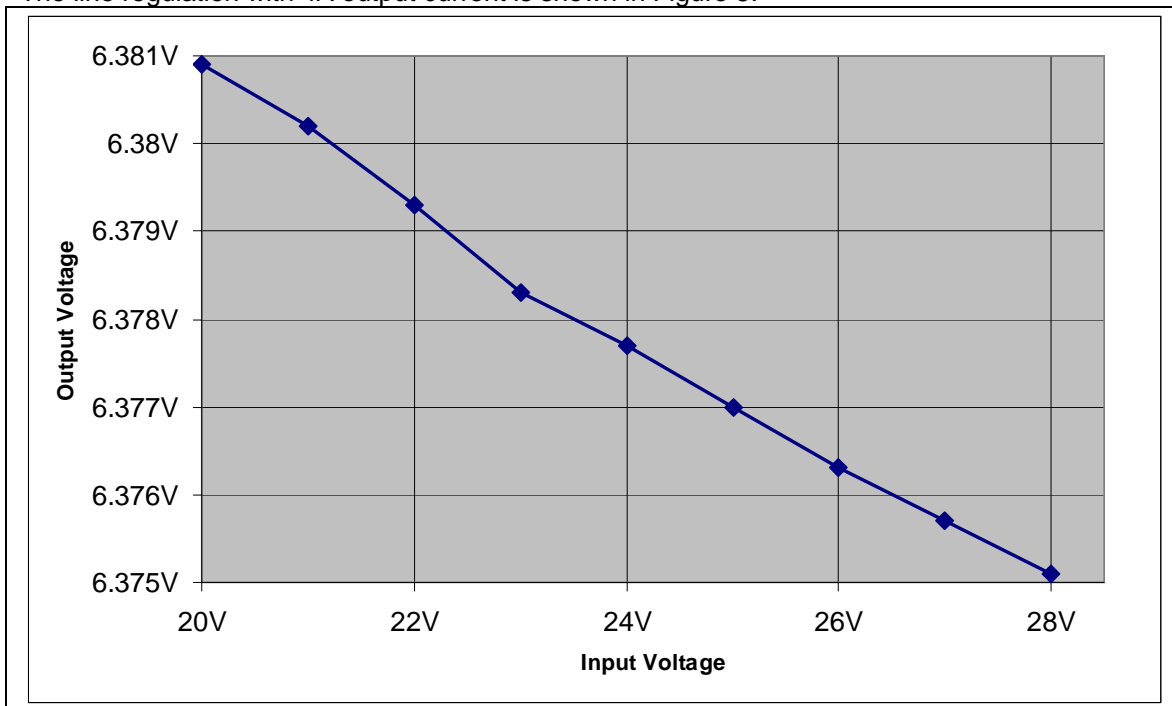


Figure 5

With the same measurement the corresponding efficiencies are shown in Figure 6.

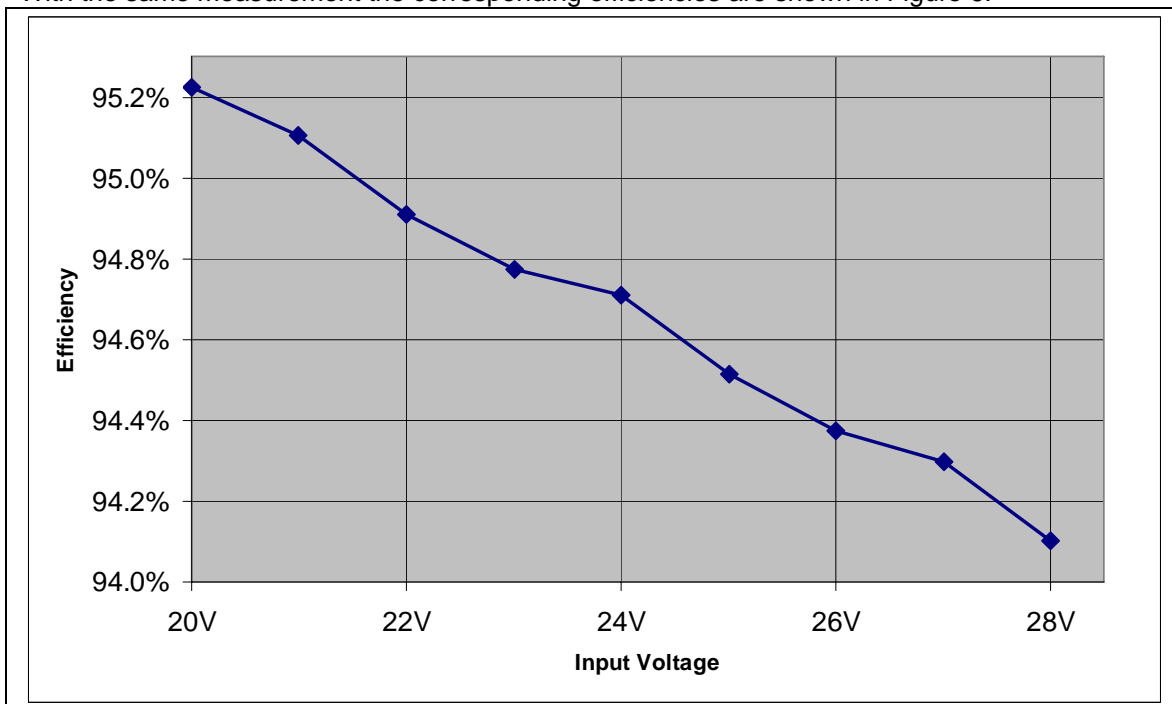
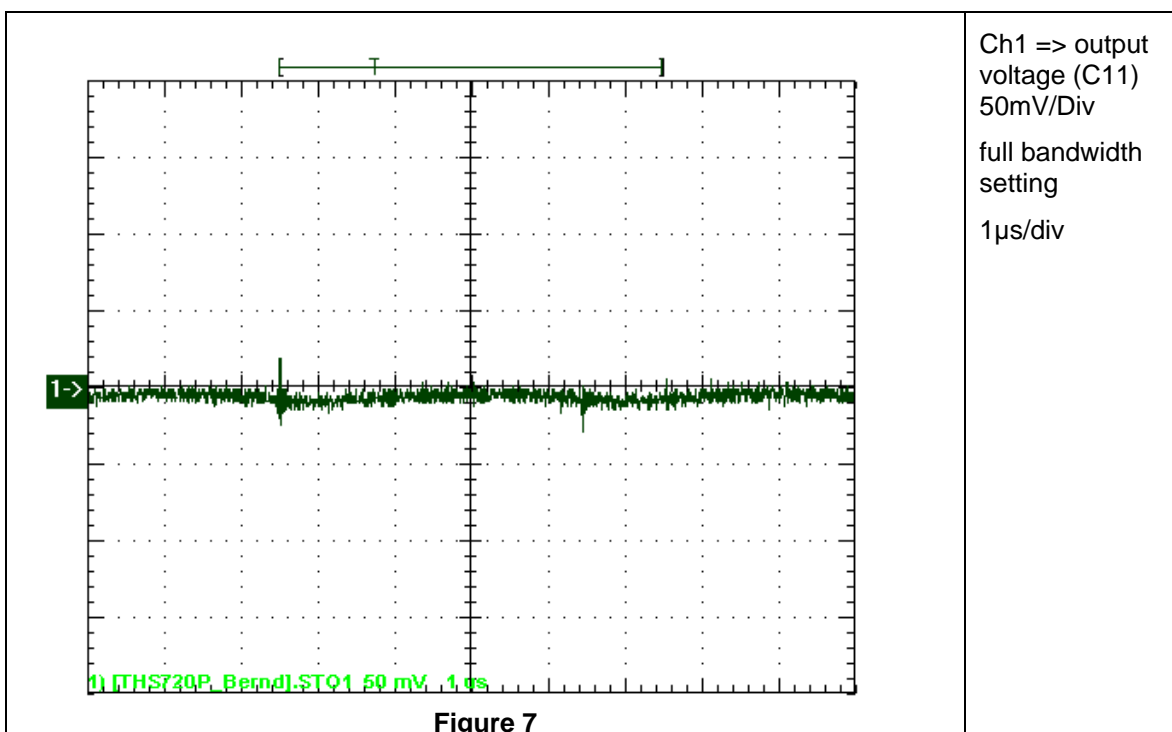


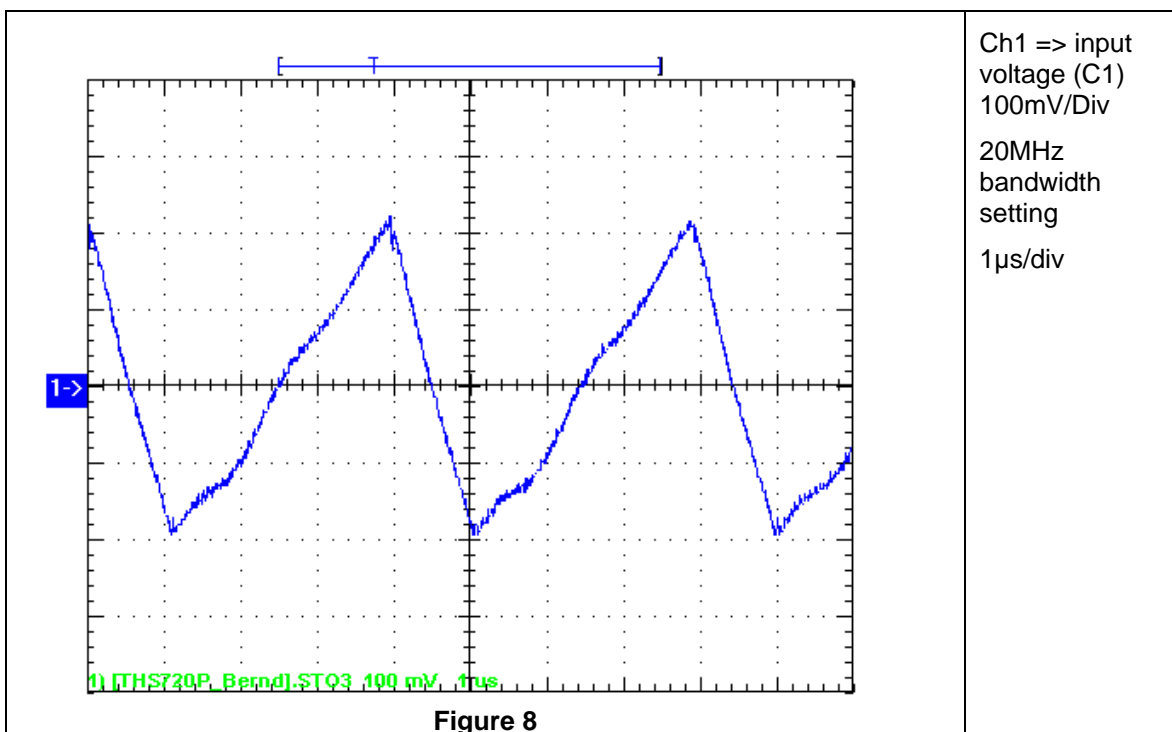
Figure 6

5. Ripple Voltage

The output ripple voltage is shown in Figure 7. The image was taken with a 4A load and 24V at the input.

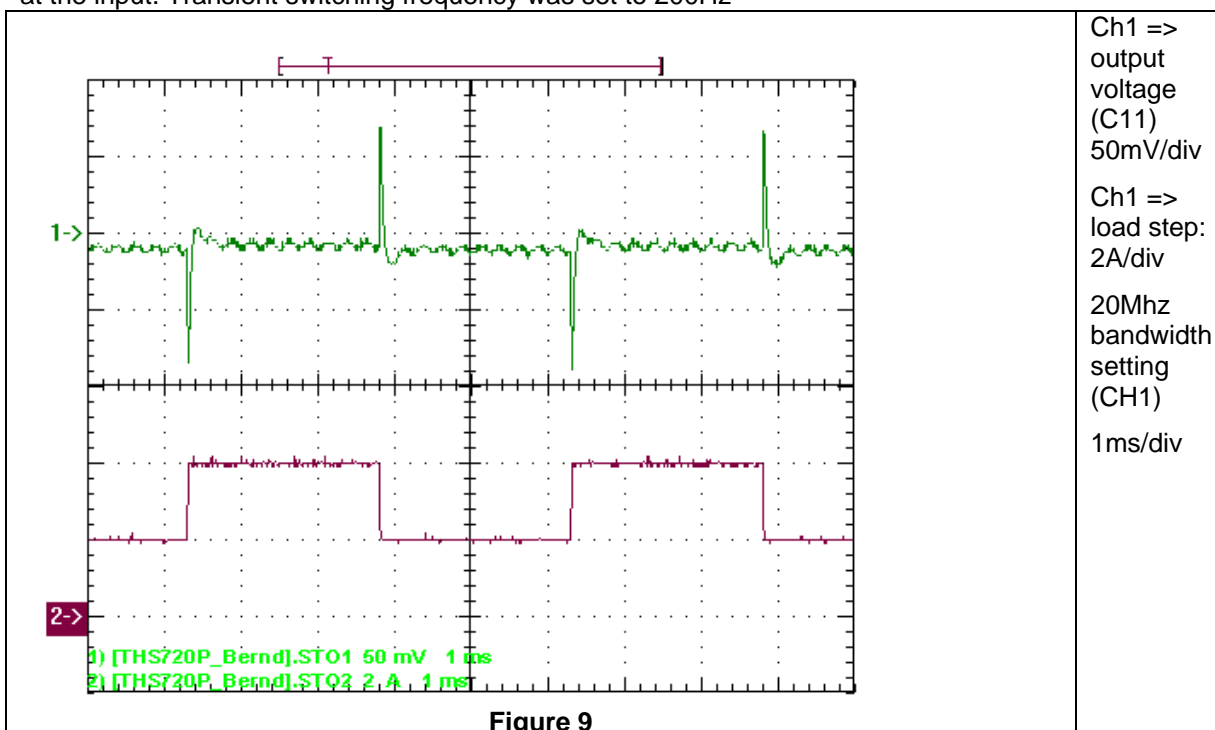


The input ripple voltage is shown in Figure 8. The image was taken with a 4A load and 24V at the input.

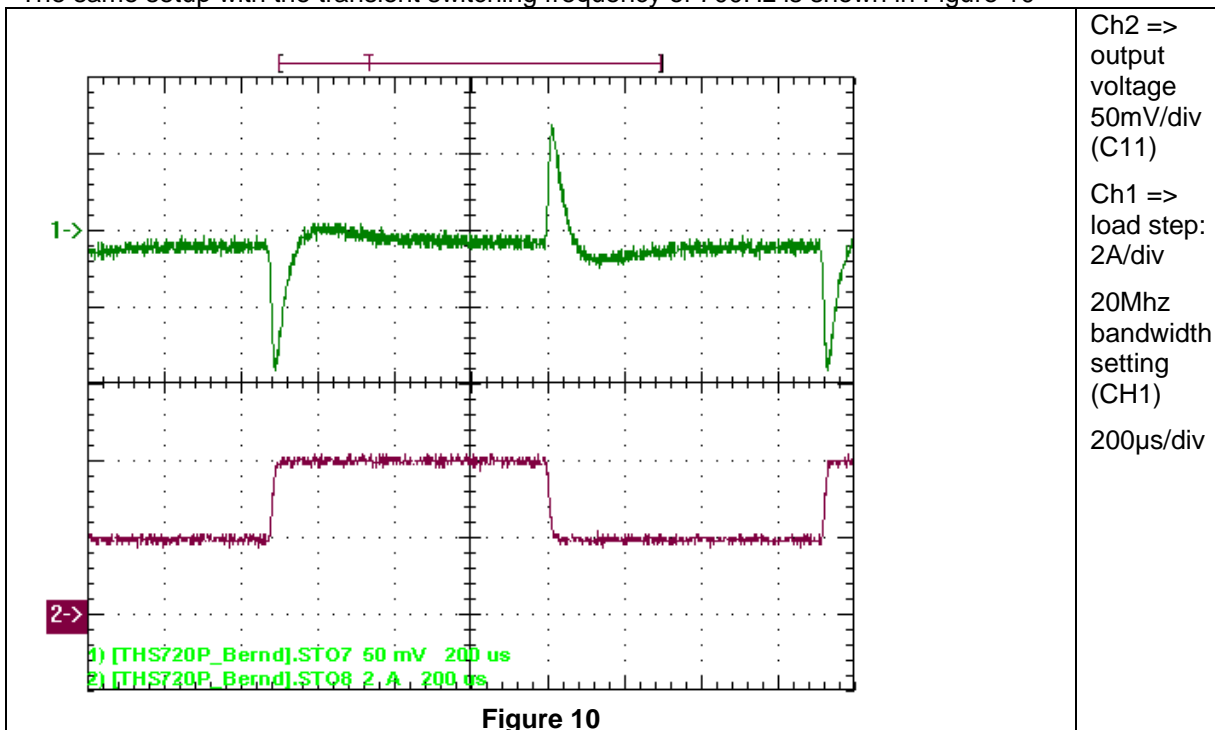


6. Load Transients

The Figure 9 shows the response to load transients. The load is switching from 2A to 4A with 24V at the input. Transient switching frequency was set to 200Hz



The same setup with the transient switching frequency of 700Hz is shown in Figure 10



7. Switch Node Waveform

With input voltage set to 24V result in the waveform shown in Figure 11 and Figure 12. Output current was set to 4A. Around 254kHz was the switching frequency.

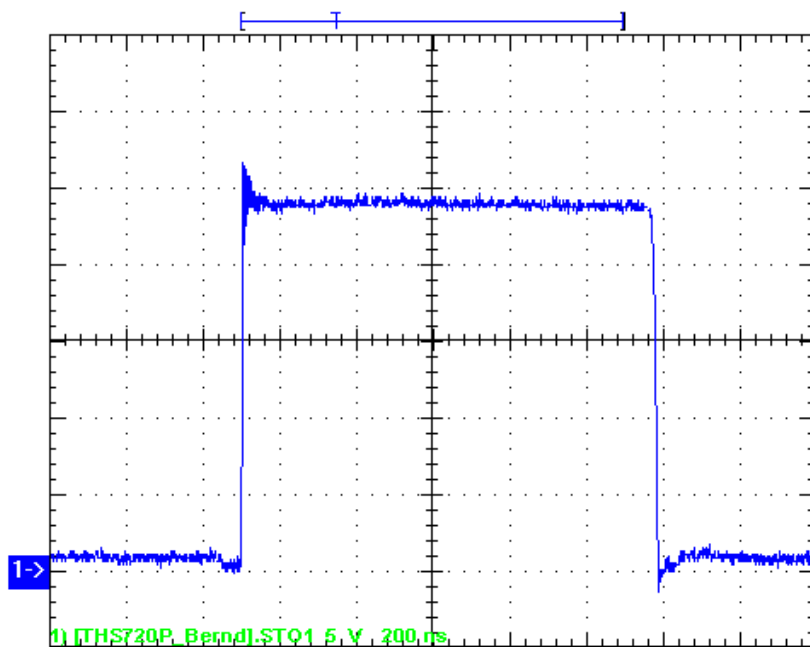


Figure 11

Ch1 =>
switch
node
5V/div
200ns/div
full
bandwidth

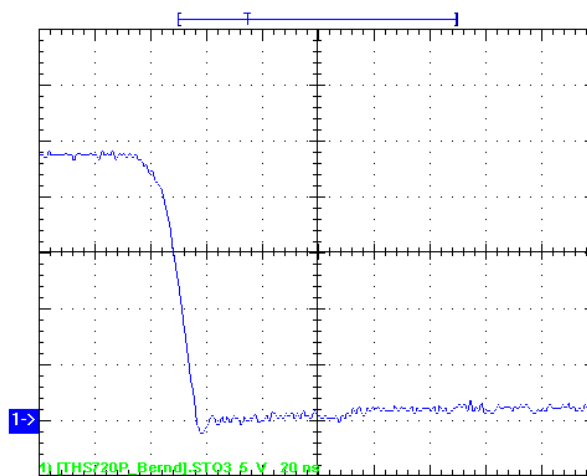
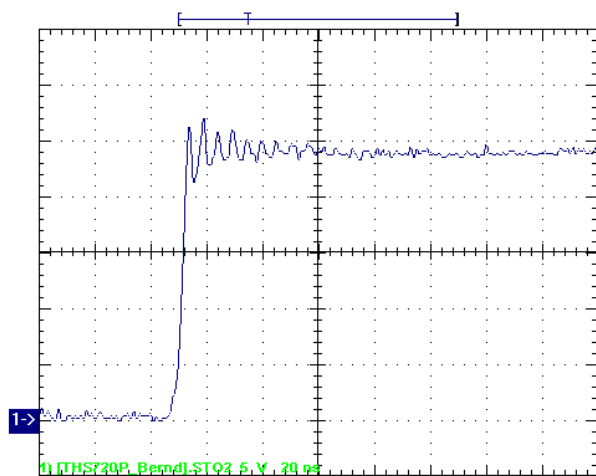


Figure 12

Ch1 =>
switchnode
5V/div
20ns/div
full
bandwidth

8. Control Loop Frequency Response

Figure 13 shows the control loop frequency response and in Table 1 are the corresponding values for gain and phase margin. The output current were set to 4A and input voltage to 24V. Please note the view of the phase is not symmetric.

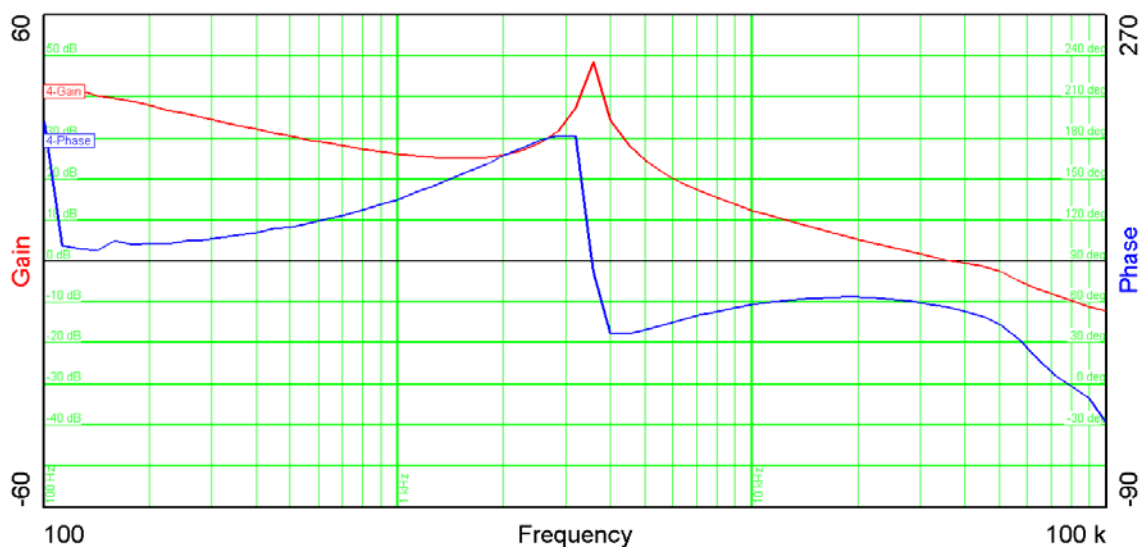


Figure 13

Bandwidth (kHz)	37
Phase margin	55°
slope (20dB/decade)	-0.927
gain margin (dB)	-9.4
at frequency (kHz)	78.4
slope (20dB/decade)	-1.38

Table 1

9. Thermal Image

The images were taken at 4A output current and 24V input voltage.

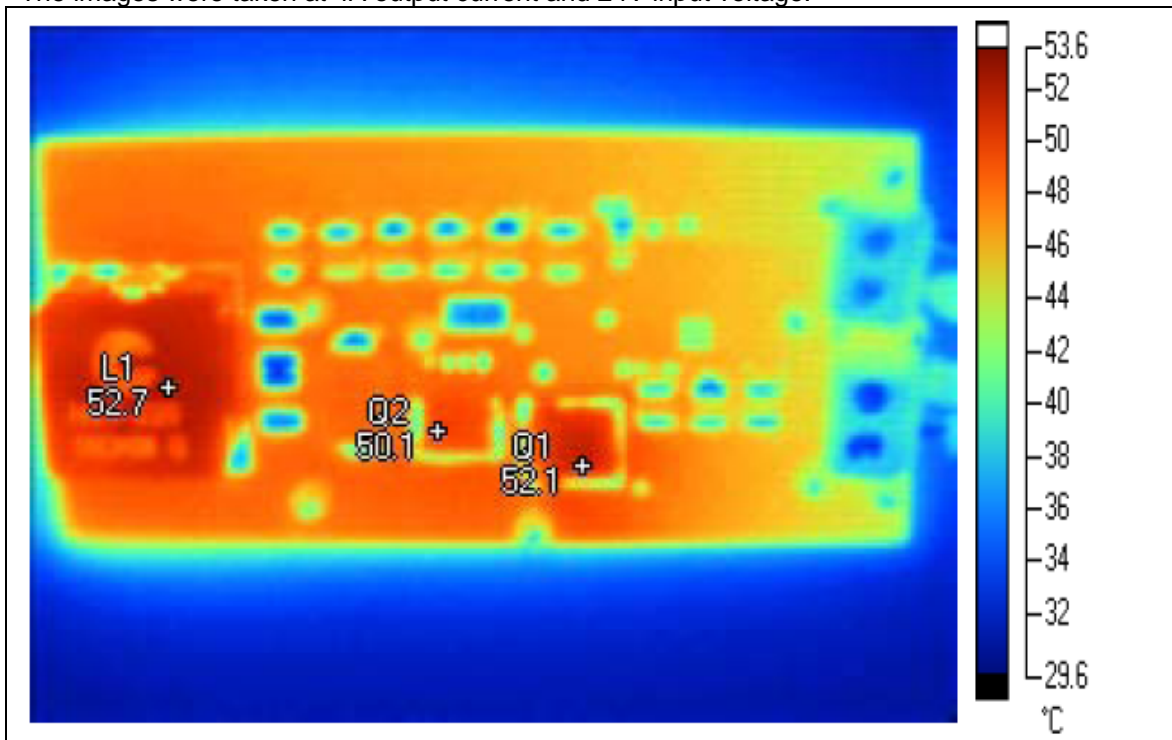
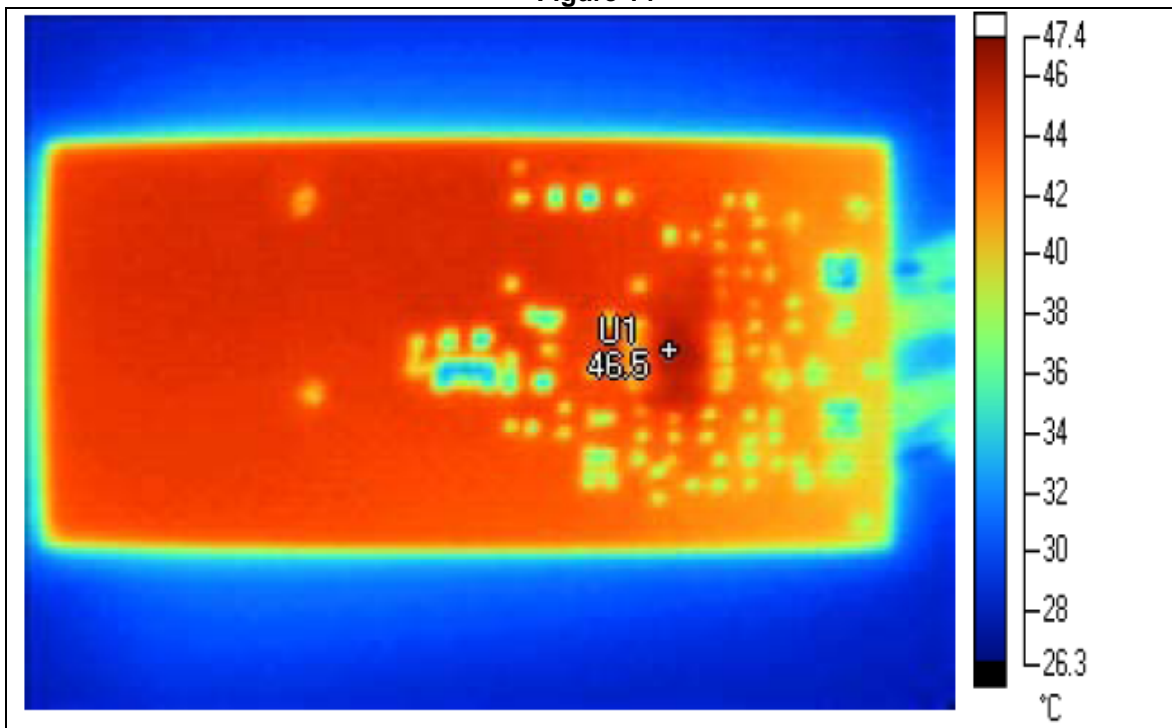


Figure 14



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For Feasibility Evaluation Only, in Laboratory/Development Environments. The reference design is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory / development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical / mechanical components, systems and subsystems. It should not be used as all or part of a production unit.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the reference design for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the reference design. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the reference design and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the REFERENCE DESIGN is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the reference design will not result in any property damage, injury or death, even if the REFERENCE DESIGN should fail to perform as described or expected.

Certain Instructions. Exceeding the specified reference design ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the reference design and/or interface electronics. Please consult the reference design User's Guide prior to connecting any load to the reference design output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output ranges are maintained at nominal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the reference design schematic. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the reference design that is not in accordance with the terms of this agreement. This obligation shall apply whether Claims arise under the law of tort or contract or any other legal theory, and even if the reference design fails to perform as described or expected.

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