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DESIGN GUIDE – STEP-BY-STEP DESIGN PROCEDURE

This example details the design of a high frequency switching regulator design using ceramic output capacitors. This design is available as the HPA375 evaluation module (EVM). A few parameters must be known in order to start the design process. These parameters are typically determined on the system level. For this example, we start with the following known parameters:

Output Voltage	1.8 V
Transient Response 1 to 2A load step	ΔVout = 5%
Maximum Output Current	4 A
Input Voltage	5 V nom. 3 V to 5 V
Output Voltage Ripple	< 30 mV p-p
Switching Frequency (Fsw)	1000 kHz

SELECTING THE SWITCHING FREQUENCY

The first step is to decide on a switching frequency for the regulator. Typically, you want to choose the highest switching frequency possible since this produces the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the converter's performance. The converter is capable of running from 300 kHz to 2 MHz. Unless a small solution size is an ultimate goal, a moderate switching frequency of 1MHz is selected to achieve both a small solution size and a high efficiency operation. Using Equation 9, R5 is calculated to be 180 kΩ. A standard 1% 182 kΩ value was chosen in the design.

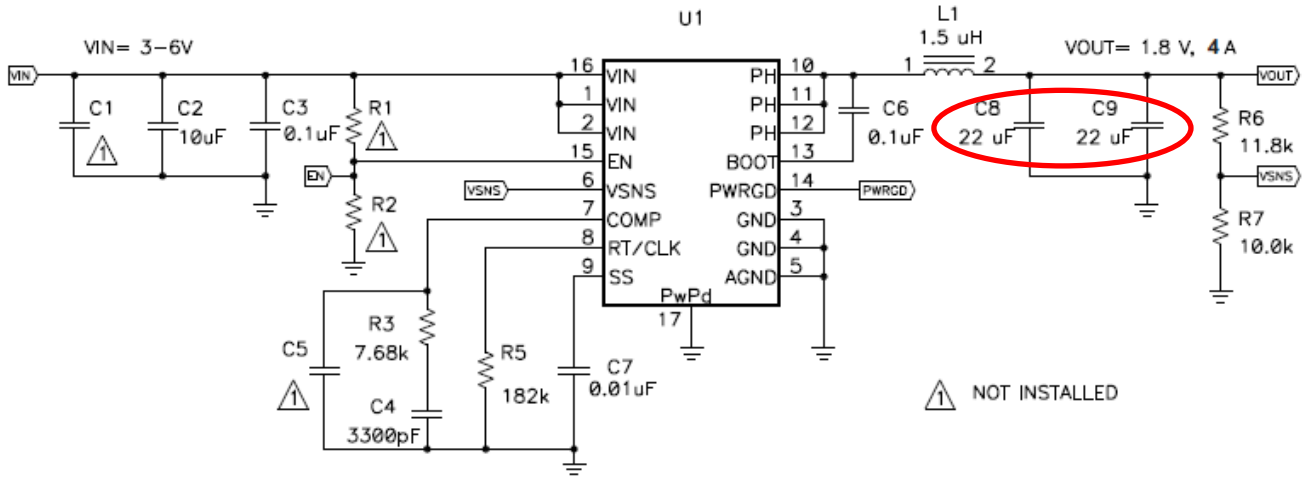

Figure 34. High Frequency, 1.8 V Output Power Supply Design with Adjusted UVLO

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COMPENSATION

There are several industry techniques used to compensate DC/DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS57114-Q1. Since the slope compensation is ignored, the actual cross over frequency is usually lower than the cross over frequency used in the calculations. Use SwitcherPro software for a more accurate design.

To get started, the modulator pole, fpmod, and the esr zero, fz1 must be calculated using Equation 36 and Equation 37. For Cout, derating the capacitor is not needed as the 1.8 V output is a small percentage of the 10 V capacitor rating. If the output is a high percentage of the capacitor rating, use the capacitor manufacturer information to derate the capacitor value. Use Equation 38 and Equation 39 to estimate a starting point for the crossover frequency, fc. For the example design, fpmod is 6.03 kHz and fzmod is 1210 kHz. Equation 38 is the geometric mean of the modulator pole and the esr zero and Equation 39 is the mean of modulator pole and the switching frequency. Equation 38 yields 85.3 kHz and Equation 39 gives 54.9 kHz. Use the lower value of Equation 38 or Equation 39 as the approximate crossover frequency. For this example, fc is 56 kHz. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole (if needed).

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \quad (36)$$

$$fz\ mod = \frac{1}{2\pi \times Resr \times Cout} \quad (37)$$

$$f_C = \sqrt{fp\ mod \times fz\ mod} \quad (38)$$

$$f_C = \sqrt{fp\ mod \times \frac{fsw}{2}} \quad (39)$$

Iout=4A、Vout=1.8V、Cout=44μF
Calculated taking into equation (36) is fp mod=8.03kHz.
Could you teach the reason why is not fp mod= 6.03kHz?