5.4.1.9 Analog MUX (AMUX)

Table 5-4 describes the selectable-analog internal signals on the DIAG_OUT terminal. In the DIAG_CFG_CTRL register, the MUX_CFG bits must be set to 10 for the analog MUX mode.

Table 5-4. Analog MUX Selection Table

SIGNAL NUMBER	VOLTAGE RAIL/ SIGNAL NAME	DESCRIPTION	DIVIDE RATIO	VOLTAGE RANGE / ACCURACY(1)	MAXIMUM OUTPUT RESISTANCE (kΩ)	DIAG_MUX_SEL[3:0]
A.1	VDD5	Linear VDD5 regulator output	2 ± 1.5%	2.5 V ±2%	55	0x01
A.2	VDD6	Switch-mode preregulator	3 ± 2.2%	2 V ±5%	140	0x02
A.3	VCP	External charge pump	13.5 ± 2%	0.6 to 4 V	1640	0x04
A.4	VSOUT1	Sensor-supply voltage	4 ± 0.5%	0.825 to 2.375 V	240	0x08
A.5	VBAT_SAFING	Safing battery supply	10 ± 2%	0.4 to 4 V	1755	0x10
A.6	VBAT	Battery supply	10 ± 2%	0.4 to 4 V	1755	0x20
A.7	MAIN_BG	Regulators bandgap reference	1	2.5 V ±2%	15	0x40
A.8	VMON_BG	Voltage-monitor band gap	1	2.5 V ±2%	15	0x80

(1) The given accuracies are without the DC load-current drawn from DIAG_OUT terminal. For overall accuracy calculation, the divide ratio accuracy and the drop voltage caused by $I_{\_DIAG\_-OUT}$ × Max. Output Resistance must be considered.

In case one of these analog signals comes to a voltage above VDDIO, a clamp becomes active to avoid any voltage level higher than VDDIO on the DIAG_OUT terminal.

In order to achieve the fastest stabilization of the signal switched to DIAG_OUT, following the AMUX switching order from A.1 up to A.8 is not recommended.

The recommendation is to switch the order from high to low voltage, starting with A.8. For example: A.8 - A.7 - A.1 - A.2 - A.3 - A.5 - A.6 - A.4.

NOTE

The sensor-supply output voltage (VSOUT1) is 0 V in this example. If VSOUT1 is higher, then the switching order described in the previous example must be changed. In the application, a series resistance of at least 100 kΩ is required on the input capacitor filter of the ADC input of the MCU.

5.4.1.10 Digital MUX (DMUX)

The following tables list the selectable digital internal signals on the DIAG_OUT terminal. In the DIAG_CFG_CTRL register, the MUX_CFG bits must be set to 01 for the digital MUX mode.

Most of these signals are internal error signals that influence the device state and behavior of the NRES terminal and the ENDRV terminal. See Table 5-2 for a more detailed table listing the internal error signals and their impact on the device behavior.