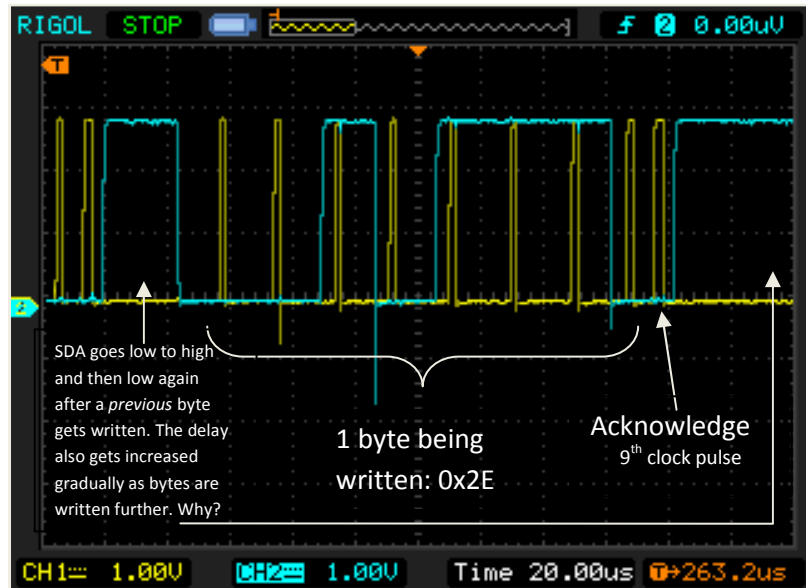
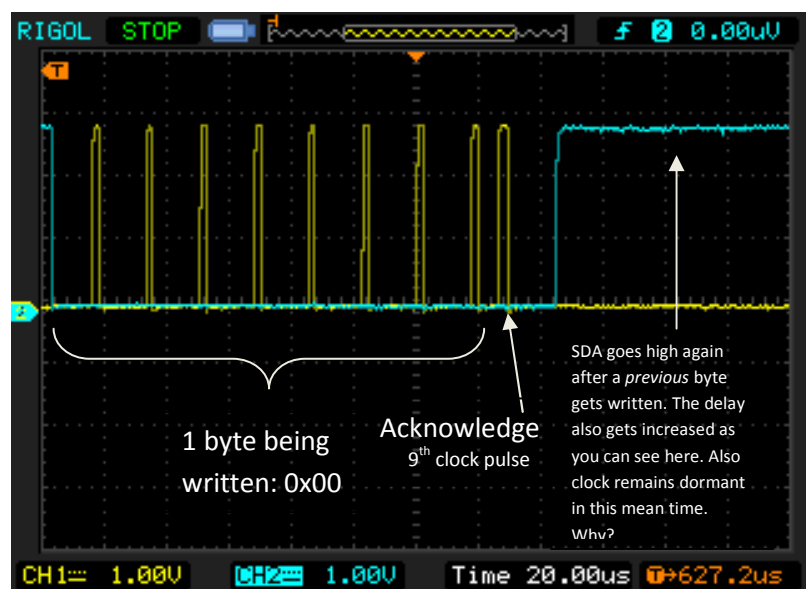


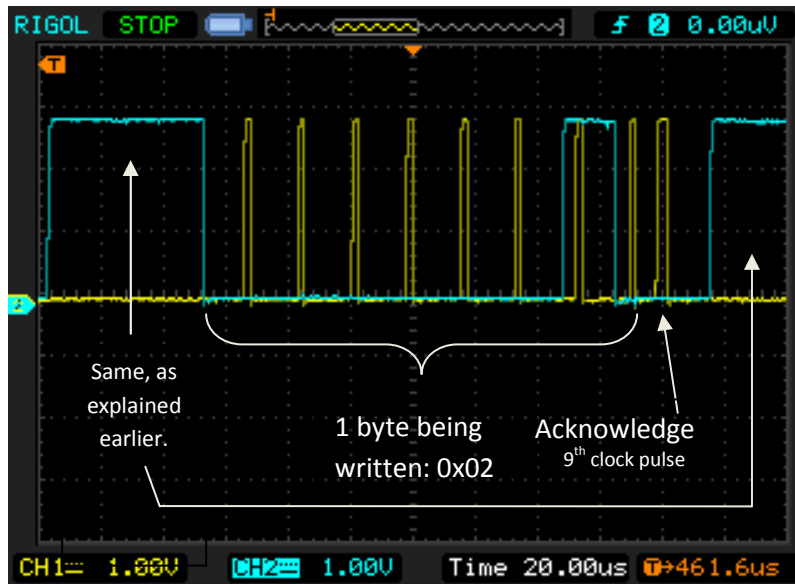
WRITE OPERATION:



Clipping 1: 1 byte waveform
extracted out of 640 bytes



Clipping 2: 1 byte waveform
extracted out of 640 bytes



Clipping 3: 1 byte waveform
extracted out of 640 bytes

Since bytes being written was in a large set: (128 user bytes + 512 bytes of configuration), I clipped several waveforms for a better understanding of the behaviour of SDA and SCL. Observing these waveforms, can you conclude that the bytes were being written properly seeing the acknowledgment being received?

Also, is there any condition for last byte to be written?

READ OPERATION:

In read operation, we are receiving 0xFF, 0x7F randomly. What does it concludes? Is there some delay issue or there needs to be a reordering in the i2c commands with some added delay? A function for checking the device ID from location 0x27 is given as below (Second Byte is read for device ID):

```
unsigned char Check()
{
    unsigned char Value=0x00;    //Initialization

    i2c_start();

    i2c_write(0xC0); //Device Address

    i2c_write(0x27); //Register Address

    i2c_start();           //Repeated Start

    i2c_write(0xC1); //Read bit is enabled

    i2c_read(TRUE);        //First Byte is read

    Value=i2c_read(FALSE); //Second Byte is read and saved

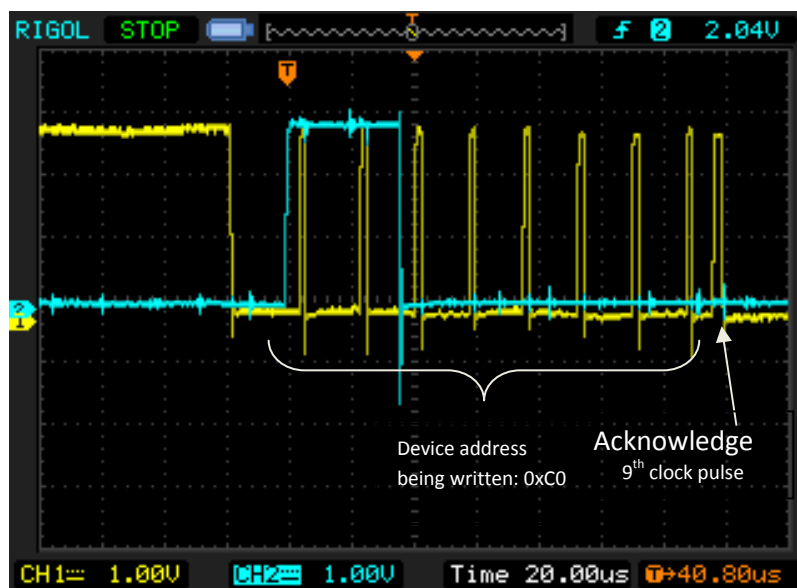
    i2c_stop();

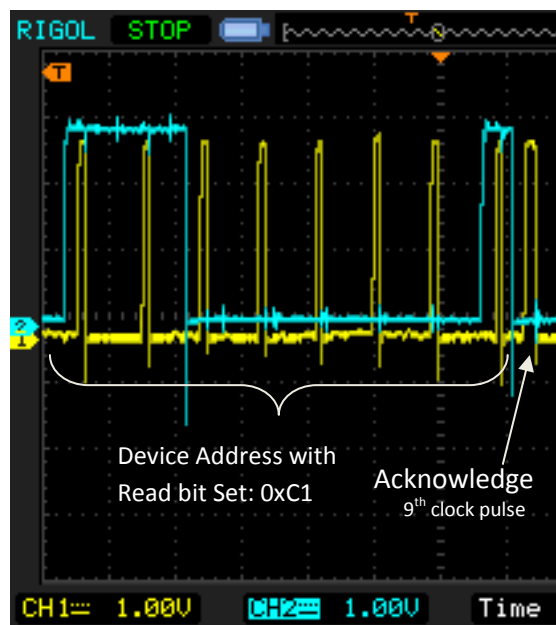
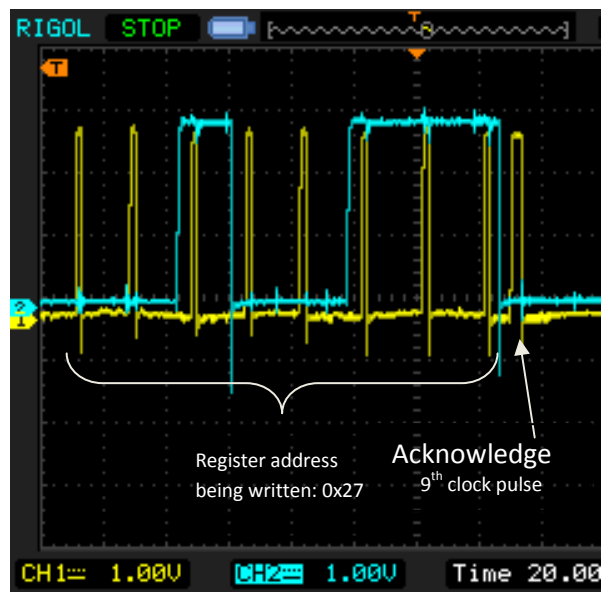
    return Value;           //Return the second byte value
}
```

We receive the Value as 0xFF / 0x7F.

The waveforms as observed in the read operation are given as below. They occur in an **order**:

Please help me identify the **i2c_start** condition.





Please help me verify the 9th clock pulse after i2c_read in (1) and (2). Are they correct as per the code?

