Using DAC NCO to solve LO fractional spur problem

Decapton Wang

ABSTRACT

High speed Digital-to-Analog Converter (DAC) and Local Oscillator (LO) products are widely used in wireless communication applications. In a typical transmitter, the modulator mixes IF product and LO product to generate RF output. Usually, the LO works under fractional mode to realize various frequency plans flexibly. However, LO under such mode have fractional spur and integer boundary spur problems. Such spurs may deteriorate EVM and ACPR at modulator output. Although there are some ways like dither that can suppress fractional spur and integer boundary spur, such ways sacrifice LO phase noise performance. So it is hard for designers to optimize both phase noise and spur performance at the same time. This application note introduces a method that uses NCO in high speed DAC to compensate fractional part of LO frequency. With this method, LO can work under integer mode and designers can focus only on optimizing LO phase noise without caring about the spur problem. And therefore both spur and phase noise problems in fractional LO can be solved.

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1 Definition

IBS: Integer boundary spur

EVM: Error vector Magnitude or Evaluation Module, depending on the context.

NCO: Numerical controlled oscillator

LO: Local oscillator

TX: Transmitter

2 Spur problem in fractional PLL

Figure 1 shows a typical fractional PLL structure. The output frequency can be derived as

$$f_{PFD} = f_{REF} / R$$
$$f_{LO} = f_{PFD} * (N + \frac{DEN}{NUM}) \quad (1)$$

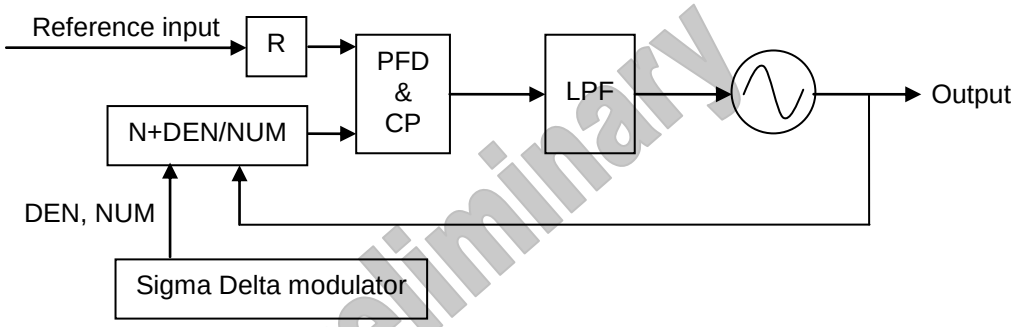

Figure 1. Typical fractional PLL structure

PLL under fractional mode will generate two kinds of spurs, fractional spur and integer boundary spur. The fractional spurs locate at

$$f_{fractional\_spur} = \frac{f_{PFD} * k}{NUM}, k = 1,2,... \quad (2)$$

The integer boundary spur (IBS) locates at

$$f_{integer\_boundary\_spur} = \frac{f_{PFD} * DEN}{NUM} \quad (3)$$

According to equation (2) and (3), the IBS belongs to fractional spur. But there is difference between the two. The fractional spur can be suppressed by dither while the IBS can not, as Figure 2 shows. Usually, designers need to adjust PFD frequency to suppress IBS. An experience is making the fractional-N part (DEN/NUM) as close as 0.5. Figure 3 shows integer boundary spurs under different PFD frequencies.

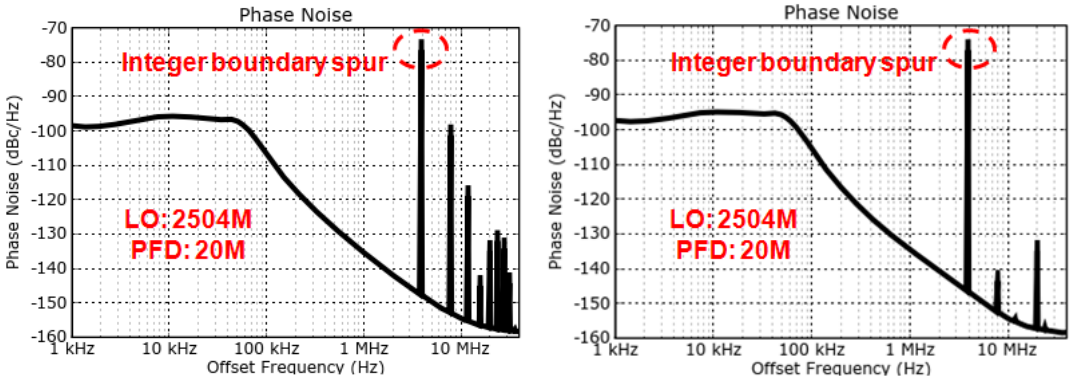

Figure 2. Fractional spurs under PLL without/with dither

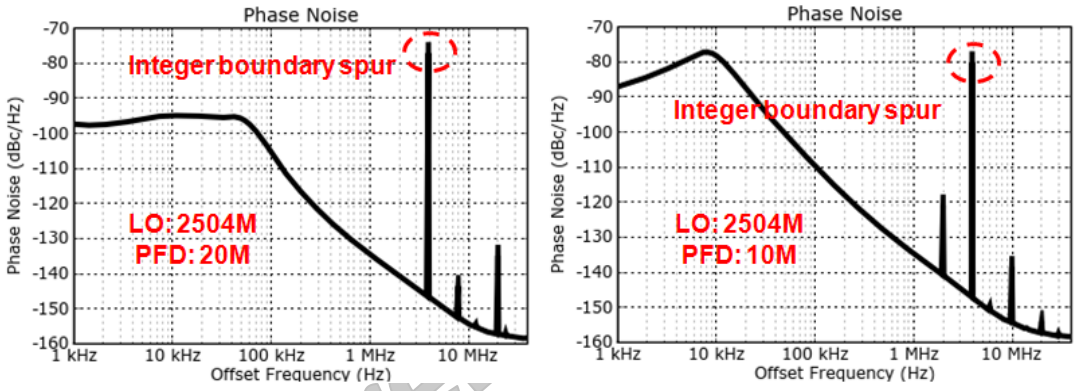

Figure 3. Integer boundary spurs under different PFD frequencies

Fractional spur can deteriorate system EVM and ACPR. In wideband application, it may generate in-band product and harm EVM and ACPR. In narrow band application, it may generate close-in product and harm ACPR. Figure 4 shows the influence of fractional spur. Figure 5 provides an actual WCDMA single carrier test result to show how ACPR in modulator output is degraded by LO fractional spur.

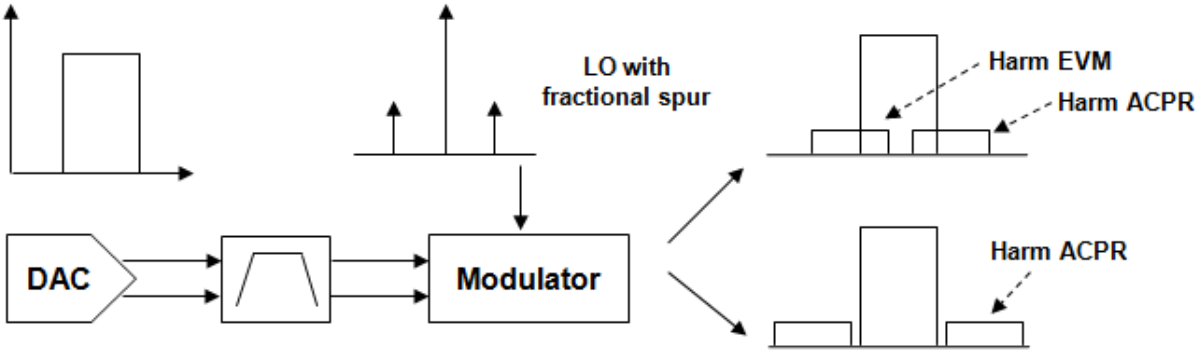

Figure 4. Influence of integer boundary spur

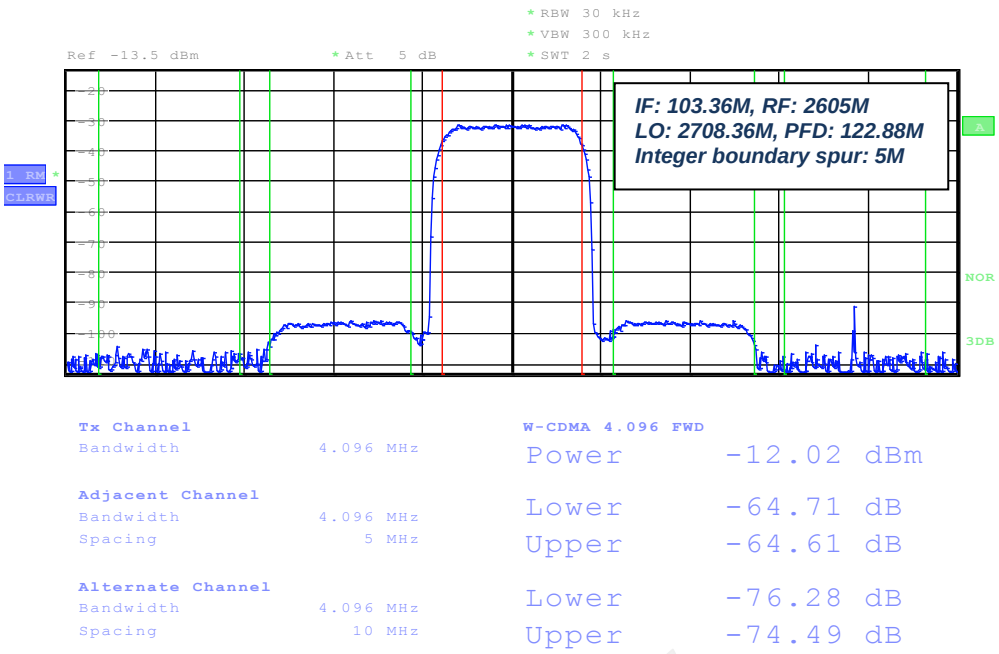

Figure 5. ACPR degradation caused by integer boundary spur

Traditionally, designers use two ways to suppress fractional spurs. For the non-IBS, it can be suppressed by dither, as Figure 2 shows. But dither introduces new phase noise especially at close-in region. Take Figure 2 as an example, the close-in phase noise (within 100KHz offset) is increased about 1~2dB by dither. For the IBS, it can be suppressed by adjusting PFD frequency and making the product of NUM/DEM as close as 0.5. However, such way has the probability to decrease PLL loop bandwidth and then cause VCO phase noise pushes into close-in region. Therefore, the LO output close-in phase noise increases, as the left side of Figure 3 shows.

According to the above analysis, it is hard for a fractional PLL to provide both good phase noise and spur performance at the same time. A method is needed to solve fractional spur problem without sacrificing phase noise performance.

3 Using DAC NCO to compensate fractional part of LO frequency

In this section, a method using DAC NCO is introduced to solve fractional spur problem. First of all, the LO frequency can be written as

$$f_{LO} = f_{LO\_fractional} + f_{LO\_integer} \tag{4}$$

All the fractional spurs are from LO fractional part. If the fractional part can combine with IF, the LO will work under integer mode without fractional spur problem, as equation (5) shows. The problems are whether there is hardware resource to realize it in TX path and whether such hardware introduces higher spurious products compared to those in fractional LO.

$$f_{IF} = f_{IF\_initial} + f_{LO\_fractional} \tag{5}$$

In TX, the Numerical Controlled Oscillator (NCO) can realize frequency transform. There are two NCOs in TX. The first one is FPGA, and the other one is DAC. This note focuses on DAC NCO and illustrates how to use DAC NCO to solve fractional LO spur problem.

An NCO is used to generate sine and/or cosine wave in digital domain. It consists from frequency and phase registers, phase accumulator (PA), dither generator and phase-amplitude converter (PAC), as Figure 6 shows [1] [2]. Equation (6) derives the NCO transfer function. The T_S and f_S are period and frequency of NCO operating clock. f_{NCO} is the target frequency. Φ_{OFFSET} and Φ_{DITHER} are optional phase offset and phase dither, separately.

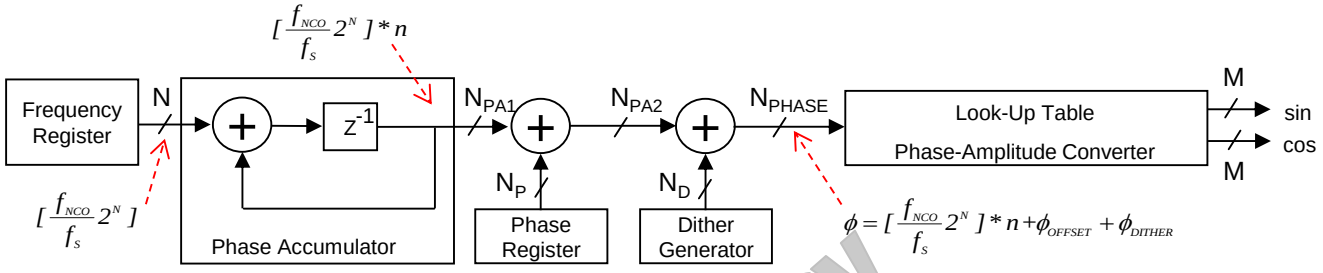

Figure 6. Typical NCO structure

$$y_{NCO} = \sin 2\pi*(nTs*f_{NCO}+\phi) = \sin 2\pi*(n*\frac{f_{NCO}}{f_S}+\phi_{OFFSET}+\phi_{DITHER}) \quad (6)$$

To initiate NCO, users need to transform the target frequency to frequency word and then write it to frequency register. In digital domain, the target frequency should be normalized to f_{NCO}/f_S and then be quantized to N bit. So the frequency word can be written as

$$Freq\_word = [\frac{f_{NCO}}{f_S}2^N] \quad (7)$$

The symbol "[ ]" means rounding the number to its nearest integer number. The integer frequency word enters PA and accumulates to an inter-mediate phase.

$$N_{PA1} = [\frac{f_{NCO}}{f_S}2^N]*n, \quad n=1,2,3... \quad (8)$$

Usually, there are optional phase offset and phase dither in NCO, and the final phase can be derived as

$$N_{PHASE} = [\frac{f_{NCO}}{f_S}2^N]*n+\phi_{OFFSET}+\phi_{DITHER}, \quad n=1,2,3... \quad (9)$$

The final phase information is sent to PAC. The PAC is a look-up table that can translate phase information to amplitude. And after this step, users can get digital sine and/or cosine wave as equation (5) shows.

The NCO accuracy is measured in two parts, frequency resolution and spur. The relative frequency resolution is 1/2^N, and the absolute frequency resolution is f_S/2^N. Take DAC34SH84 as an example, its N is 32. When f_S is 1.5GHz, the absolute frequency resolution is 0.35Hz (1.5G/2^32). This resolution is so small that it can meet most of wireless infrastructure applications' need.

The NCO spur is introduced by truncation operations. For saving hardware resource, there are phase truncation and amplitude truncation in NCO. The phase truncation occurs in phase forming path. The N_{PA1}, N_{PA2} and N_{PHASE} are all truncation products of their previous stages. The amplitude truncation occurs in PAC, and it is introduced by the truncated PAC output. The truncation operations, whatever phase or amplitude, introduce spurious products [2]. Without dither, the truncation spur level can be estimated as the larger one between -6N_{PHASE} and -6M [3]. For further improving NCO spur performance, dither is usually used. Dither is a series of pseudo-random numbers. In spectrum, it can be treated as wide band white noise. Added to the PAC input, it can randomize the truncation error from N_{PA1} to N_{PHASE}. So the truncation spur can be split to noise floor, and then the SFDR performance improves [1][2].

In the modern state-of-art DAC designs, dither is usually removed for saving more hardware resource and getting lower noise floor. Then the NCO spur performance is dominated by N_{PHASE} and M. Take DAC34SH84 as an example, N_{PHASE} and M are all 16. After optimization, its NCO spur level can be smaller than -90dBc. Compared to LO fractional spurs, the NCO spur is much lower, so it can be used to compensate LO fractional part without introducing larger spurs.

In application, designers also need to note that the NCO in DAC can realize complex up-conversion but cannot realize real up-conversion. Figure 7 shows the detailed complex TX path. The NCO discussed above is used in complex digital mixer in DAC, as equation (10) and (11) show. If using real up-conversion, designer needs to use NCO in FPGA rather than DAC.

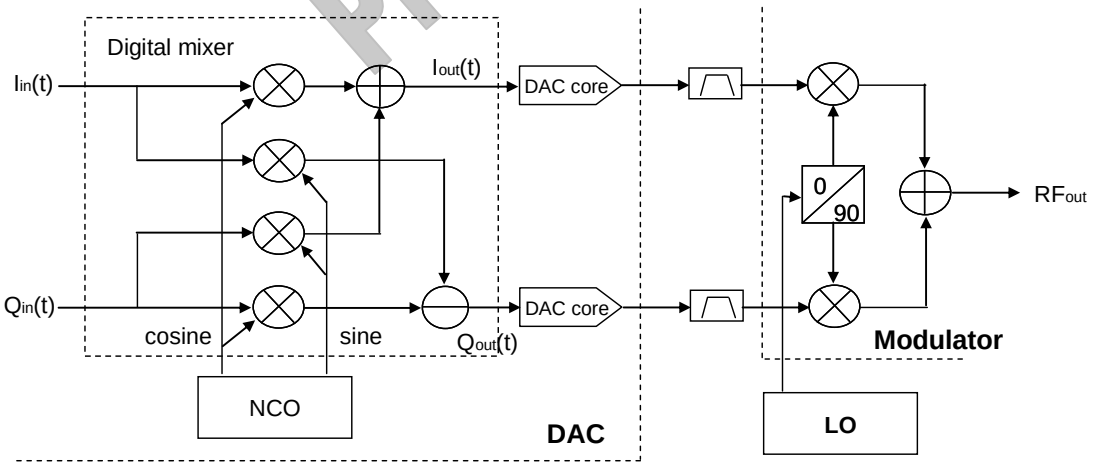

Figure 7. Typical complex TX path

$$I_{OUT} = I_{in} \cos \omega_{IF} + j Q_{in} \sin \omega_{IF}$$
$$Q_{OUT} = -I_{in} \sin \omega_{IF} + j Q_{in} \cos \omega_{IF} \quad (10)$$

$$RF_{out} = I_{out} * \cos\omega_{RF} + Q_{out} * \sin\omega_{RF} = I_{in} * \cos(\omega_{IF} + \omega_{RF}) + \mathrm{j}Q_{in} * \cos(\omega_{IF} + \omega_{RF}) \quad (11)$$

4 Application examples

This section introduces an application example to show to how to use DAC NCO to compensate LO fractional part. The test-bench consists from TSW1400 EVM, TSW30SH84 EVM and an LO source, as Figure 8 shows [4][5][6]. Detailed EVM information is listed in table 1.

Table 1. Detailed EVM information used in this work

Part number	Information
TSW30SH84 EVM	Complete RF signal chain evaluation module including DAC34SH84 and TRF3705
LMX2581 EVM	Evaluation module for wideband frequency synthesizer with integrated VCO
TSW1400 EVM	High Speed Data Capture and Pattern Generation Platform

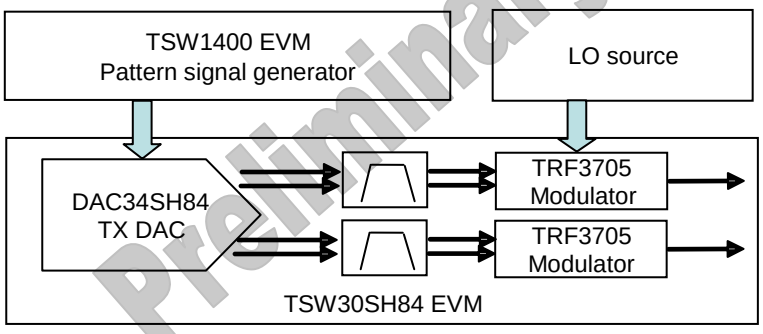

Figure 8. Test-bench used in this work

Below steps illustrate the detailed compensation process.

1. The initial frequency plan is listed in the upper side of table 2. The dominant fractional spur is IBS that lies at 5MHz offset of LO and causes ACPR degradation. For cancelling the IBS, LO should work under integer mode, and its frequency should change to 2703.36M. Therefore IF changes to 98.36M, as the bottom side of table 2 shows.

Table 2. Frequency plans for fractional LO and integer LO

Fractional LO frequency plan					
DAC clock, MSPS	IF, MHz	RF, MHz	LO, MHz	PFD, MHz	Dominant fractional spur, MHz offset
1228.8	103.36	2605	2708.36	122.88	5
Integer LO frequency plan					
DAC clock, MSPS	IF, MHz	RF, MHz	LO, MHz	PFD, MHz	Dominant fractional spur, MHz offset
1228.8	98.36	2605	2703.36	122.88	No fractional spur

2. Suppose the IF from FPGA to DAC is zero, then all the frequency up-conversion is done in DAC. The NCO frequency word length of DAC34SH84 is 32 bit. f_{NCO} equals to 98.36M. According to equation (6), the frequency word is

$$Freq\_word = [\frac{f_{NCO}}{f_{DAC}} 2^N] = [\frac{98.36}{1228.8} 2^{32}] = 343793118 \quad (12)$$

Change the decimal value to hex and write it into DAC34SH84

$$(343793118)_2 = (147\,\mathrm{DDDDE})_{16} \quad (13)$$

3. Set the LO frequency to 2703.36M.

4. Send single carrier WCDMA pattern signal and four carrier WCDMA pattern signal from FPGA (TSW1400) to DAC (DAC34SH84), and capture the modulator (TRF3705) output.

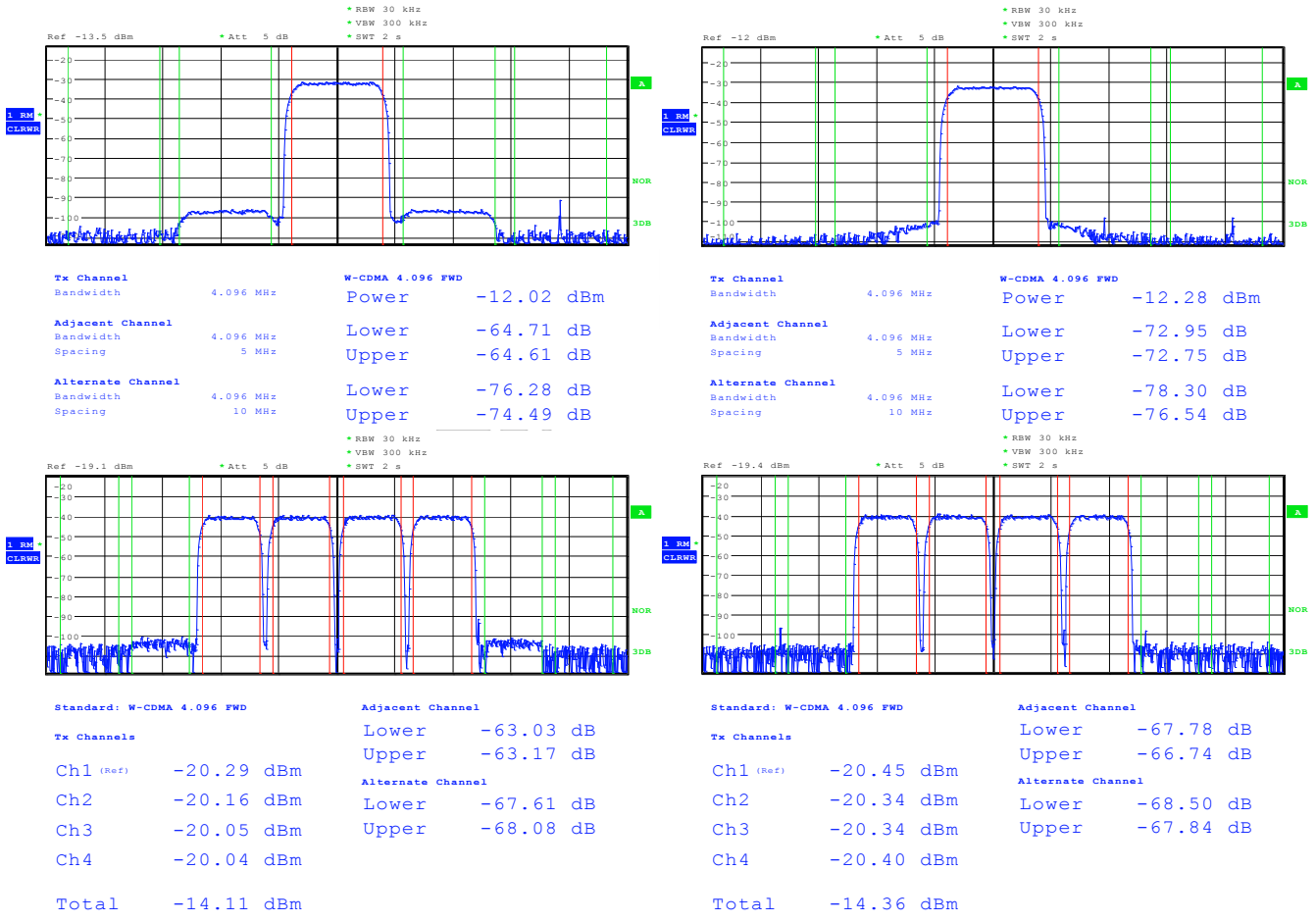

Figure 9. WCDMA pattern signal ACPR test results

Table 3. WCDMA pattern signal ACPR test summary

	Fractional LO	Integer LO
Single carrier ACPR (adjacent channel, dBc)	-64.61	-72.75
Four carrier ACPR (adjacent channel, dBc)	-63.03	-66.74

According to Table 3, the adjacent channel power suppression improves after using DAC NCO to compensate LO fractional part. Designers can also use similar steps in application.

5 Conclusion

This application notes discusses the influence of LO fractional spur on TX and how to use DAC NCO to cancel it. The fractional spur deteriorates TX EVM and ACPR. It can be suppressed with the sacrifice of increasing LO phase noise. The NCO is introduced to solve this problem. According to analysis and test results, the spur level of NCO is much lower than that of fractional LO. It can be used to compensate LO fractional part without introducing higher spurious product. Designers can use this method to make the LO work under integer mode and focus only on optimizing LO phase noise performance.

References

1. *GC5316 datasheet. Texas Instruments Inc., 2004 (SLWS154A)*
2. *Analysis of Fixed-Point Numerically Controlled Oscillator, MathWorks*
3. *The NCO as a Stable, Accurate Synthesizer, Intersil, 1998 (TB318.1)*
4. *DAC34SH84 datasheet, Texas Instruments Inc., 2012 (SLAS808D)*
5. *TSW30SH84 EVM User's Guide, Texas Instruments Inc., 2012* (SLAU433)
6. *TSW140x High Speed Data Capture/Pattern Generator Card, Texas Instruments Inc., 2012* (SLWU079A)