Operational Amplifier Stability
Part 10 of 15: Capacitor Loop Stability: Riso with Dual Feedback

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Part 10 of this series is the sixth and final verse of our familiar electrical engineering tune, *"There must be six ways to leave your capacitive load stable."* The six ways are Riso, High Gain & CF, Noise Gain, Noise Gain & CF, Output Pin Compensation, and, what we cover here: Riso w/Dual Feedback.

This topology is very often used to buffer a precision reference integrated circuit. As a voltage buffer, the op amp circuit provides higher source and sink currents than can be originally driven from the precision reference. Although we will look specifically at the gain of one, voltage follower configuration, the Riso w/Dual Feedback can be used with gains greater than one with slight modifications to the formulae provided. We will look at the two dominant types of op amp topologies, bipolar emitter-follower and CMOS RRO. The analytical and synthesis steps and techniques will be similar, but there are subtle differences -- enough to warrant looking at each respective output topology. As an added bonus we will purposely violate our rule-of-thumb guide and create the BIG NOT to see the effects of improper stability compensation.

From our stability analysis tool kit the Riso w/Dual Feedback technique will be presented by first-order analysis, confirmed through TINA-TI (a fully functional SPICE program loaded with TI models) loop stability simulation, checked by the Vout/Vin ac transfer function analysis in TINA-TI, and finally sanity-checked by the Transient Real World Stability Test run in TINA-TI. This Cload stability technique has been confirmed to work as predicted in real-world, actually-built circuits at some time over the last 25 years. However, due to resource limitations, each circuit specifically presented here has not been built, but rather is left to the reader as an exercise or the application of each technique to his/her own individual application (ie analyze, synthesize, simulate, build and test).

Bipolar Emitter-Follower: Riso w/Dual Feedback

The bipolar emitter-follower we will choose to analyze the Riso w/Dual Feedback technique is the OPA177, as detailed in Fig. 10.1. The OPA177 is a low drift, low input offset voltage op amp capable of being powered from ±3 V to ±15 V.

OPA177 **Precision Operational Amplifier**	
Parameter	**Specification**
Supply Voltage	+/-3V to +/-15V
Quiescent Current	1.3mA typical
Offset Voltage	10uV typical
Offset Drift	0.1uV/C typical
Input Bias Current	+/-0.5nA typical
Input Voltage Noise	85nVrms (1Hz to 100Hz)
Input Voltage Range	(V-)+2V to (V+)-2V
Gain-Bandwidth Product	600kHz
Open Loop Gain	140dB
Open Loop Output Resistance	60 ohms
Slew Rate	0.3V/us
Voltage Output Swing from Rail	2V typical (RL=2k)
Package	DIP-8, SO-8

Fig. 10.1: Bipolar Emitter-Follower Op Amp Specifications

Note that in a typical bipolar emitter-follower topology (see Fig. 10.2) both the positive and negative output drives to Vo are bipolar emitter-followers. Very few op amp data sheets today include *equivalent schematics* that would tell us the topology of the output stage used inside of the op amp. As such it is only through *factory only* information that we are assured of the topology.

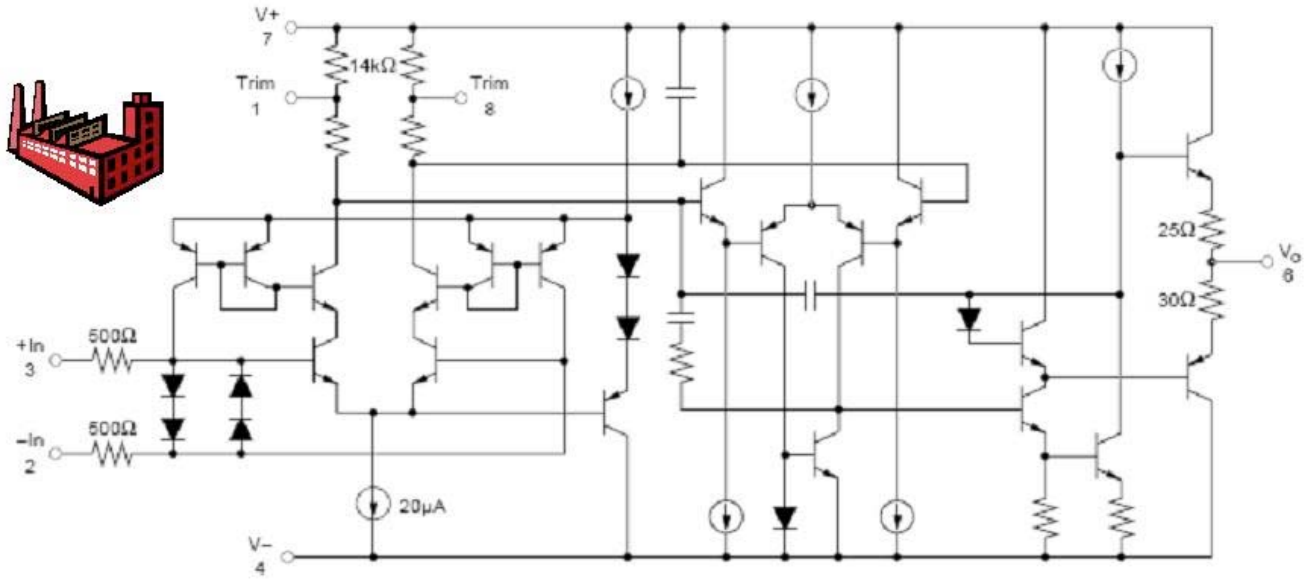


Fig. 10.2: Typical Bipolar Emitter-Follower Op Amp Topology

The Riso w/Dual Feedback circuit we will analyze for Bipolar Emitter-Follower op amps is shown in Fig. 10.3. Through RF direct feedback is provided across the load, CL, and thereby forces Vout to equal VREF. FB#2, through CF, provides a second feedback path, which dominates at high frequency, to guarantee stable operation. Riso creates the isolation between FB#1 and FB#2. Notice than in many of our previous techniques for stabilizing capacitive loads we used the modified Aol approach where the output impedance of the op amp and capacitive load modified the op amp Aol curve, on which we plotted a 1/β which would make the circuit stable. With the Riso w/Dual Feedback technique we will find it easier to leave the op amp Aol curve unmodified and to plot FB#1 1/β and FB#2 1/β. We will then use superposition to arrive at a net 1/β curve which, when plotted on the op amp Aol curve, will allow us to easily synthesize a solution to this capacitive load stability problem.

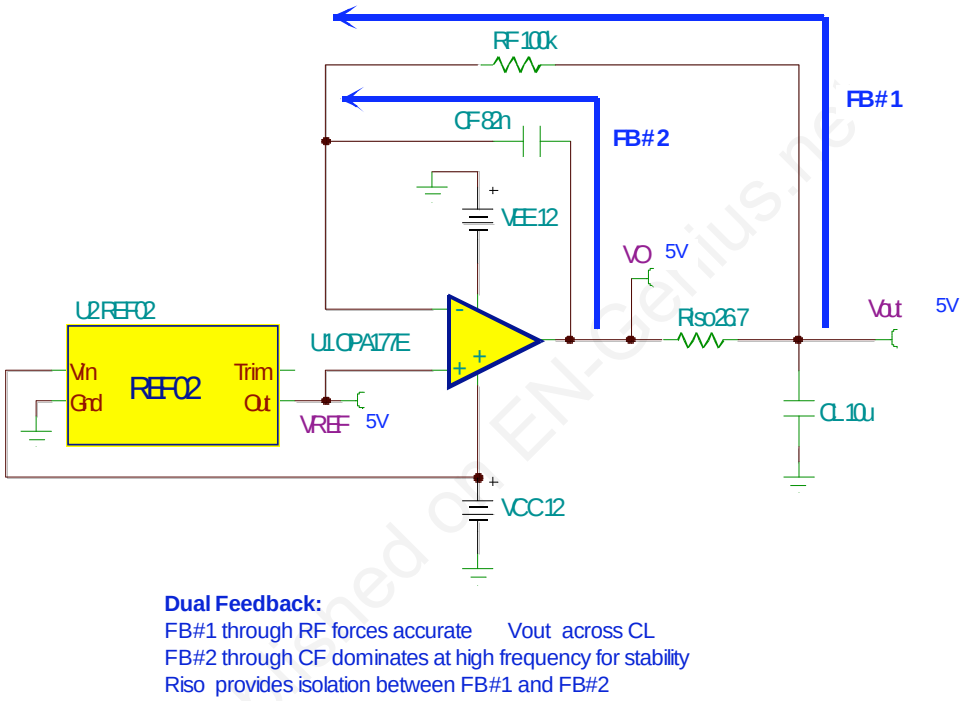


Fig. 10.3: Riso With Dual Feedback: Emitter-Follower

Having a chosen op amp, the Aol Test Circuit (Fig. 10.4) will give us a stability analysis starting point.

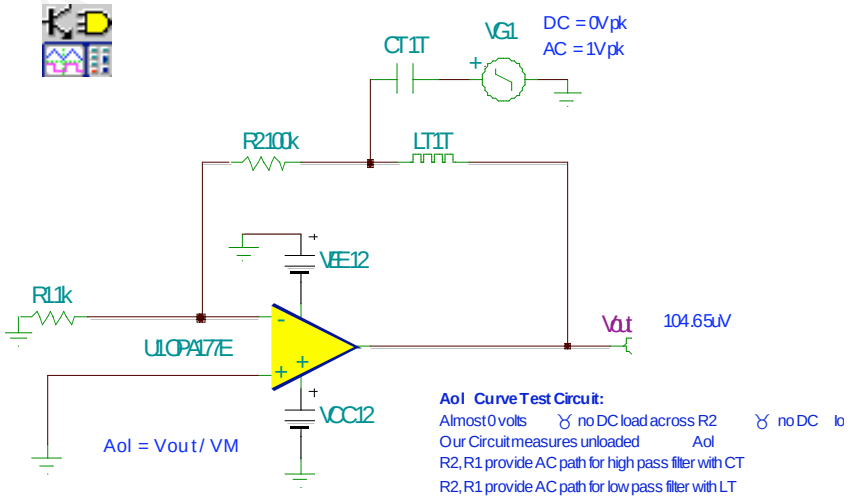


Fig. 10.4: Aol Test Schematic: Emitter-Follower

The Aol curve can be obtained from the data sheet, or measured in our TINA-TI simulation as shown here. This circuit, using dual power supplies, allows us to measure the unloaded Aol curve since Vout is nearly zero volts and our input common mode voltage specification is easily met. R2 and R1 together with LT provide an ac path for the low-pass filter function, which allows us dc short circuit and ac open circuit in the feedback path. Remember, TINA-TI must perform a closed-loop dc analysis to find the operating point of the circuit before it can perform an ac analysis. R2 and R1, together with CT provide an ac path for the high-pass filter function, which allows us dc open circuit and ac short circuit into the input. LT and CT are chosen as large values to ensure their respective operations of shorts and opens at any ac frequency of interest.

In the OPA177 Aol Curve as a result of simulation (Fig. 10.5) the unity gain bandwidth is 607.2 kHz.

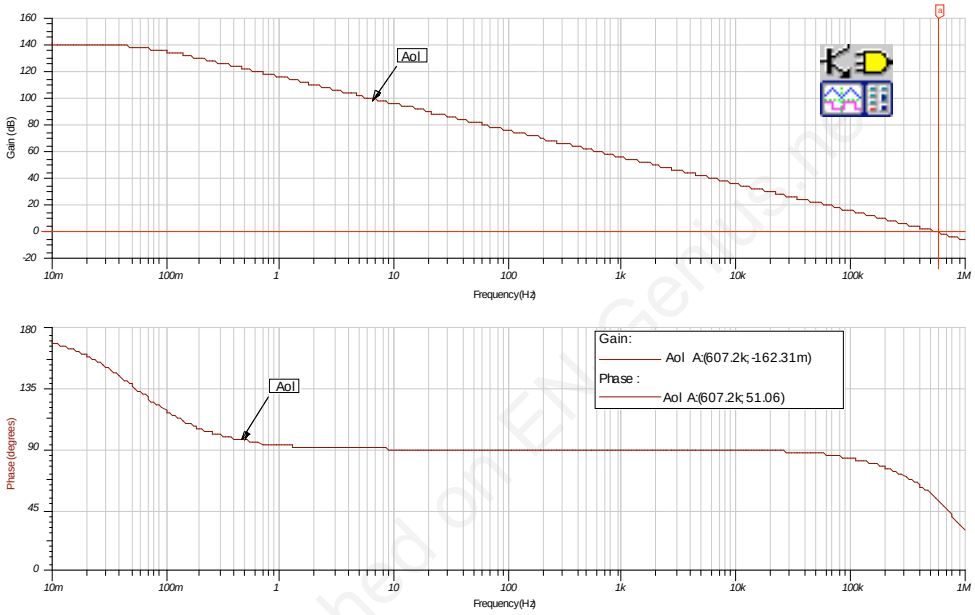


Fig. 10.5: Aol Test Results: Emitter-Follower

We must now measure Zo (small signal ac open loop output impedance) as shown (Fig. 10.6). This TINA-TI test circuit will test the unloaded Zo of the OPA177. R2 and R1 together with LT provide an ac path for the low-pass filter function which allows us dc short circuit and ac open circuit in the feedback path. The dc operating point is shown to be nearly zero volts at the output which means no current is flowing into, or out of, the OPA177. Zo is now easily measured by our application of a 1 Apk ac current generator, which we will sweep over the ac frequency range of 10 MHz to 1 MHz. Zo = Vout, and if we convert the results from dB to linear or logarithmic, Vout will be Zo in ohms.

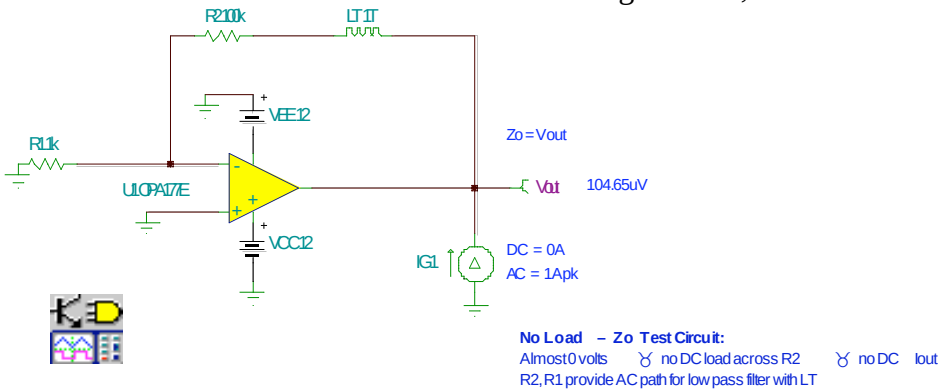


Fig. 10.6: No Load Zo Test Circuit: Emitter-Follower

The OPA177 Zo (Fig. 10.7) is seen to be characteristic of bipolar emitter-follower output stages with Ro dominating the only component of output impedance within the unity-gain bandwidth. Ro is 60 Ω.

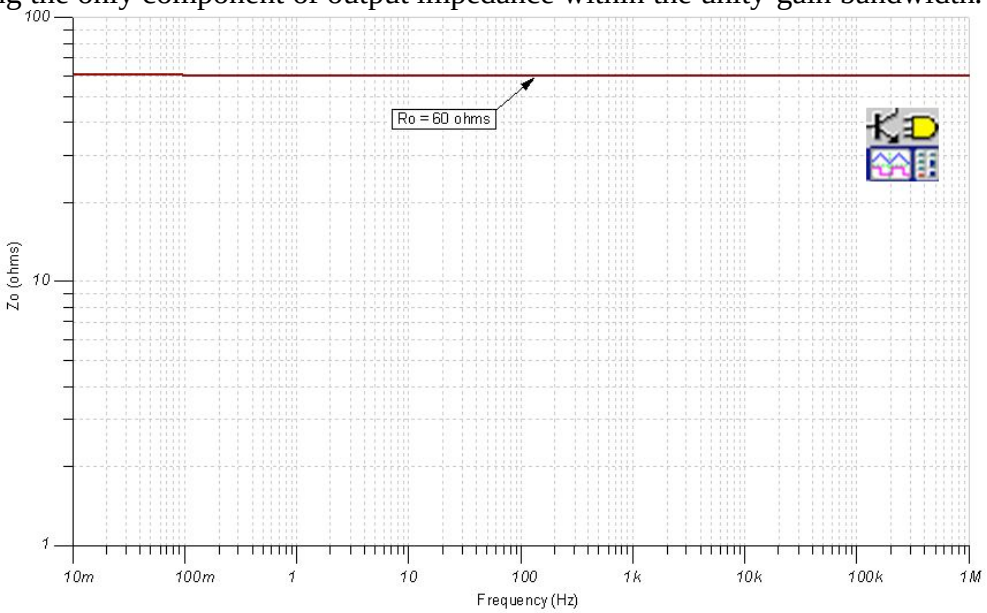


Fig. 10.7: Zo, Open Loop Output Impedance: Emitter-Follower

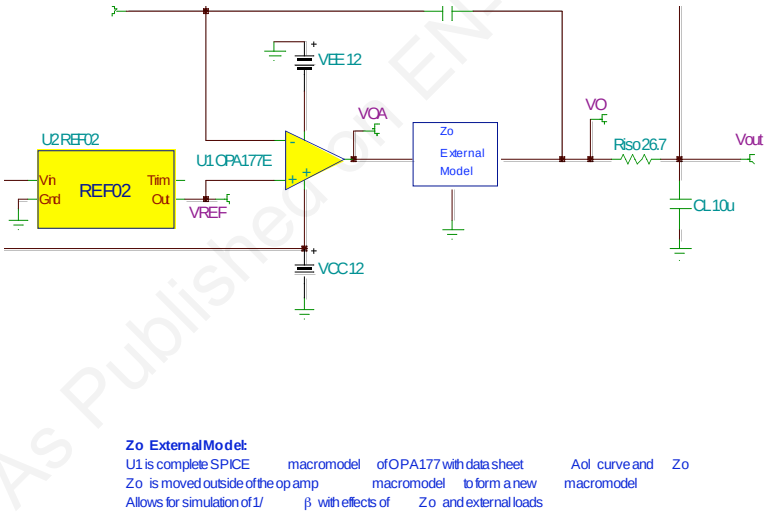


Fig. 10.8: Zo External Model: Emitter-Follower

In order for our 1/β analysis to include the effects of Zo interacting with Riso, CL, CF and RF, we need to move Zo outside of our op amp macromodel so we can probe the necessary nodes in our circuit. This concept (Fig. 10.8) will provide the data sheet Aol curve and be buffered from any effects of Riso, CL, CF and RF.

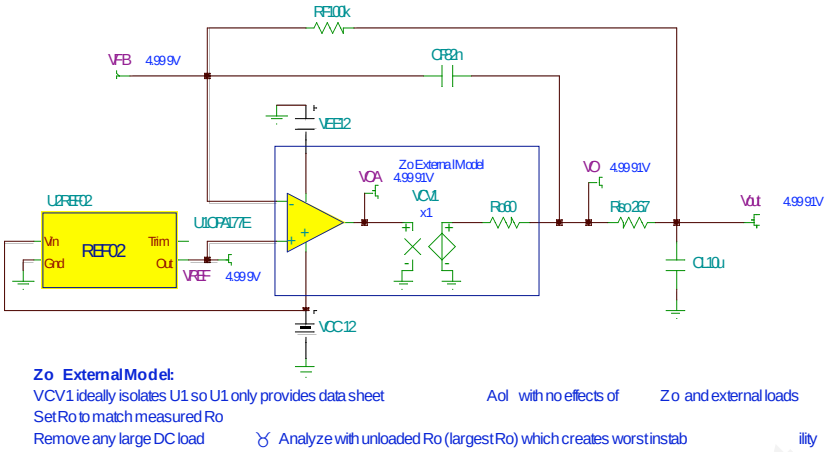


Fig. 10.9: Zo External Model Details: Emitter-Follower

The Zo external model (Fig. 10.9) allows us to measure the effects of Zo interacting with Riso, CL, RF and CF on 1/β. In our Zo External Model set Ro = Ro OPA177, measured to be 60 Ω. The voltage-controlled voltage source, VCV1, isolated our op amp macromodel, U1, from Ro, Riso, CL, CF and RF. VCV1 is set to x1 to keep the data sheet Aol gain the same. Remove any large dc load since we want to analyze this circuit under worst case stability conditions which will be with CL only and our calculated unloaded Zo (Ro=60 Ω for this case). VOA is an internal node to the op amp, which in the real world cannot be measured. It is also not easy to access this internal node on many SPICE macromodels. 1/β is analyzed relative to VOA to include the effects of Ro, Riso, CL, CF, and RF. Final stability simulation in TINA-TI, without using the Zo External Model, cannot plot 1/β but can plot loop gain to confirm our analysis using the Zo external model.

First we will analyze FB#1 (Fig. 10.10). Notice that CF is treated as an open since we are only going to analyze FB#1. Later we will analyze FB#2 and then, using superposition, combine the two feedback paths for the net 1/β. The results of our analysis are shown above with the derivations and details shown in the next slide. We see a zero in the FB#1 1/β plot at fzx = 183.57 Hz. The low frequency 1/β value is one. If this had gain, the low frequency 1/β value would be greater than one.

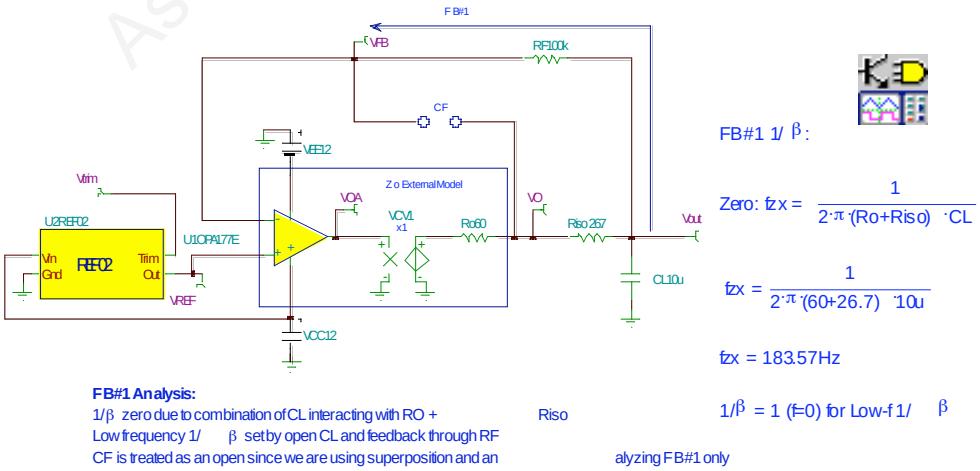


Fig. 10.10: FB#1 Analysis: Emitter-Follower

FB#1 β Derivation:

$$\beta = \frac{VFB}{VOA}$$

$$\beta = \frac{XCL}{Ro+Riso+XCL}$$

$$\beta = \frac{\frac{1}{SCL}}{Ro+Riso+\frac{1}{SCL}}$$

$$\beta = \frac{1}{(Ro+Riso).SCL+1}$$

$$\beta = \frac{\frac{1}{(Ro+Riso).CL}}{S+\frac{1}{(Ro+Riso).CL}}$$

$$\text{Pole: } fpx = \frac{1}{2.\pi.(Ro+Riso).CL}$$

$\beta = 1$ (f=0) for Low-fβ

FB#1 1/β Derivation:

$$1/\beta = \frac{VOA}{VFB}$$

$$1/\beta = \frac{Ro+Riso+XCL}{XCL}$$

$$1/\beta = \frac{Ro+Riso+\frac{1}{SCL}}{\frac{1}{SCL}}$$

$$1/\beta = \frac{(Ro+Riso).SCL+1}{1}$$

$$1/\beta = \frac{S+\frac{1}{(Ro+Riso).CL}}{\frac{1}{(Ro+Riso).CL}}$$

$$\text{Zero: } fzx = \frac{1}{2.\pi.(Ro+Riso).CL}$$

$1/\beta = 1$ (f=0) for Low-f 1β

Fig. 10.11: FB#1 1/β Derivation: Emitter-Follower

In Fig. 10.11 the derivation for FB#1 β is shown on the left. Since 1/β is the reciprocal of β, FB#1 1/β calculation is easily derived as shown on the right. We see that the pole, fpx, in the β derivation becomes the zero, fzx, in the 1/β derivation.

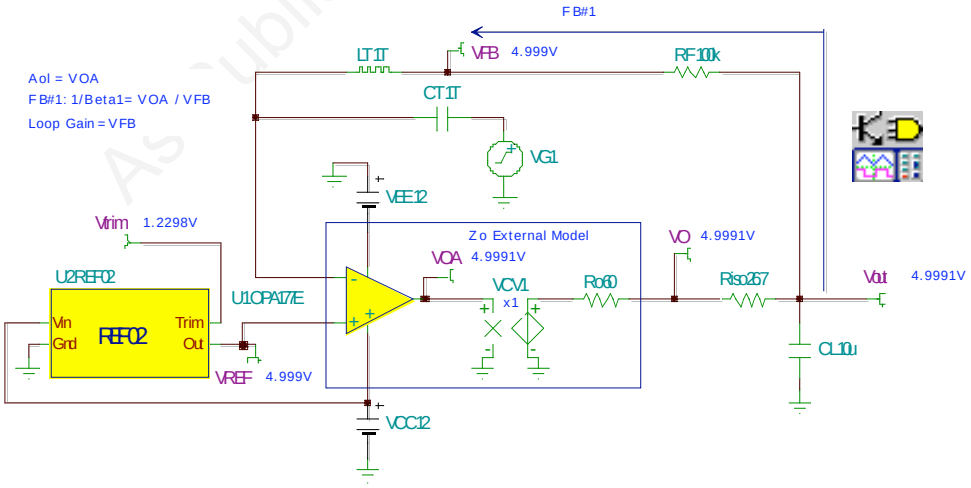


Fig. 10.12: FB#1 Analysis Ac Circuit: Emitter-Follower

We will use the circuit in Fig. 10.12 to perform ac analysis, using TINA-TI, to find 1/β for FB#1, Aol, and loop gain for this circuit using only FB#1. Because of this we eliminate CF from the schematic.

FB#1 1/β results are plotted (Fig. 10.13) on the OPA177 Aol curve. At fcl, where loop gain goes to zero, we see that the rate-of-closure is 40dB/decade:

[(–20 dB/decade from Aol) – (+20 dB/decade from FB#1 1/β) = –40 dB/decade rate-of-closure] which, from our rate-of-closure rule-of-thumb indicates instability. Our analysis of FB#1 was low frequency 1/β = one, with a zero, fzx, at 183.57 Hz. As can be seen (Fig. 10.13) our first-order analysis predicted accurately FB#1 1/β.

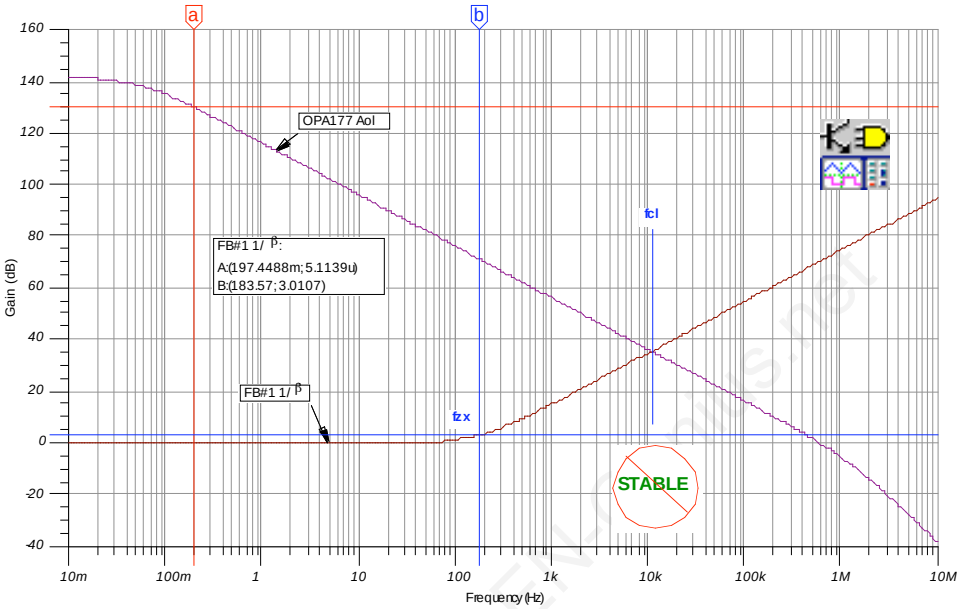


Fig. 10.13: FB#1 1/β Plot: Emitter-Follower

In Fig. 10.14 we see loop gain analysis of our circuit using only FB#1 and it shows that we have close to zero phase margin at fcl where loop goes to zero. This is definite confirmation that we have an unstable circuit. The poles and zeros in the loop gain plot can be predicted, by inspection, from the FB#1 1/β plot on the Aol curve in Fig. 10.13.

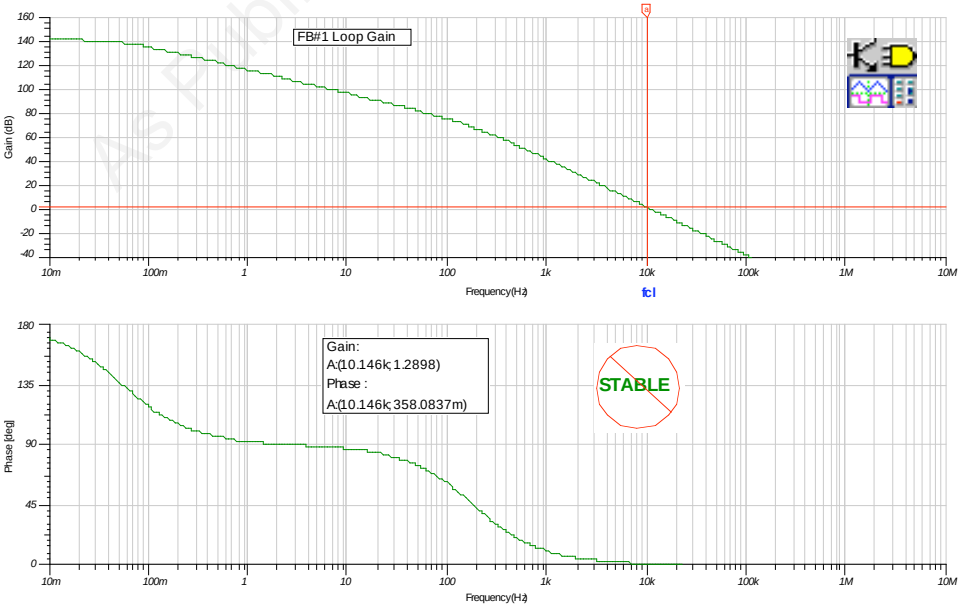


Fig. 10.14: FB#1 Loop Gain Analysis: Emitter-Follower

In case we had any doubt, or if we built our reference buffer circuit with only FB#1 we could use our real world transient stability test using the circuit in Fig. 10.15.

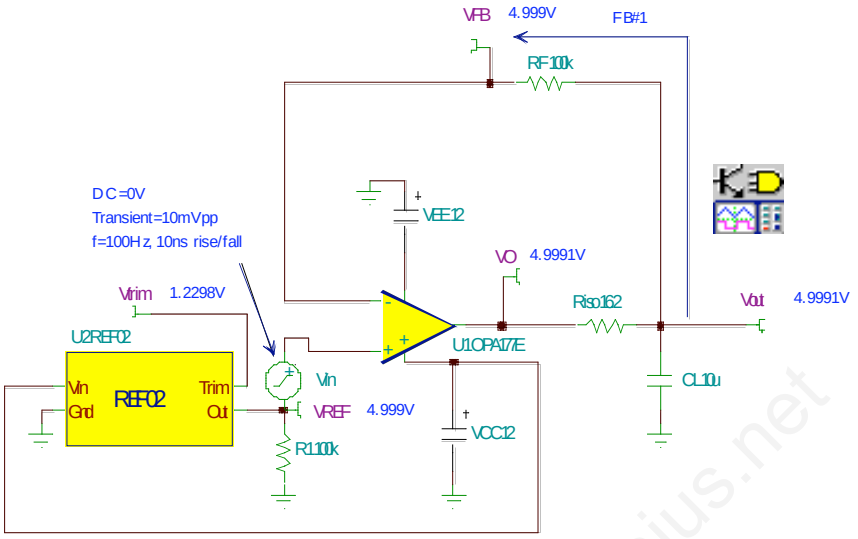


Fig. 10.15: FB#1 Transient Stability Test Circuit: Emitter-Follower

The transient stability test results (Fig. 10.16) coincide with both the 1/β on Aol Pot and loop gain plot in confirming we have an unstable circuit by using only FB#1 in our reference buffer configuration.

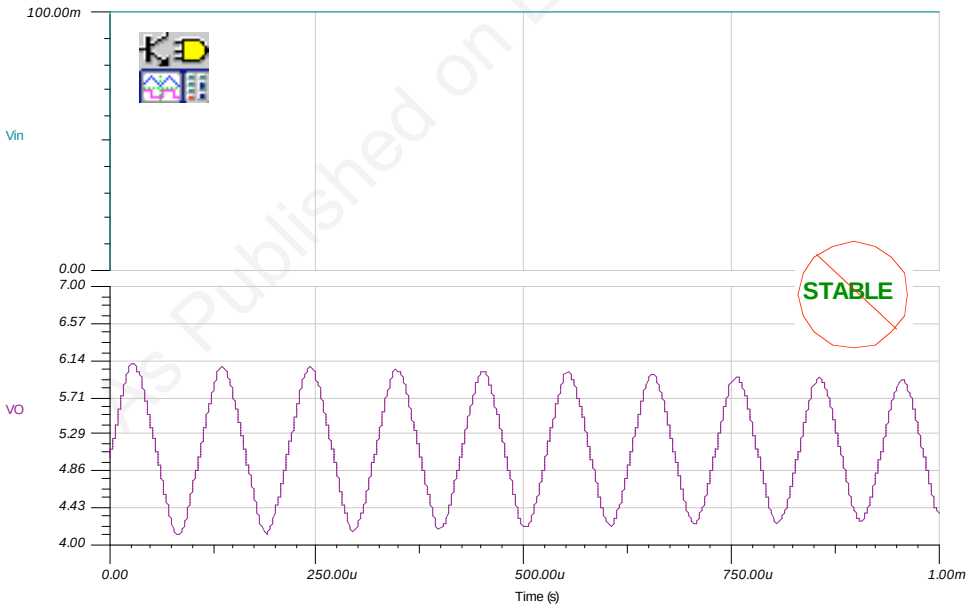


Fig. 10.16: FB#1 Transient Stability Test: Emitter-Follower

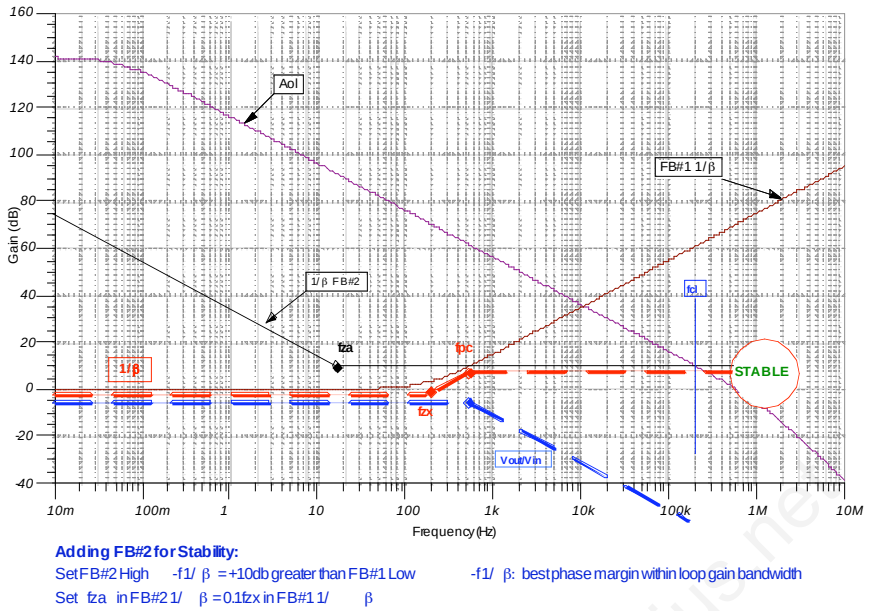


Fig. 10.17: FB#2 Graphical Analysis: Emitter-Follower

Now we must figure out how to synthesize a solution to make our reference buffer with capacitive load stable. At this point we know the Aol curve and the FB#1 1/β (Fig. 10.17). If we add FB#2 1/β we can see a net 1/β which will be a stable circuit from our stability rule-of thumb for rate-of-closure at fcl. Additionally, we will force fpc to be less than a decade from fzx in the 1/β curve to ensure phase margin will be better than 45° for frequencies less than fcl. This is done by setting the high frequency portion of FB#2 1/β only +10 dB greater than the low frequency 1/β of FB#1. fza is set to be at least one decade less than fpc to guarantee that as parameters shift in the real world, we can avoid the BIG NOT. By inspection, the net 1/β curve is formed from FB#1 1/β and FB#2 1/β by choosing the path with lowest 1/β.

Remember, in dual feedback paths the largest voltage fed back from the op amp output to the negative input will dominate the feedback. The largest feedback voltage implies the largest β or the smallest 1/ β. Fig. 10.18 reminds us of this key trick.

As a final point we see that the Vout/Vin transfer function is predicted to follow FB#1 until FB#2 dominates, at which point Vout/Vin will roll off at –20 dB/decade until FB#2 intersects with the Aol curve where it would then follow the Aol curve on down.

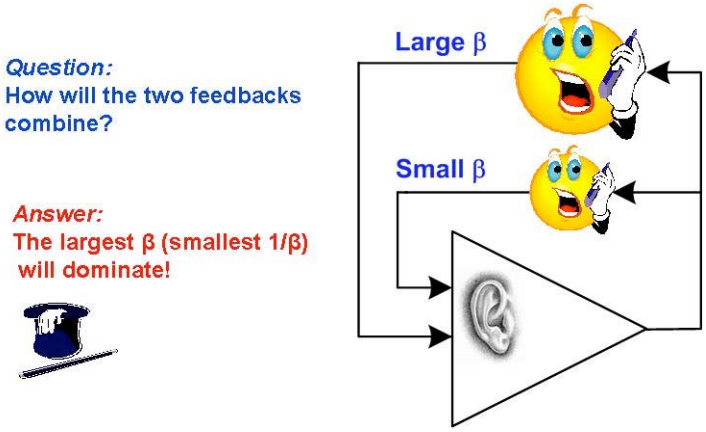
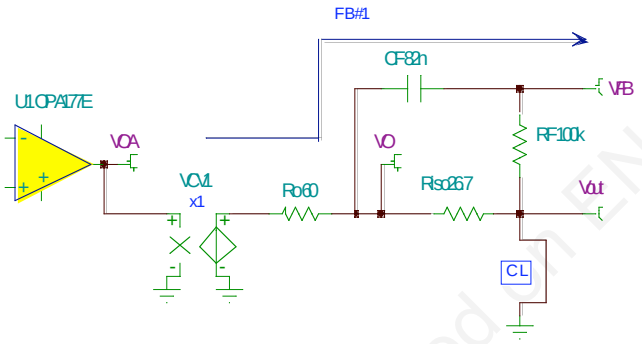


Fig. 10.18: Dual Feedback, Superposition & 1/β: Emitter-Follower

Fig. 10.18 reminds us when using dual feedback paths around op amp circuits the largest β path will dominate. An easy analogy to remember is that if two people are talking to you in one ear, which person do you hear the easiest? The one talking the loudest! So the op amp will *listen* to the feedback path with the largest β or smallest 1/β. The net 1/β plot the op amp sees is the lower one at any frequency of FB#1 1/β or FB#2 1/β.

As shown in Fig. 10.19 there are some key assumptions we will make that apply to almost all Riso w/Dual Feedback circuits. First we will assume that CL > 10 * CF, which means that CL will become a short at high frequencies long before CF does. We will, therefore, short CL to eliminate FB#1 so as to analyze FB#2 independently. In addition, we will assume that RF > 10 * Riso, which implies that that RF has little to no effect as a load across Riso. From Fig. 10.19, and the detailed derivations in Fig. 10.20, we see FB#2 will have a pole at the origin with a zero, fza, at 19.41 Hz caused by RF and CF. The high frequency 1/β portion of FB#2 is a ratio of Ro + Riso to Riso since CF and CL are both a short at high frequency. The derivation of FB#2 1/β is shown in Fig. 10.20 with the results computed in Fig. 10.19. The high frequency 1/β for FB#2 is set to be 3.25 dB or 10.24 dB, with a pole at the origin and a zero at 19.41Hz.



FB#2 Analysis:
1/β pole at the origin
1/β zero set by RF and CF
High - f 1/β set by RO and Riso
CL = zero since we are using superposition and only analyzing FB#2

Assume:
$CL > 10 \cdot CF$
$RF > 10 \cdot Riso$
$\beta = \frac{VFB}{VOA}$
$1/\beta = \frac{VOA}{VFB}$

FB#2 $1/\beta$ Calculation:

Pole: At Origin

Zero: $\frac{1}{2 \cdot \pi \cdot RF \cdot CF}$

Zero: $\frac{1}{2 \cdot \pi \cdot 100k \cdot 82nF}$

Zero: fza = 19.41Hz

High Frequency β:
CL = short
By Inspection:
$1/\beta = \frac{Ro+Riso}{Riso}$ for High-f 1/β
$1/\beta = \frac{60+26.7}{26.7}$ for High-f 1/β
1/β = 3.25 or 10.24dB for High-f 1/β

Fig. 10.19: FB#2 Analysis: Emitter-Follower

FB#2 β Derivation:

FB#2 β Calculation:

$$VFB = \frac{VOA \cdot RF}{XCF + RF}$$

$$\frac{VFB}{VOA} = \frac{RF}{RF + \frac{1}{SCF}}$$

$$\frac{VFB}{VOA} = \frac{SCF \cdot RF}{SCF \cdot RF + 1}$$

$$\frac{VFB}{VOA} = \frac{S}{S + CF \cdot RF}$$

This Implies:
Zero: At Origin

$$\text{Pole: } fpa = \frac{1}{2 \cdot \pi \cdot RF \cdot CF}$$

Assume:
CL > 10·CF
RF > 10·Riso

$$\beta = \frac{VFB}{VOA}$$

$$1/\beta = \frac{VOA}{VFB}$$

High Frequency β:
CL = short
By Inspection:

$$\beta = \frac{Riso}{Ro + Riso}: \beta \text{ High-f}$$

$$1/\beta = \frac{Ro + Riso}{Riso}: 1/\beta \text{ High-f}$$

FB#2 1/ β Derivation:

Fig. 10.20: FB#2 1/β Derivation: Emitter-Follower

The derivation for FB#2 β is shown on the left in Fig. 10.20. Since 1/ β is the reciprocal of β, FB#1 1/β calculation is easily derived as shown on the right. We see that the pole, fpa, in the β derivation becomes the zero, fza, in the 1/β derivation.

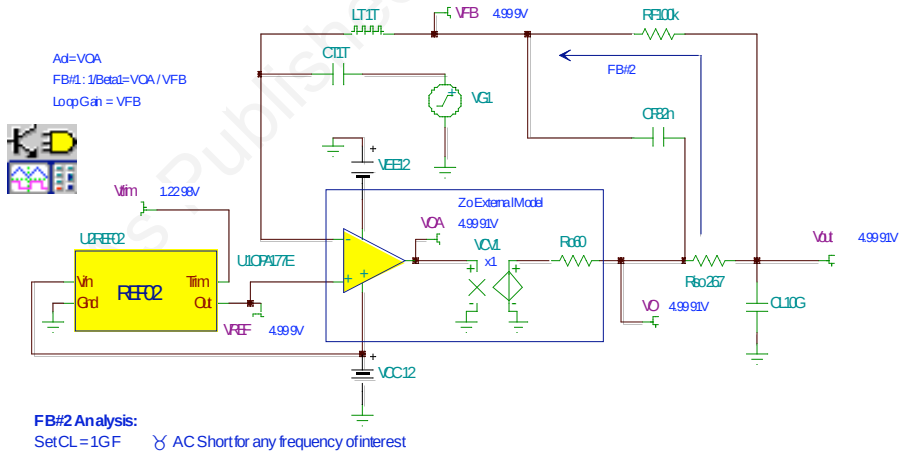


Fig. 10.21: FB#2 Analysis Ac Circuit: Emitter-Follower

To check our first order analysis of FB#2 we can use the TINA-TI circuit shown in Fig. 10.21. For ease of analysis we set CL to 10 GF so it will be a short for any frequencies of interest but will still allow a proper dc operating point to be found by SPICE before the ac Analysis is performed.

The results of our TINA-TI simulation are shown in Fig. 10.22. The FB#2 1/β plot is as predicted by our first-order analysis with fza = 19.41 Hz and a high frequency 1/β of 10.235 dB. We also plot the OPA177 Aol curve to see how FB#2 will intersect with it at high frequency.

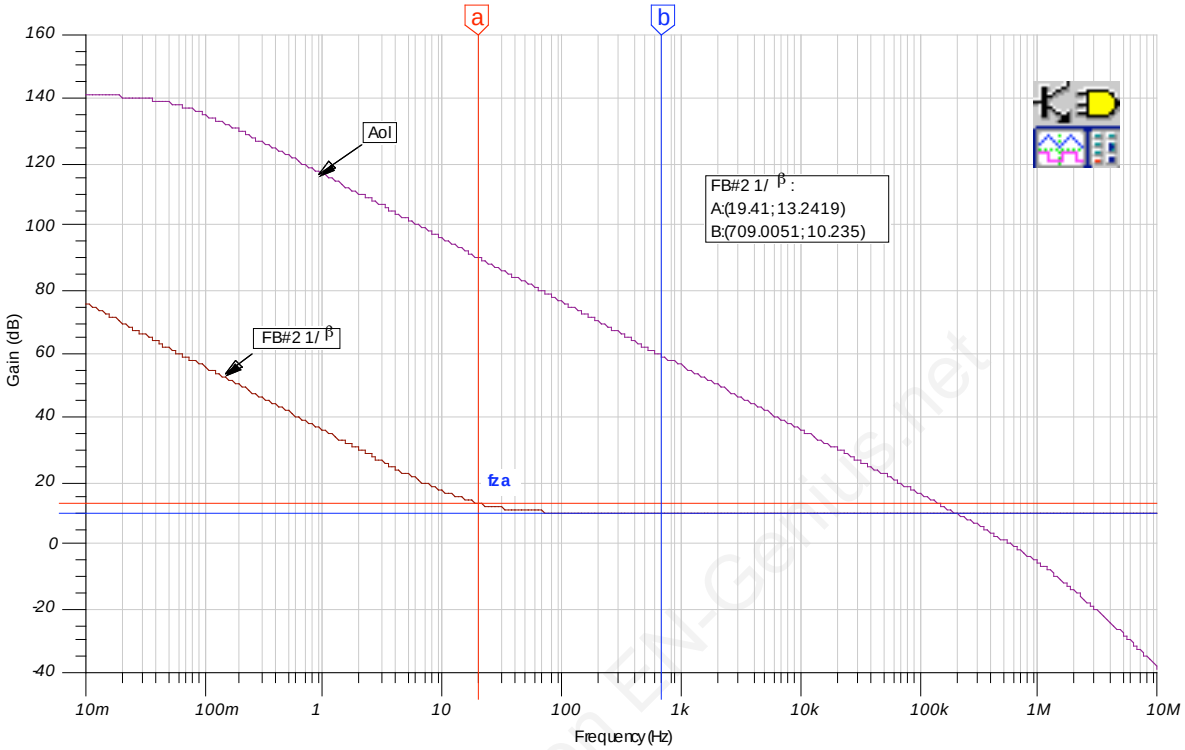


Fig. 10.22: FB#2 1/β Plot: Emitter-Follower

We will analyze if the predicted superposition results of FB#1 and FB#2 will produce the desired net 1/β by using the TINA-TI circuit (Fig.10.23). This same circuit will allow us to plot Aol, net 1/β and loop gain.

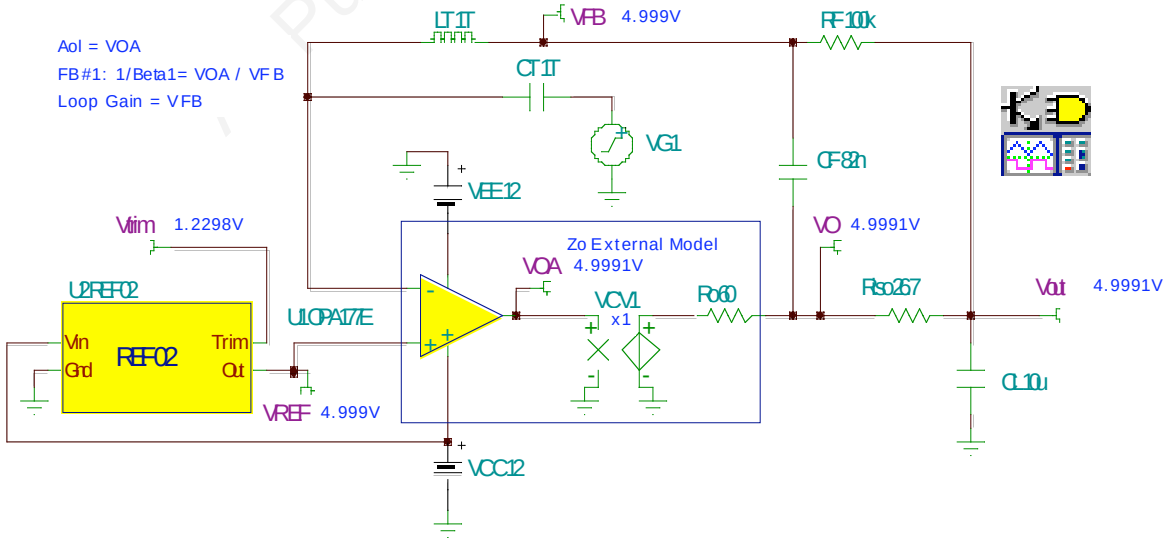


Fig. 10.23: Final Loop Gain Analysis Circuit: Emitter-Follower

In Fig. 10.24 we see our analysis results confirm our predicted net 1/β plot. At fcl, where loop gain goes to zero, we see our expected 20 dB/decade rate-of-closure.

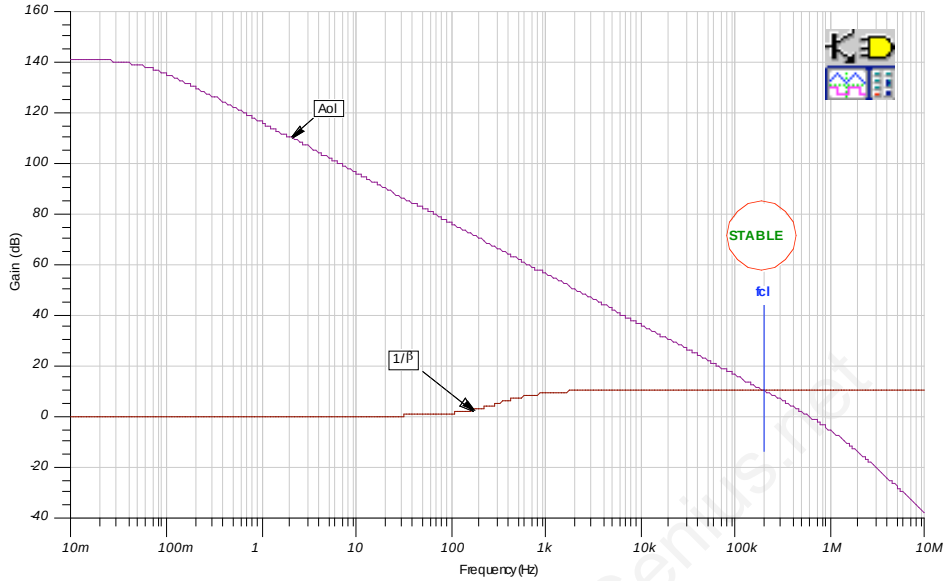


Fig. 10.24: Final Net 1/β: Emitter-Follower

The loop gain phase plot for our final circuit, which uses FB#1 and FB#2 (Fig. 10.25) shows it never dips to less than 58.77° (as seen at 199.57 kHz) and at fcl, 199.57 kHz, the phase margin is 76.59°.

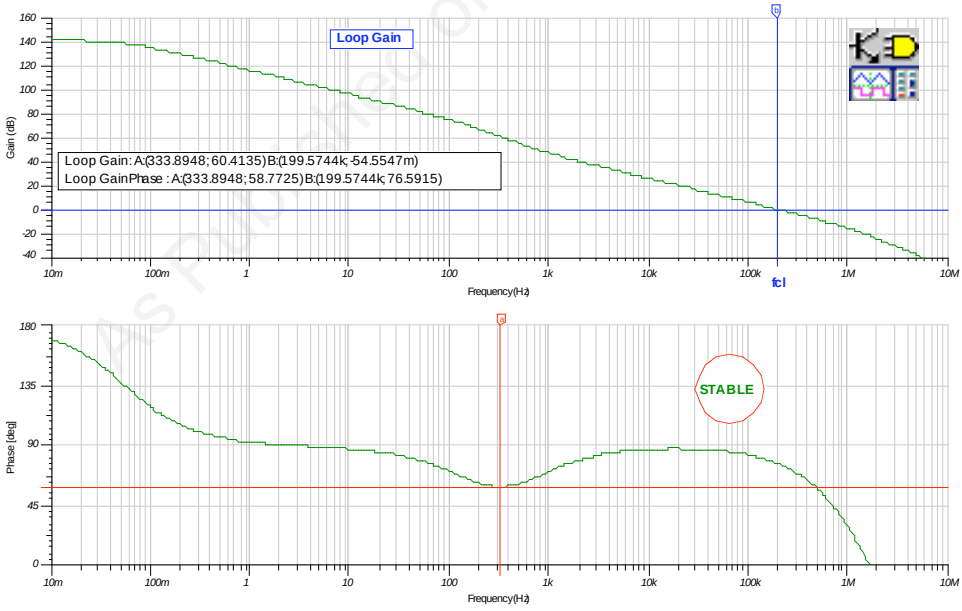


Fig. 10.25: Final Loop Gain Analysis: Emitter-Follower

We do our final check on our stabilized circuit by running a transient stability test using the TINA-TI circuit in Fig. 10.26.

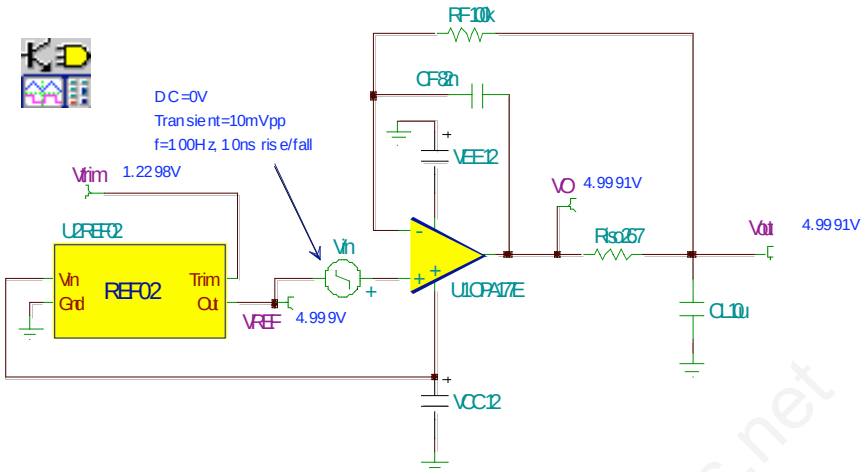


Fig. 10.26: Final Transient Stability Test Circuit: Emitter-Follower

The results of our transient stability test on our final circuit (see Fig. 10.27) agree with all of our other predictions, resulting in a good, stable circuit we can put into production with confidence that we will not have any failures or real world operation anomalies.

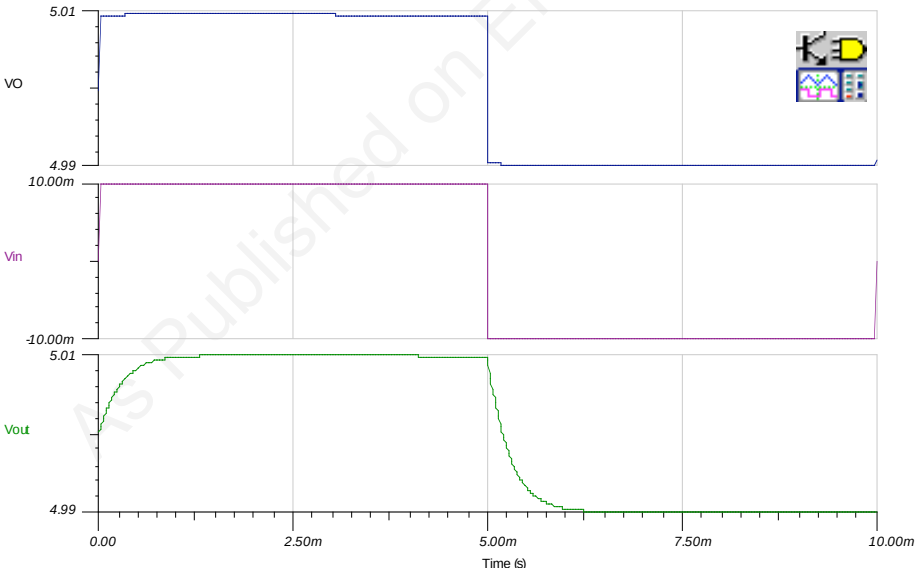


Fig. 10.27: Final Transient Stability Test: Emitter-Follower

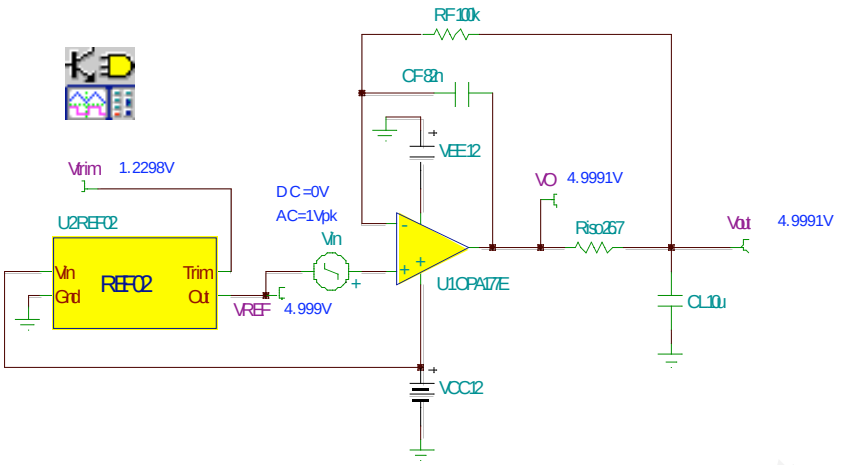


Fig. 10.28: Final Vout/Vin Transfer Function Circuit: Emitter-Follower

The TINA-TI circuit in Fig. 10.28 will allow us to confirm if our prediction of Vout/Vin is correct. We see (Fig. 10.29) that the results of our Vout/Vin test match our predicted first-order results with a single pole roll off at 625.53 Hz and a second pole appearing at about 200 kHz where FB#2 intersects the OPA177 Aol curve.

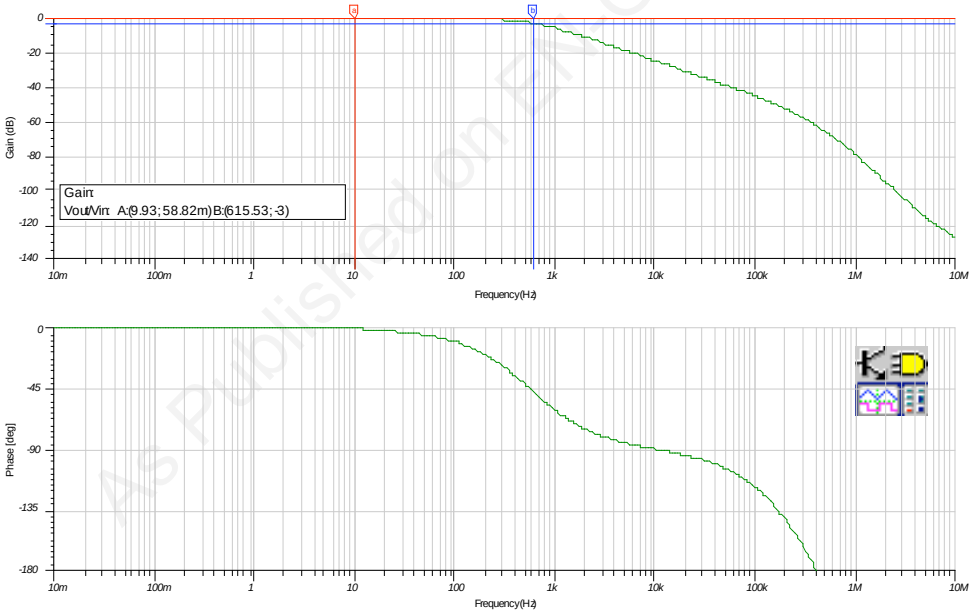
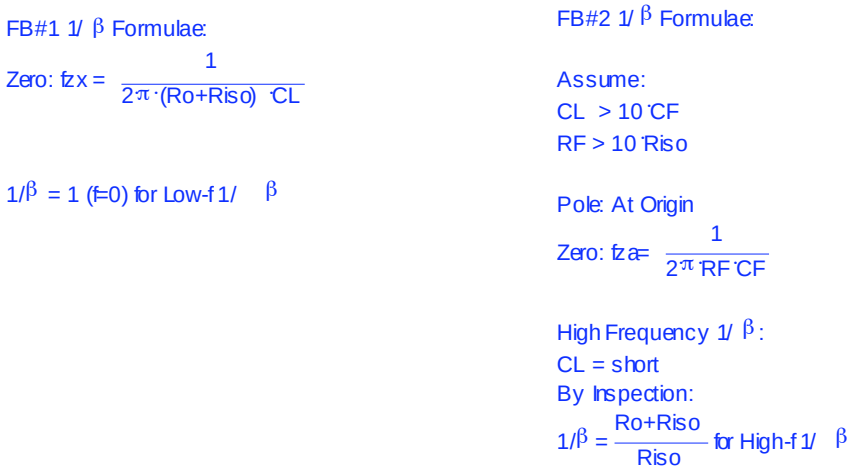


Fig. 10.29: Final Vout/Vin Transfer Function: Emitter-Follower

Fig. 10.30 summarizes an easy to use step-by-step procedure to easily use the Riso w/Dual Feedback capacitive load stability technique on bipolar emitter-follower output op amps.



1) Measure Aol of op amp
2) Measure & Plot Zo of op amp
3) Determine RO
4) Create Zo external model
5) Compute FB#1 Low-f 1/β: equals 1 for unity gain voltage buffer
6) Set FB#2 High-f 1/β = +10 dB higher than FB#1 Low-f 1/β (For best Vout/Vin transient response and least amount of phase shift within loop-gain bandwidth)
7) Choose Riso from FB#2 High-f 1/β and RO
8) Compute FB#1 1/β fzx from CL, Riso, RO
9) Set FB#2 1/β fza = 1/10 fzx
10) Choose RF and CF with practical values to yield fza
11) Run simulation with final values for Aol, 1/β, loop gain, Vout/Vin, transient analysis to confirm design
12) Check for loop-gain Phase shift NOT to dip more than 135° (>45° phase margin)
13) For low noise applications: check for flat Vout/Vin response to avoid gain peaking leading to noise peaking in Vout/Vin

Fig. 10.30: Riso w/Dual Feedback Compensation Procedure: Emitter-Follower

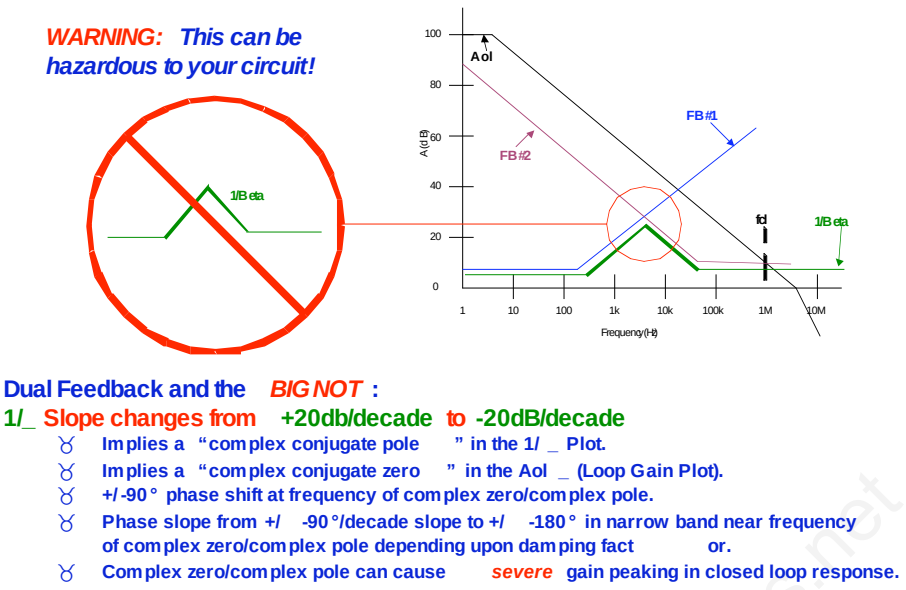


Fig. 10.31: Dual Feedback and the BIG NOT

When using dual feedback paths around an op amp there is one extremely important case to avoid – the "BIG NOT". As demonstrated in Fig. 10.31, there are op amp circuits that can result in feedback paths that create the BIG NOT, which is seen in the net 1/β plot that contains a net 1/β slope which changes from +20 dB/decade to –20 dB/decade abruptly. This rapid change implies a complex conjugate pole in the 1/β plot which is, therefore, a complex conjugate zero in the loop-gain plot. Complex zeros and poles create a ±90º phase shift at the frequency of the complex zero/complex pole. Also, the phase slope around a complex zero/complex pole can range from ±90º to ±180º in a narrow frequency band around the frequency location of the occurrence. Complex zero/complex pole occurrences can cause severe gain peaking in the closed-loop op amp response. This can be very undesirable, especially in power op amp circuits.

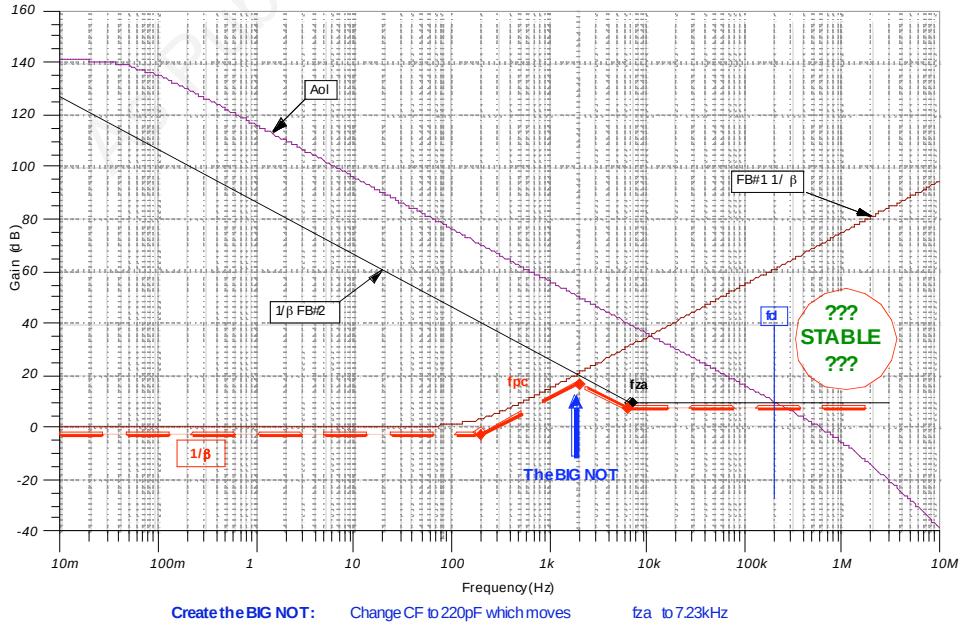


Fig. 10.32: Create the BIG NOT Graphically

Let's return to our plot of FB#1 and FB#2 on the OPA177 Aol curve (Fig. 10.17, again). We can easily create the BIG NOT by simply changing the location of fza (Fig. 10.32).. At fcl our rate-of-closure rule-of-thumb would indicate that this circuit is stable -- but is it?

In Fig. 10.33 we modify our TINA-TI circuit used to analyze FB#1 and FB#2 together to create the BIG NOT, as described in Fig. 10.32. CF is changed from 82 nF to 220 pF to move fza to the desired BIG NOT creation location.

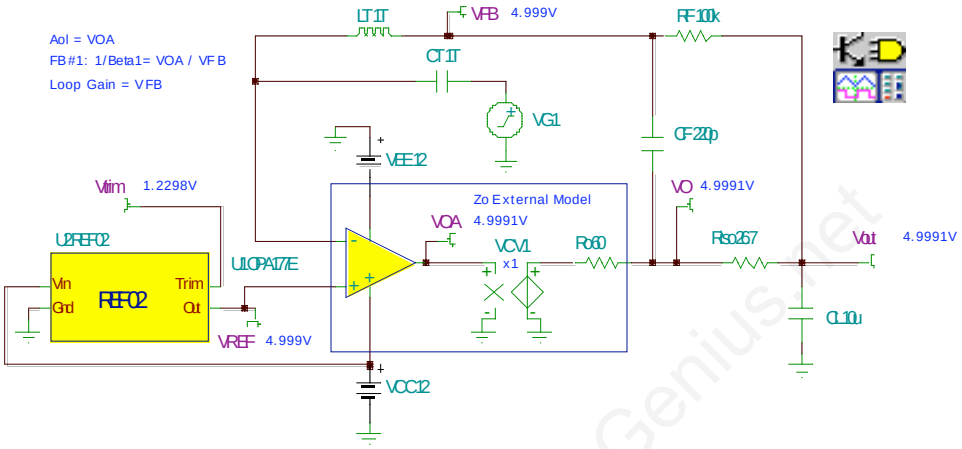


Fig. 10.33: Loop Gain Analysis Circuit: BIG NOT

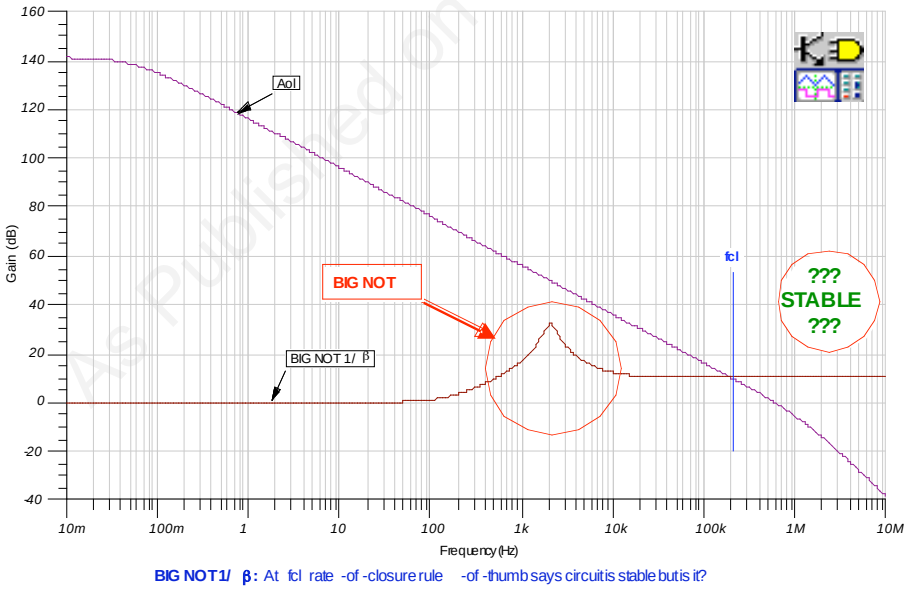


Fig. 10.34: 1/β: BIG NOT

The 1/β plot of the BIG NOT (Fig. 10.34) shows a 20 dB/decade rate of closure, but there is quick turnaround from +20 dB/decade to –20 dB/decade slope in the 1/β plot; peaking is not a good thing and we should question if this circuit will be stable.

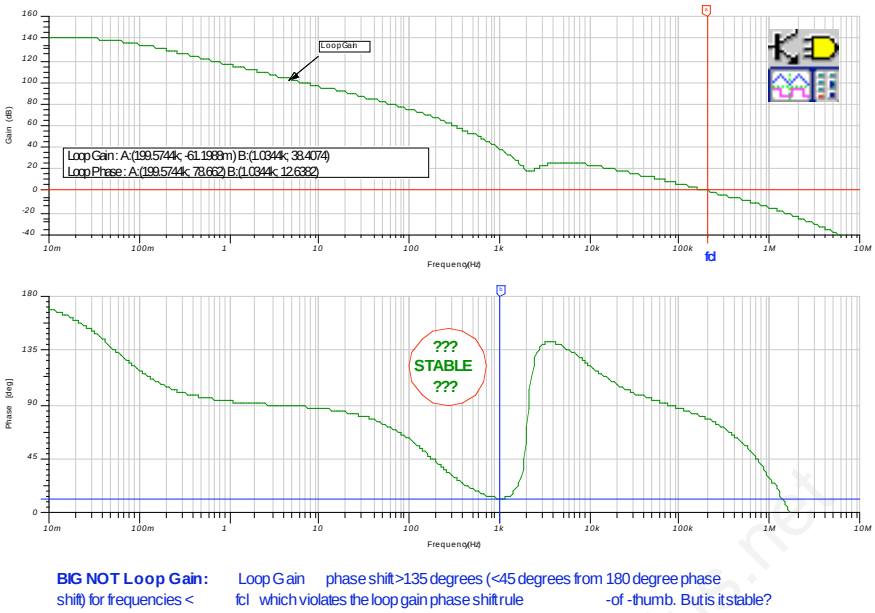


Fig. 10.35: Loop Gain Analysis: BIG NOT

A loop gain plot of our circuit (Fig. 10.35) shows phase shift to be 167° at 1.034 kHz, only 13° away from a 180° phase shift. Also note how loop gain is sharply spiking downwards toward zero loop gain in this same region. Again, at fcl there is plenty of phase margin, but are we stable?

Assume we are inexperienced in the wisdom of stability analysis (which we are not), and built this circuit; what can we expect a real-world transient stability test to look like? The TINA-TI circuit in Fig. 10.36 allows us to see the result of putting this circuit into production and then out into the world.

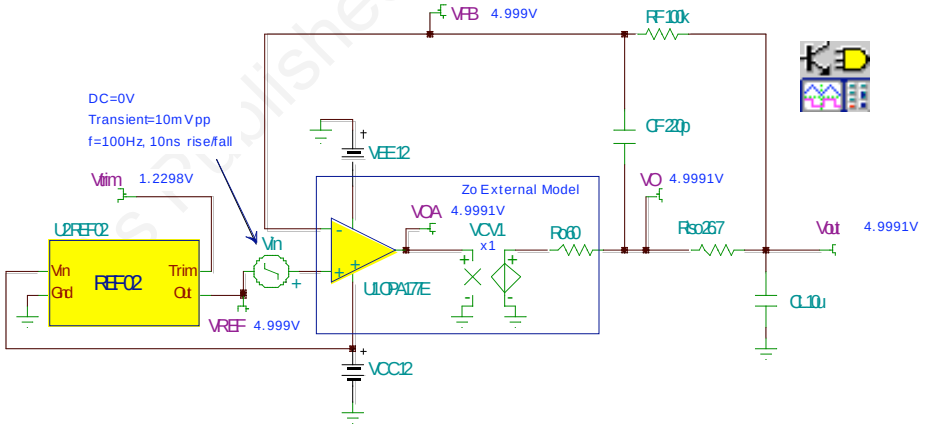


Fig. 10.36: Transient Stability Test Circuit: BIG NOT

Don’t tell your boss we put this circuit into production or, worse yet, the customer who received the equipment you shipped with this circuit which causes weird and intermittent problems when powered-up sometimes, or when something else abruptly loads this reference buffer. Time to update our resumés? Despite the fact that this is not an oscillator, the excessive ringing and long settling time from our transient stability test (Fig. 10.37) indicate an extremely marginally-stable circuit.

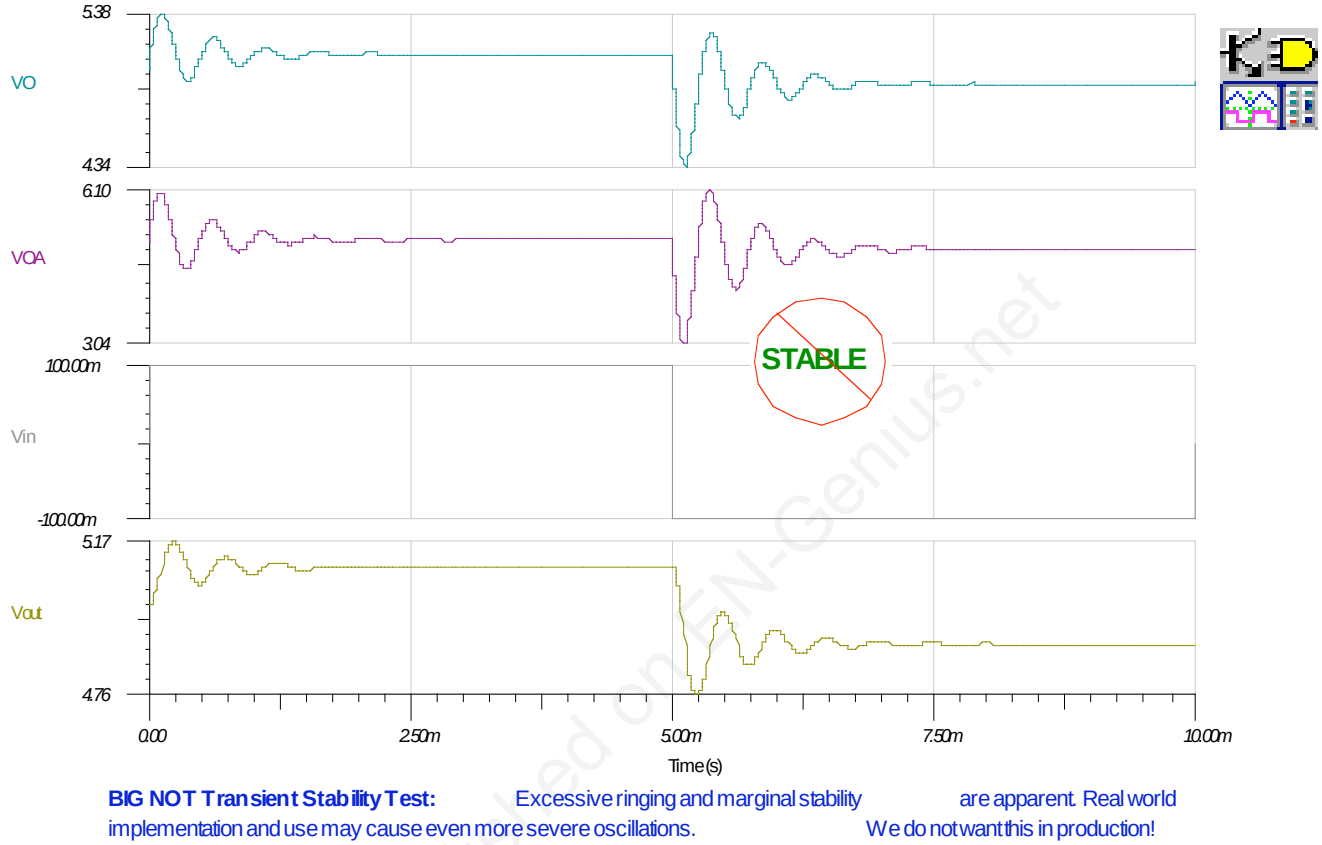


Fig. 10.37: Transient Stability Test: BIG NOT

Depending upon where the BIG NOT occurs, the duration and amplitude of the ringing can easily be worse than this example. From a board and system level view we call this circuit *unstable*, especially since our analysis does not account for real world parasitics in our PCB layout, component and op amp parameter and temperature variances. Fortunately, we only put this into virtual production and can apply our Riso w/Dual Feedback technique properly to the circuit, which will go into real production.

CMOS RRO: Riso w/Dual Feedback

We choose to analyze the Riso w/Dual Feedback technique with the OPA734 (Fig. 10.38). It is a zero-drift, low input offset voltage op amp powered from +2.7 V to +12 V. Low drift of 0.05 µV/°C, plus a super low initial input offset voltage of 1 µV, make it an ideal single supply reference buffer. It is not rail-to-rail on the input so we need to observe the input voltage range of (V–) –0.1 V to (V+) –1.5 V.

OPA734
0.05uV/C Max, Single-Supply, CMOS Operational Amplifier, Zero-Drift Series

Parameter	**Specification**
Supply Voltage (Vs)	+2.7V to +12V
Quiescent Current	600uA typical
Offset Voltage	1uV max
Offset Drift	0.05uV/C max
Input Bias Current	+/-100pA typical
Input Voltage Noise	0.8uVp-p (0.1Hz to 10Hz)
Input Voltage Noise Density	135nV/rt-Hz
Input Voltage Range	(V-)-0.1V to (V+)-1.5V
Gain-Bandwidth Product	1.6MHz
Open Loop Gain	130dB (RL=10k)
Open Loop Output Resistance	125 ohms @ f=1MHz, Io=0A
Slew Rate	1.5V/us
Voltage Output Swing from Rail	20mV max (RL=10k to Vs/2)
Package	SOT23-5, MSOP-8, SO-8

Fig. 10.38: CMOS RRO Op Amp Specifications

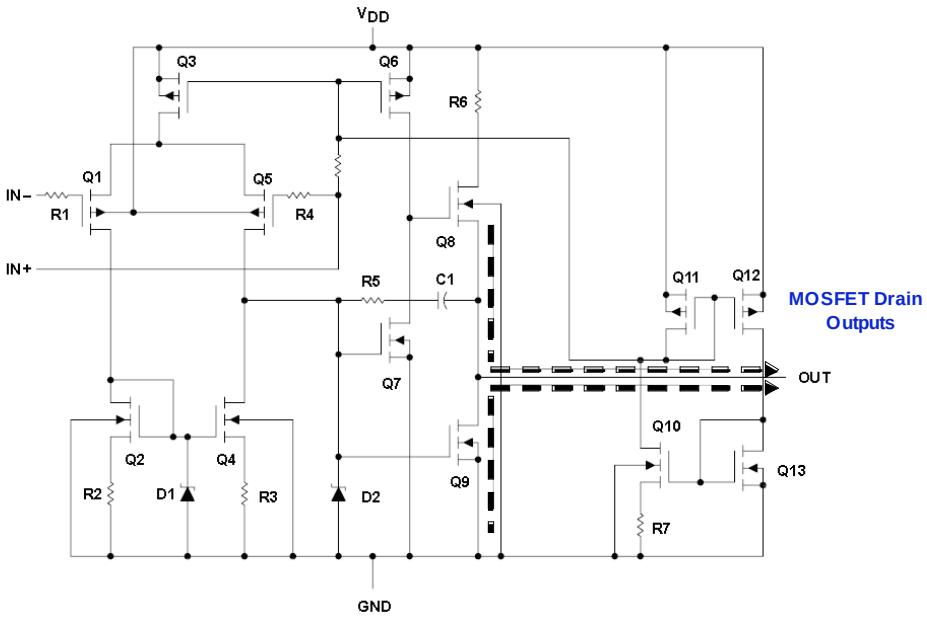
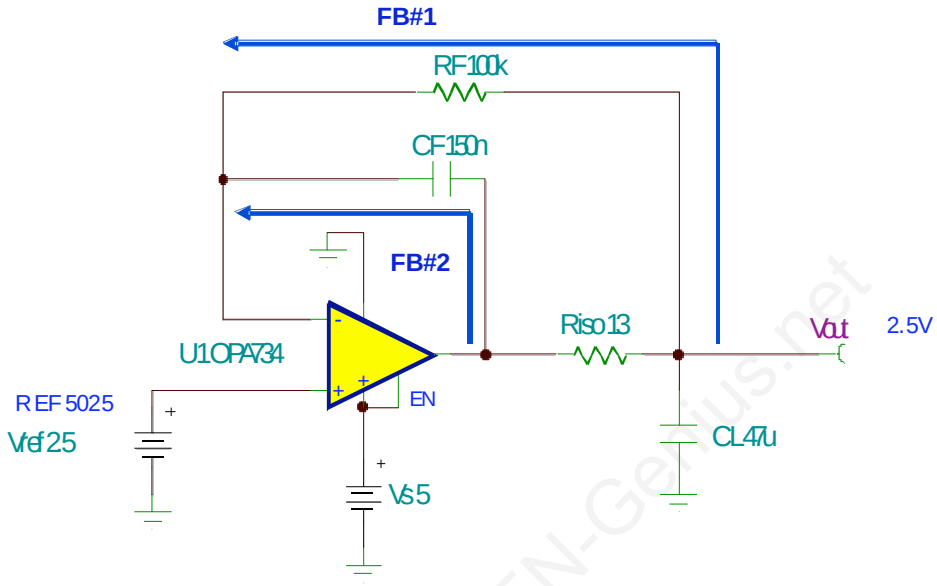


Fig. 10.39: Typical CMOS RRO Op Amp Topology

In a typical CMOS RRO equivalent schematic (Fig. 10.39) the output of the op amp is connected to the drains of the MOSFETs. This type of drain output op amp will exhibit a Zo which is both resistive and capacitive requiring some slightly different techniques for analysis.

From the outside (Fig. 10.40) our CMOS RRO reference buffer looks the same as the bipolar emitter-follower example. This application uses a single 5 V supply and we will be buffering a 2.5 V reference which is under our input voltage range specification (input voltage range: 5 V – 1.5 V = 3.5 V). An accurate reference voltage will be at Vout due to FB#1. FB#2 will provide the required feedback at high frequency for good stability. Riso will provide the needed isolation between the two feedbacks.



Dual Feedback:
FB#1 through RF forces accurate Vout across CL
FB#2 through CF dominates at high frequency for stability
Riso provides isolation between FB#1 and FB#2

Fig. 10.40: Riso w/Dual Feedback: CMOS RRO

With a single supply here, a few new circuit (Fig. 10.41) tricks are used to get the unloaded Aol curve.

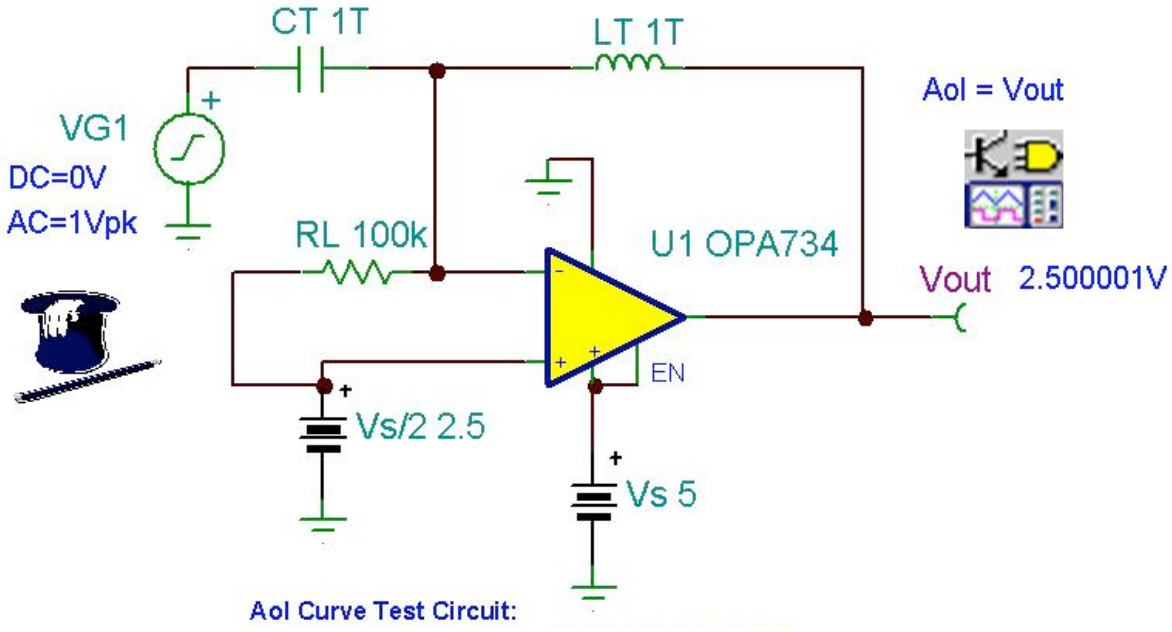


Fig. 10.41: Aol Test Schematic: CMOS RRO

First we need to ensure the OPA734 output, after a dc operating point analysis, is in the linear region of operation. Typically, saturated outputs of op amps do not give correct ac performance since they are not in the linear region, and this is also true for most op amp macromodels. At dc, LT is a short and CT is an open. The non-inverting input of the OPA734 is tied to Vs/2 (2.5 V). Thus, the output will also be at 2.5 V. With RL connected as shown, there is no dc load on the output of the op amp. RL together with LT provides an ac path for the low-pass filter function, which allows a dc short circuit and ac open circuit in the feedback path. Remember, TINA-TI must perform a closed-loop dc analysis to find the operating point of the circuit before it can perform an ac analysis. RL, together with CT, provides an ac path for the high-pass filter function which allows us dc open circuit and ac short circuit into the input. LT and CT are chosen as large values to ensure their respective operations of shorts and opens at any ac frequency of interest.

The OPA734 Aol curve (Fig. 10.42) from the simulation shows the unity-gain bandwidth as 1.77 MHz.

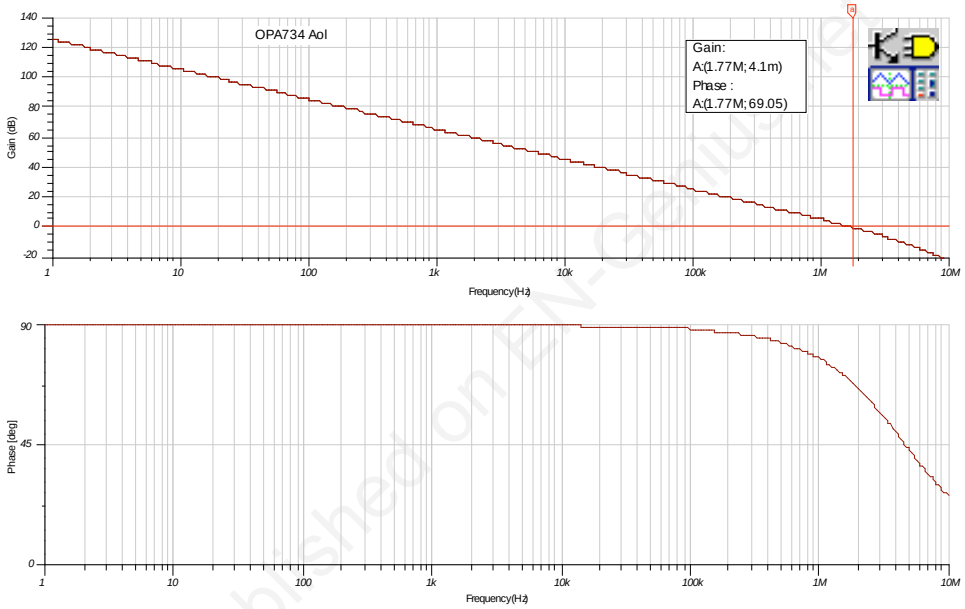


Fig. 10.42: Aol Test Results: CMOS RRO

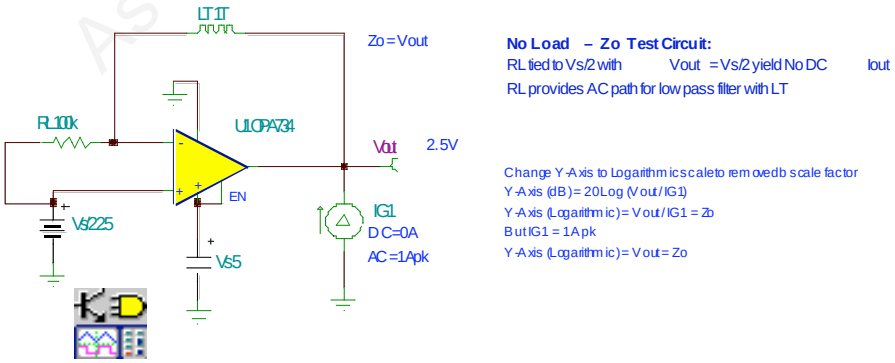


Fig. 10.43: TINA-TI Circuit For Modified Aol Effects By Zo, CCO, RCO, CL

We must now measure Zo (small signal ac open-loop output impedance) as shown in Fig. 10.43. This TINA-TI circuit will test the unloaded Zo of the OPA734. Remember that we chose to put the output at 2.5 V to ensure linear operation. RL, together with LT, provides an ac path for the low-pass

filter function which allows us dc short circuit and ac open circuit in the feedback path. No current is flowing into or out of the OPA734 since RL is tied between Vout (2.5 V) and Vs/2 (2.5 V). Zo is now easily measured by our application of a 1 Apk ac current generator which we will sweep over the ac frequency range of 10 MHz to 1 MHz.

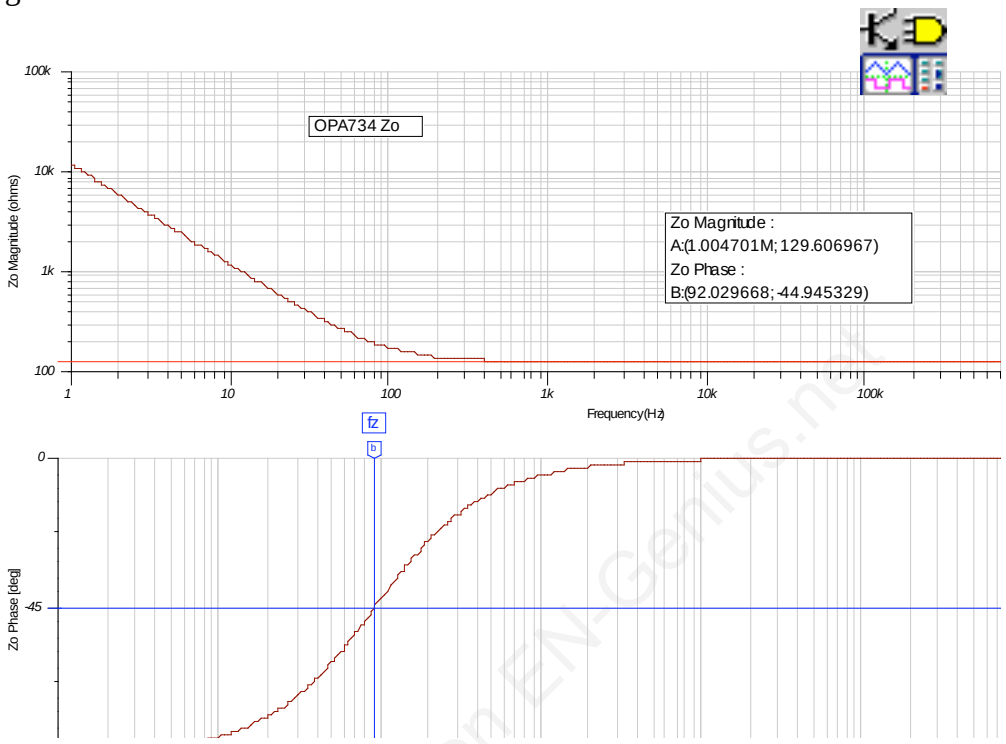
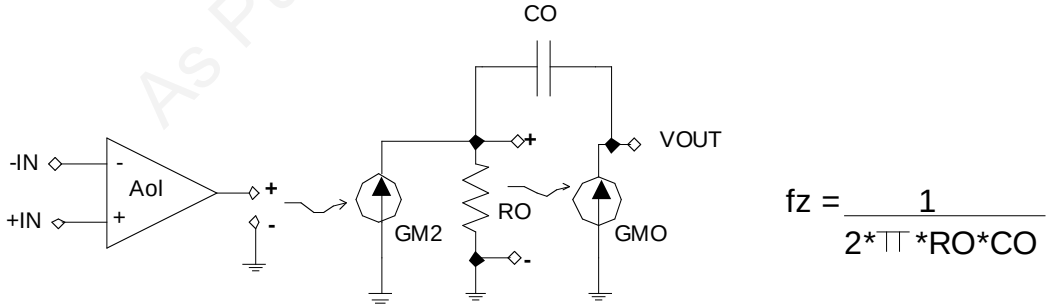


Fig. 10.44: Zo, Open-Loop Output Impedance: CMOS RRO

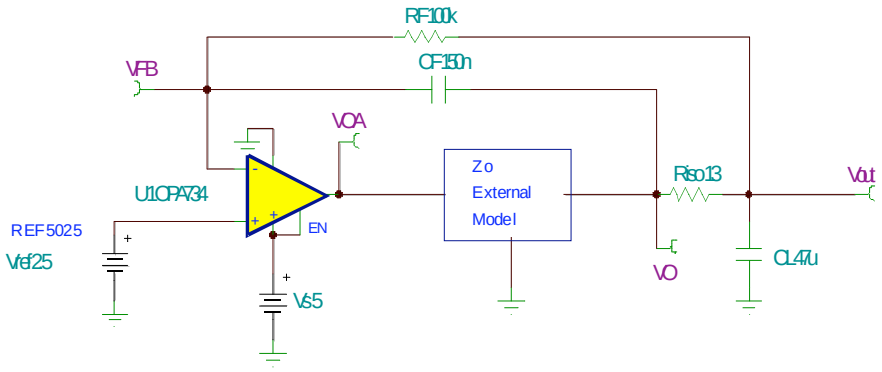
The OPA734 Zo (Fig. 10.44) is characteristic of CMOS RRO output stages with Ro dominating at high frequency, and the capacitive effect represented by Co dominating at frequencies less than 92 Hz.



	fz	RO	CO
No Load	92Hz	129 Ω	13.4 µF

Fig. 10.45: Zo Model: CMOS RRO

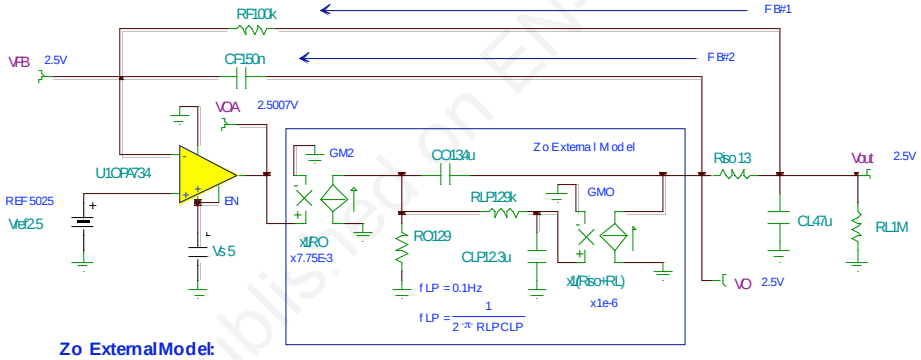
In Fig. 10.45 we build our Zo model of the OPA734 based on simulation test results from the previous slide. RO was measured directly to be 129 Ω and fz was measured directly to be 92 Hz. From fz and RO we can easily compute CO to be 13.4 µF and our Zo model is complete as shown.



Zo External Model:
U1 is complete SPICE macromodel of OPA734 with data sheet Aol curve and Zo
Zo is moved outside of the op amp macromodel to form a new macromodel
Allows for simulation of 1/ β with effects of Zo and external loads

Fig. 10.46: Zo External Model: CMOS RRO

For our 1/β analysis to include the effects of Zo interacting with Riso, CL, CF and RF, we need to move Zo outside of our op amp macromodel so we can probe the necessary nodes in our circuit concept (see Fig. 10.46). U1 will provide the data sheet Aol curve and be buffered from any effects of Riso, CL, CF and RF.

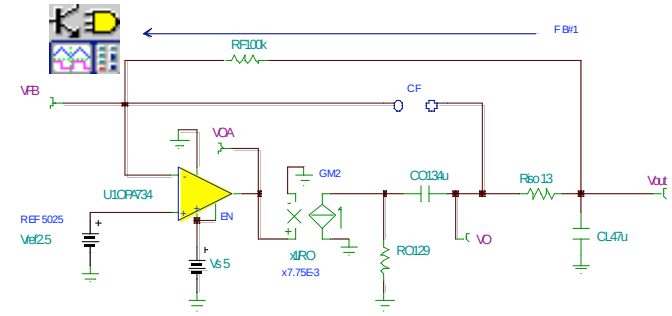


Zo External Model:
GM2 ideally isolates U1 so U1 only provides data sheet Aol with no effects of Zo and external loads
Set GM2 = x1/RO to maintain data sheet Aol gain characteristic
RLP, CLP, GMO provide a path for DC Analysis
Set RLP = 1000 * RO to avoid loading RO to any level of concern
Set CLP to yield fLP = 0.1* fLOW , where fLOW is the lowest frequency of interest
Set GMO = 1/(Riso+RL) to maintain proper data sheet Aol DC gain

Fig. 10.47: Zo External Model Details: CMOS RRO

The Zo External Model (Fig. 10.47) allows for us to measure the effects of Zo interacting with Riso, CL, RF and CF on 1/β. RO and CO are parameters we measured in an earlier slide. GM2 isolates U1, the OPA734 op amp macromodel, from our Zo External Model. GM2 is set to 1/RO to preserve the proper Aol gain to match the original OPA734 op amp macromodel and data sheet Aol. TINA-TI must perform a dc analysis before it can perform an ac analysis. Therefore, we need to make sure our expanded op amp model will have the correct dc operating point without saturating U1. To do this we add a low-frequency path around CO to VO. GMO will be controlled by the voltage across RO which matches VOA. GMO is set to 1/RL to preserve the overall gain at dc to match the original OPA734 Aol. A low-pass filter is formed by RLP and CLP and set to be 0.1 * fLOW where fLOW is our lowest frequency of interest. RLP is set to 1000 * RO to prevent any loading on RO, or interaction, to cause the Zo transfer function to be wrong.

First we will analyze FB#1 (see Fig. 10.48) and notice that CF is treated as an open since we are only going to analyze FB#1. Later we will analyze FB#2 and then, using superposition, combine the two feedback paths for the net 1/β. The results of our analysis are shown Figure 10.48 with the derivations and details in Fig. 10.49. We see a zero in the FB#1 1/β plot at fzx = 107.49 Hz. The low frequency 1/β value is 4.5 or 13 dB and is determined by a capacitor divider between CO and CL. If this circuit were changed to have gain, the low frequency 1/β value would be greater than one.



FB#1 Analysis:

1/β zero due to series combination of CO and CL interacting with RO + Riso

Low frequency 1/ β set by capacitive divider between CO and CL

CF is treated as an open since we are using superposition an ana lyzing FB#1 only

FB#1 1/β :

$$fzx = \frac{1}{2\cdot\pi\cdot\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}$$

$$fzx = \frac{1}{2\cdot\pi\cdot\left(\frac{13.4u\cdot 47u}{47u+13.4u}\right)\cdot(13+129)}$$

$fzx = 107.49Hz$

$$\frac{1}{\beta} = \frac{CL+CO}{CO} \text{ for Low-f}$$

$$\frac{1}{\beta} = \frac{47u+13.4u}{13.4u} \text{ for Low-f}$$

$\frac{1}{\beta}$ = 4.5 or 13dB for for Low-f

Fig. 10.48: FB#1 Analysis: CMOS RRO

FB#1 β Derivation:

$$\beta = \frac{VFB}{VOA}$$

$$\beta = \frac{XCL}{RO+XCO+Riso+XCL}$$

After Algebraic Manipulation:

$$\beta = \frac{\frac{1}{CL\cdot(Riso+RO)}}{S+\frac{1}{\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}}$$

Note: $\frac{CO\cdot CL}{CL+CO}$ is series combination of CO and CL

$$\text{Pole: } fpx = \frac{1}{2\cdot\pi\cdot\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}$$

$$\beta = \frac{CO}{CL+CO} \text{ for } f = 0 \text{ (Low-f } \beta\text{)}$$

CO and CL form a Capacitive Divider

FB#1 1/ β Derivation:

$$\frac{1}{\beta} = \frac{Vout}{VOA}$$

$$\frac{1}{\beta} = \frac{RO+XCO+Riso+XCL}{XCL}$$

After Algebraic Manipulation:

$$\frac{1}{\beta} = \frac{S+\frac{1}{\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}}{\frac{1}{CL\cdot(Riso+RO)}}$$

Note: $\frac{CO\cdot CL}{CL+CO}$ is series combination of CO and CL

$$\text{Zero: } fzx = \frac{1}{2\cdot\pi\cdot\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}$$

$$\frac{1}{\beta} = \frac{CL+CO}{CO} \text{ for } f = 0 \text{ (Low-f 1/ } \beta\text{)}$$

CO and CL form a Capacitive Divider

Fig. 10.49: FB#1 1/β Derivation: CMOS RRO

The derivation for FB#1 β is shown on the left in Fig. 10.49. Since 1/β is the reciprocal of β, FB#1 1/β calculation is easily derived as shown on the right in the same Fig. We can see that the pole, fpx, in the β derivation becomes the zero, fzx, in the 1/β derivation.

We will use the circuit in Fig. 10.50 to perform ac analysis, using TINA-TI, to find 1/β for FB#1, Aol for the OPA734, and loop gain for this circuit using only FB#1.

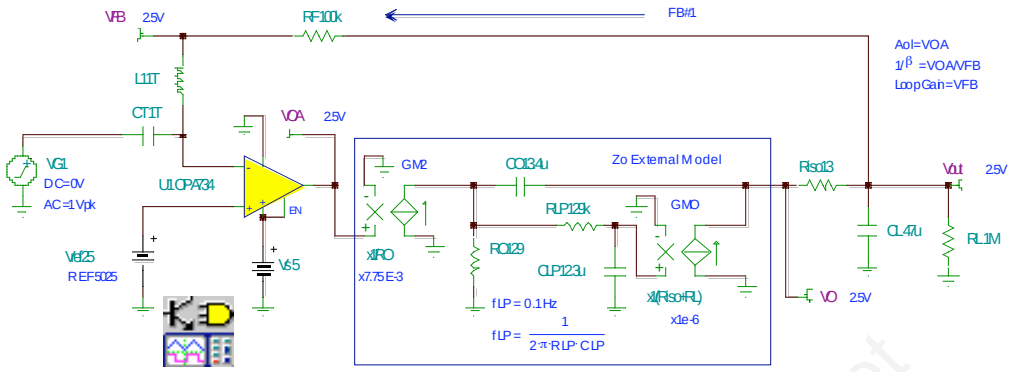


Fig. 10.50: FB#1 Analysis Ac Circuit: CMOS RRO

FB#1 1/β results are plotted on the OPA734 Aol curve (see Fig. 10.51). At fcl, where loop gain goes to zero, we see that the rate-of-closure is 40 dB/decade:

[(–20 dB/decade from Aol) – (+20 dB/decade from FB#1 1/β) = –40 dB/decade rate-of-closure] which, from our rate-of-closure rule-of-thumb, indicates instability.

Our analysis of FB#1 was low frequency 1/β = 13.09 dB with a zero, fzx, at 183.57 Hz, and as can be seen (Fig. 10.51) our first-order analysis predicted accurately FB#1 1/β.

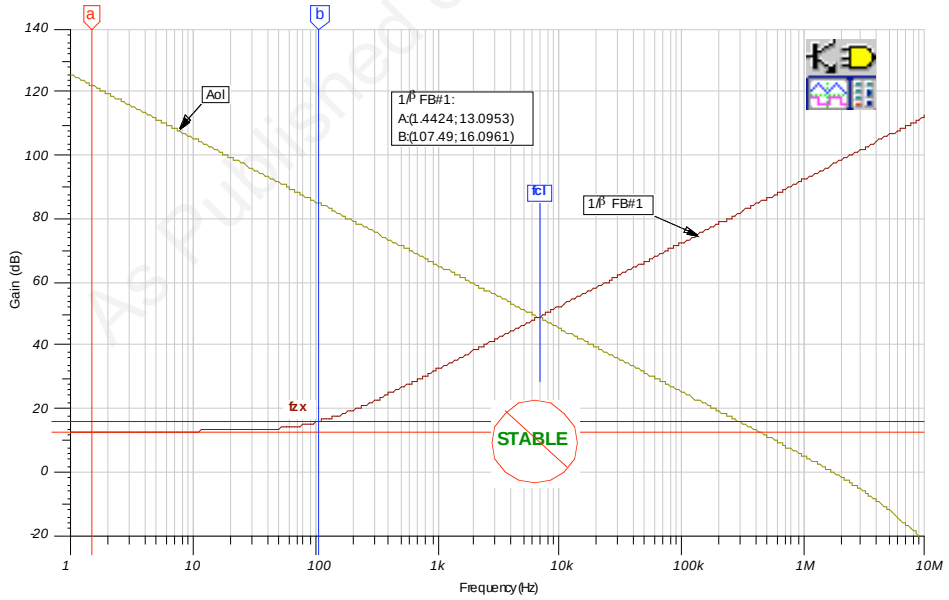


Fig. 10.51: FB#1 1/β Plot: CMOS RRO

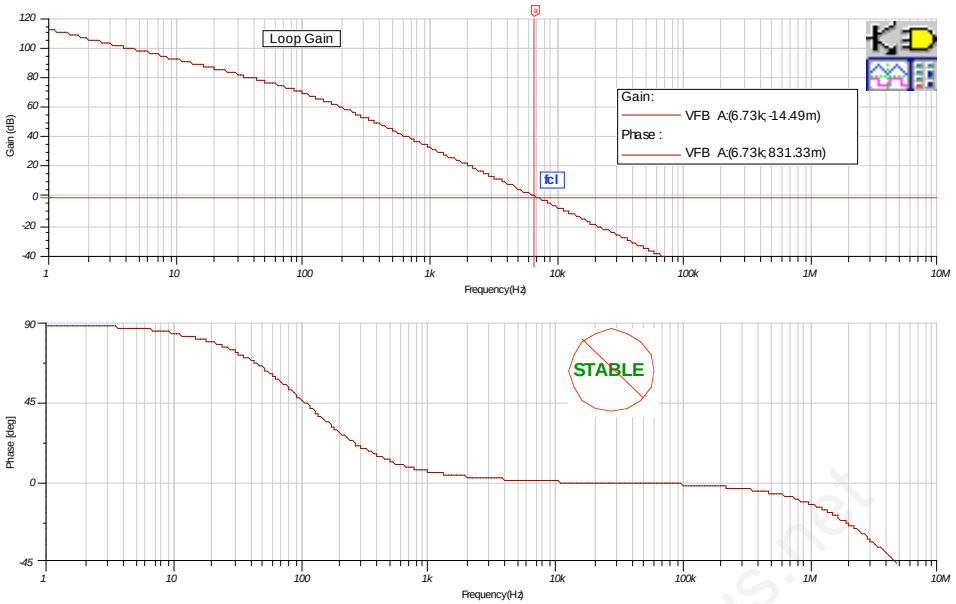


Fig. 10.52: FB#1 Loop Gain Analysis: CMOS RRO

In Fig. 10.52 the loop-gain analysis of our circuit using only FB#1 shows that we have close to zero phase margin at fcl where gain goes to zero. This is definite confirmation that we have an unstable circuit. The poles and zeros in the loop-gain plot can be predicted, by inspection, from the FB#1 1/β plot on the Aol curve (Fig. 10.51, again).

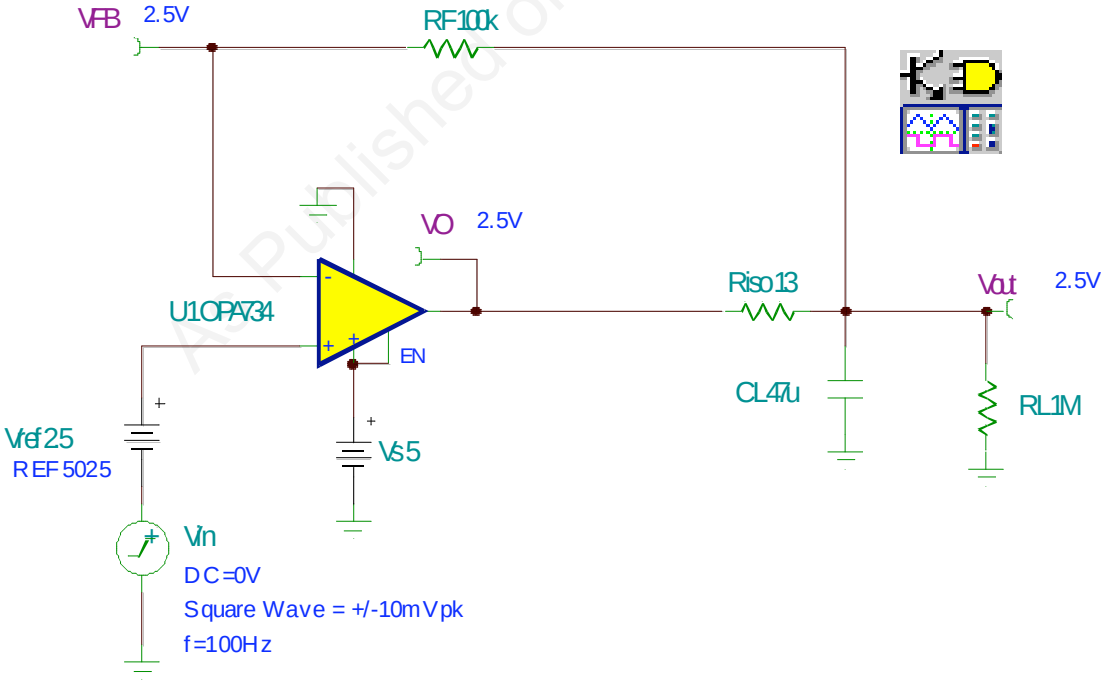


Fig. 10.53: FB#1 Transient Stability Test Circuit: CMOS RRO

In case we had any doubt, or if we built our reference buffer circuit with only FB#1, we could use our real world transient stability test using the circuit in Fig. 10.53.

The transient stability test results (Fig. 10.54) coincide with both the 1/β on Aol Plot and loop-gain plot in confirming we have an unstable circuit by using only FB#1 in our reference buffer configuration.

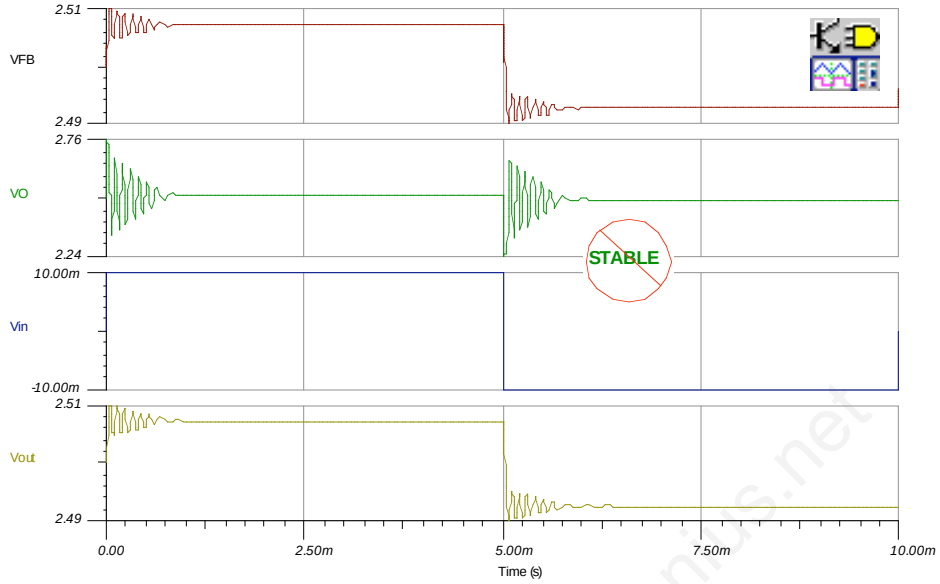


Fig. 10.54: FB#1 Transient Stability Test: CMOS RRO

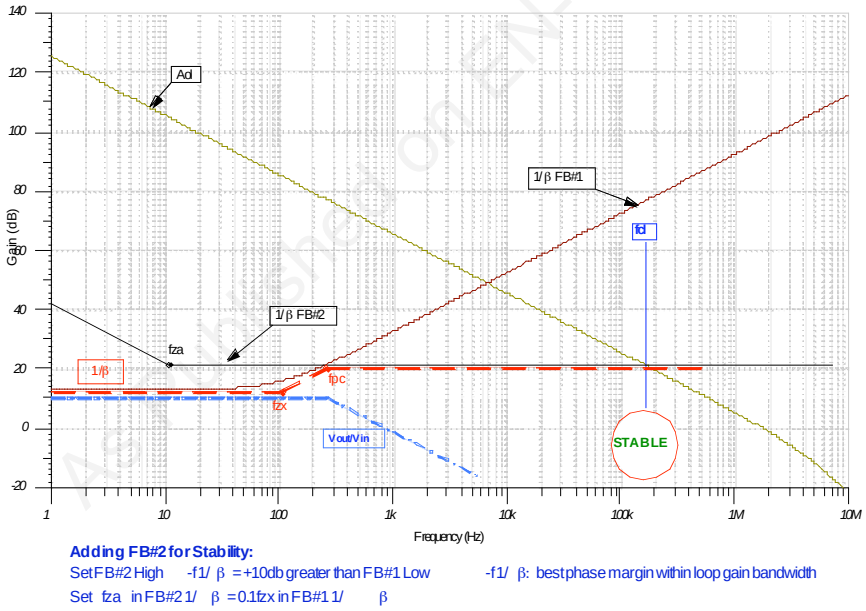


Fig. 10.55: FB#2 Graphical Analysis: CMOS RRO

Now we must figure out how to synthesize a solution to make our reference buffer with capacitive load stable. At this point we know the Aol curve and the FB#1 1/β (Fig. 10.55). If we add FB#2 1/β (Fig. 10.55) we can see a net 1/β which will be stable from our rule-of thumb for rate-of-closure at fcl. Moreover, we will force fpc to be less than a decade from fzx in the 1/β curve to ensure phase margin better than 45° for frequencies less than fcl, by setting the high frequency portion of FB#2 1/β only +10 dB greater than the low frequency 1/β of FB#1. Fza is set to be at least one decade less than fpc to guarantee that as parameters shift in the real world we can avoid the BIG NOT. By inspection, the net 1/β curve is formed from FB#1 1/β and FB#2 1/β by choosing the path with lowest 1/β.

Remember, in dual-feedback paths the largest voltage fed back from the op amp output to the negative input will dominate the feedback. The largest feedback voltage implies the largest β or the smallest 1/β.

As a final point, we see that the Vout/Vin transfer function is predicted to follow FB#1 until FB#2 dominates at which point Vout/Vin will roll off at –20 dB/decade until FB#2 intersects with the Aol curve where it would then follow the Aol curve on down.

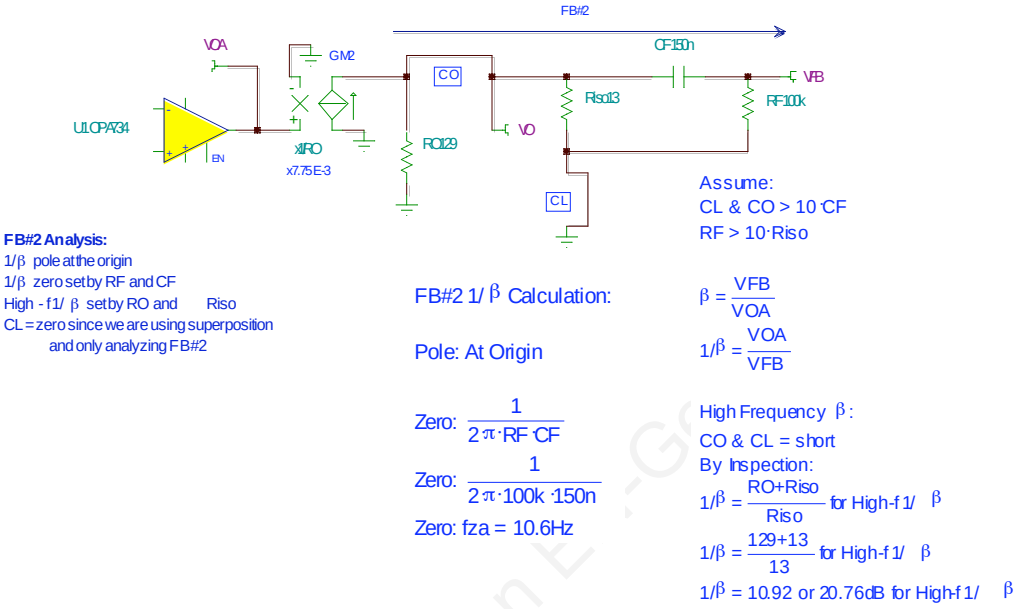


Fig. 10.56: FB#2 Analysis: CMOS RRO

There are some key assumptions (see Fig. 10.56) we will make that apply to almost all Riso w/Dual Feedback circuits. First we will assume that CL > 10 * CF, which means that CL will become a short at high frequencies long before CF does. We will, therefore, short CL to eliminate FB#1 so as to analyze FB#2 independently. Furthermore, we will assume that RF > 10 * Riso which implies that that RF has little-to-no effect as a load across Riso. From Fig. 10.56 and the detailed derivations in Fig. 10.57, we see FB#2 will have a pole at the origin with a zero, fza, at 19.41 Hz caused by RF and CF. The high frequency 1/β portion of FB#2 is a ratio of Ro+Riso to Riso since CF and CL are both a short at high frequency. The derivation of FB#2 1/β is shown in the next figures. The high frequency 1/β for FB#2 is set to be 10.92 or 20.76 dB with a pole at the origin and a zero at 10.6 Hz.

The derivation for FB#2 β is shown on the left in Fig. 10.57. Since 1/β is the reciprocal of β, FB#1 1/β calculation is easily derived as shown on the right. We see that the pole, fpa, in the β derivation becomes the zero, fza, in the 1/β derivation.

FB#2 β Derivation:

FB#2 β Calculation:

$$VFB = \frac{VOA \cdot RF}{XCF+RF}$$

$$\frac{VFB}{VOA} = \frac{RF}{RF + \frac{1}{SCF}}$$

$$\frac{VFB}{VOA} = \frac{SCF \cdot RF}{SCF \cdot RF+1}$$

$$\frac{VFB}{VOA} = \frac{S}{S+CF \cdot RF}$$

This Implies:
Zero: At Origin

$$\text{Pole: fpa} = \frac{1}{2 \cdot \pi \cdot RF \cdot CF}$$

Assume:
CL & CO > 10 ·CF
RF > 10·Riso

$$\beta = \frac{VFB}{VOA}$$

$$1/\beta = \frac{VOA}{VFB}$$

High Frequency β:
CO & CL = short
By Inspection:

$$\beta = \frac{Riso}{RO+Riso}: \beta \text{ High-f}$$

$$1/\beta = \frac{RO+Riso}{Riso}: 1/\beta \text{ High-f}$$

FB#2 1/ β Derivation:

FB#2 1/β Calculation:

$$VFB = \frac{VOA \cdot RF}{XCF+RF}$$

$$\frac{VOA}{VFB} = \frac{RF + \frac{1}{SCF}}{RF}$$

$$\frac{VOA}{VFB} = \frac{SCF \cdot RF+1}{SCF \cdot RF}$$

$$\frac{VOA}{VFB} = \frac{\frac{1}{S+CF \cdot RF}}{S}$$

This Implies:
Pole: At Origin

$$\text{Zero:fza} = \frac{1}{2 \cdot \pi \cdot RF \cdot CF}$$

Fig. 10.57: FB#2 Analysis: CMOS RRO

To check our first-order analysis of FB#2 we can use the TINA-TI circuit of Fig. 10.58. For ease of analysis we set CL to 10 GF so it will be a short for any frequencies of interest, but will still allow a proper dc operating point to be found by SPICE before the ac analysis is performed.

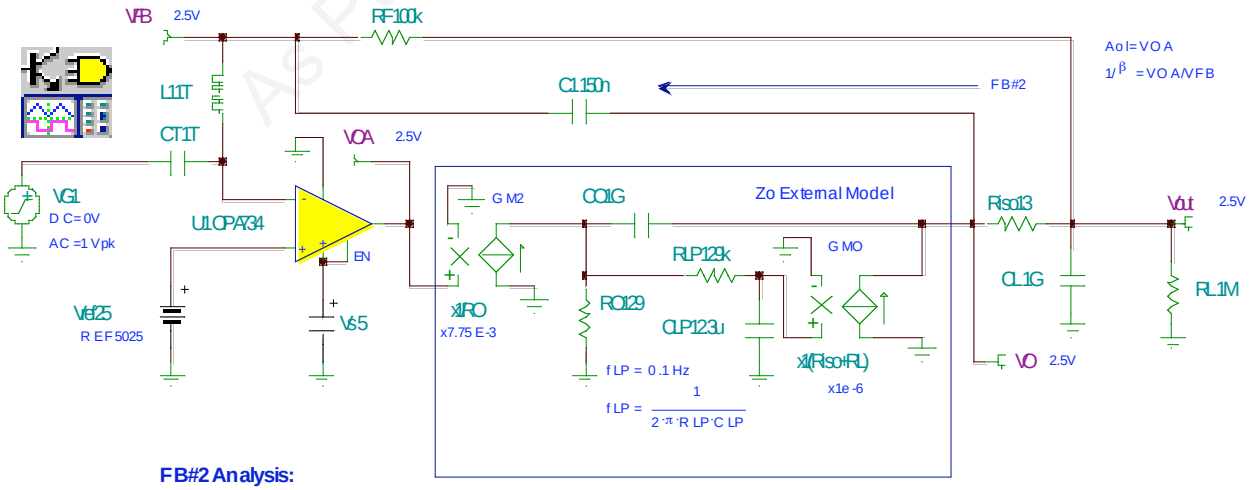


Fig. 10.58: FB#2 Analysis Ac Circuit: CMOS RRO

The results of our TINA-TI simulation(Fig. 10.59) show the FB#2 1/β plot is as predicted by our first-order analysis with fza = 10.6 Hz and a high frequency 1/β of 23.78 dB. We also plot the OP734 Aol curve to see how FB#2 will intersect with it at high frequency.

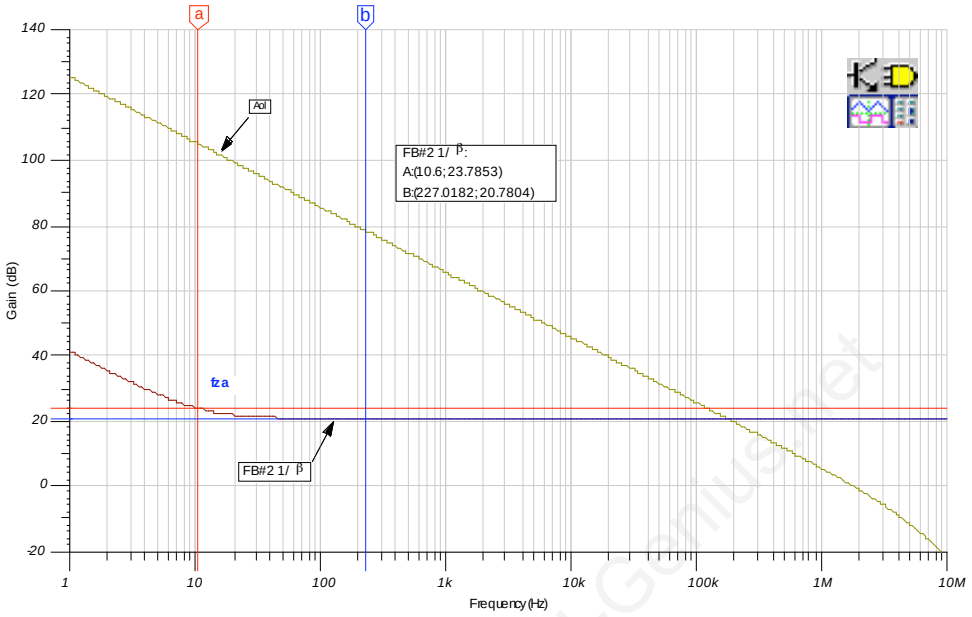


Fig. 10.59: FB#2 1/β Plot: CMOS RRO

We will use the TINA-TI circuit in Fig. 10.60 to analyze if the predicted superposition results of FB#1 and FB#2 will produce the desired net 1/β. It will also allow us to plot Aol, net 1/β and loop gain.

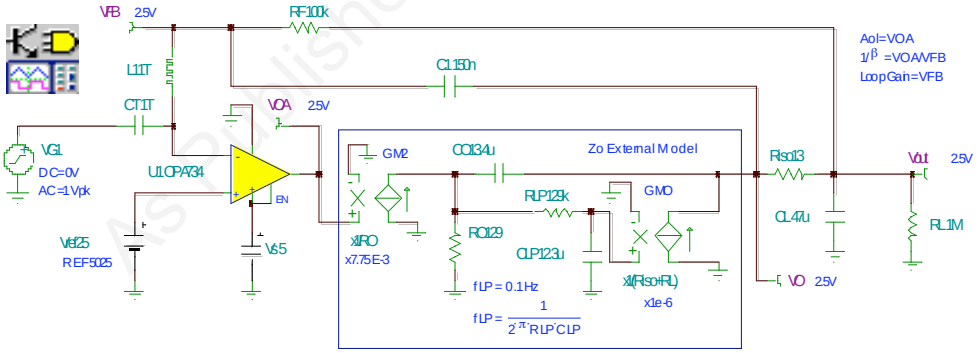


Fig. 10.60: Final Loop-Gain Analysis Circuit: CMOS RRO

We see our analysis results (Fig. 10.61) confirm our predicted net 1/β plot. At fcl, where loop gain goes to zero, we see our expected 20 dB/decade rate-of-closure.

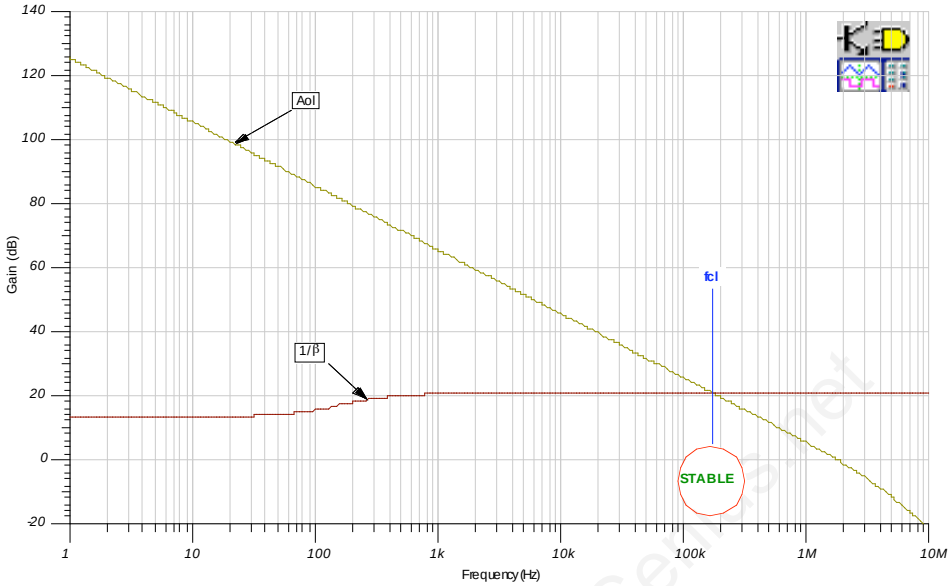


Fig. 10.61: Final Net 1/β: CMOS RRO

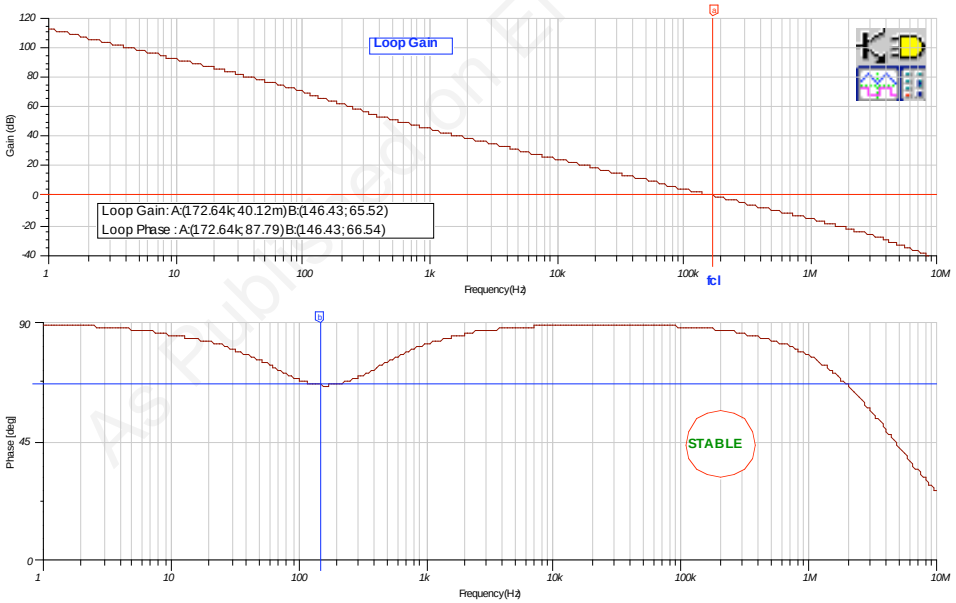


Fig. 10.62: Final Loop-Gain Analysis: CMOS RRO

The loop-gain phase plot for our final circuit, which uses FB#1 and FB#2 (Fig. 10.62) shows phase shift never dips to less than 66.54° (at 146.43 Hz) and at fcl, 172.64 kHz, the phase margin is 87.79°.

We will do our final check on our stabilized circuit with a transient stability test using the TINA-TI circuit of Fig. 10.63.

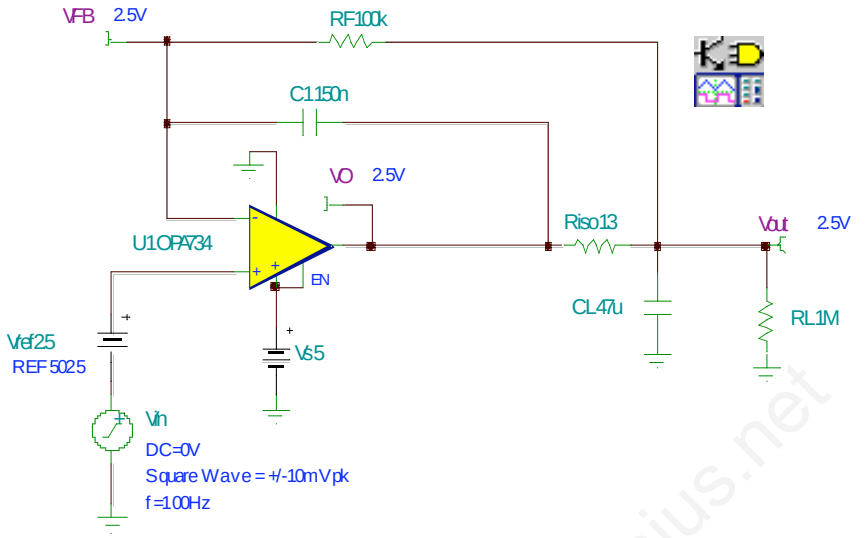


Fig. 10.63: Final Transient Stability Test Circuit: CMOS RRO

The results of our transient stability test on our final circuit (Fig. 10.64) agrees with all of our other predictions resulting in a good, stable circuit we can put into production with confidence that we will not have any failures or real world operation anomalies.

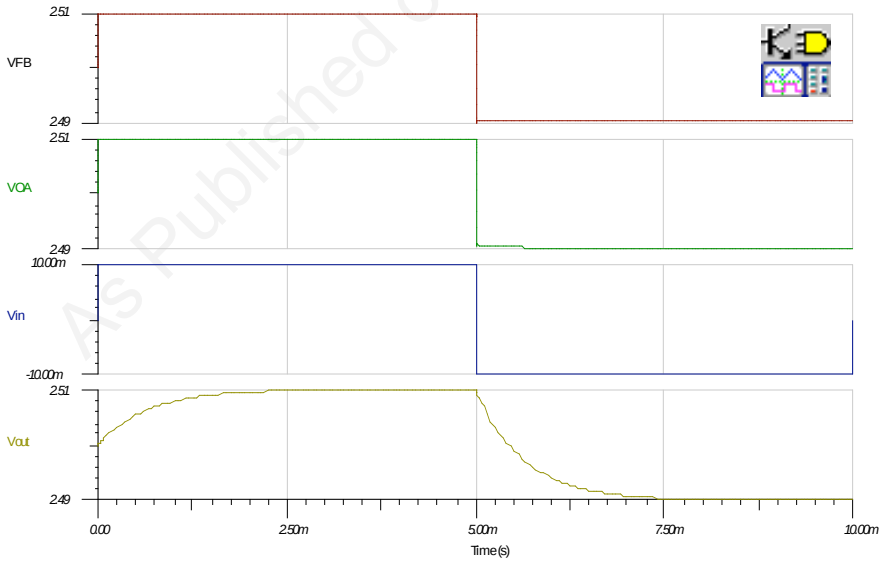


Fig. 10.64: Final Transient Stability Test: CMOS RRO

The TINA-TI circuit of Fig. 10.65 will allow us to confirm if our prediction of Vout/Vin is correct.

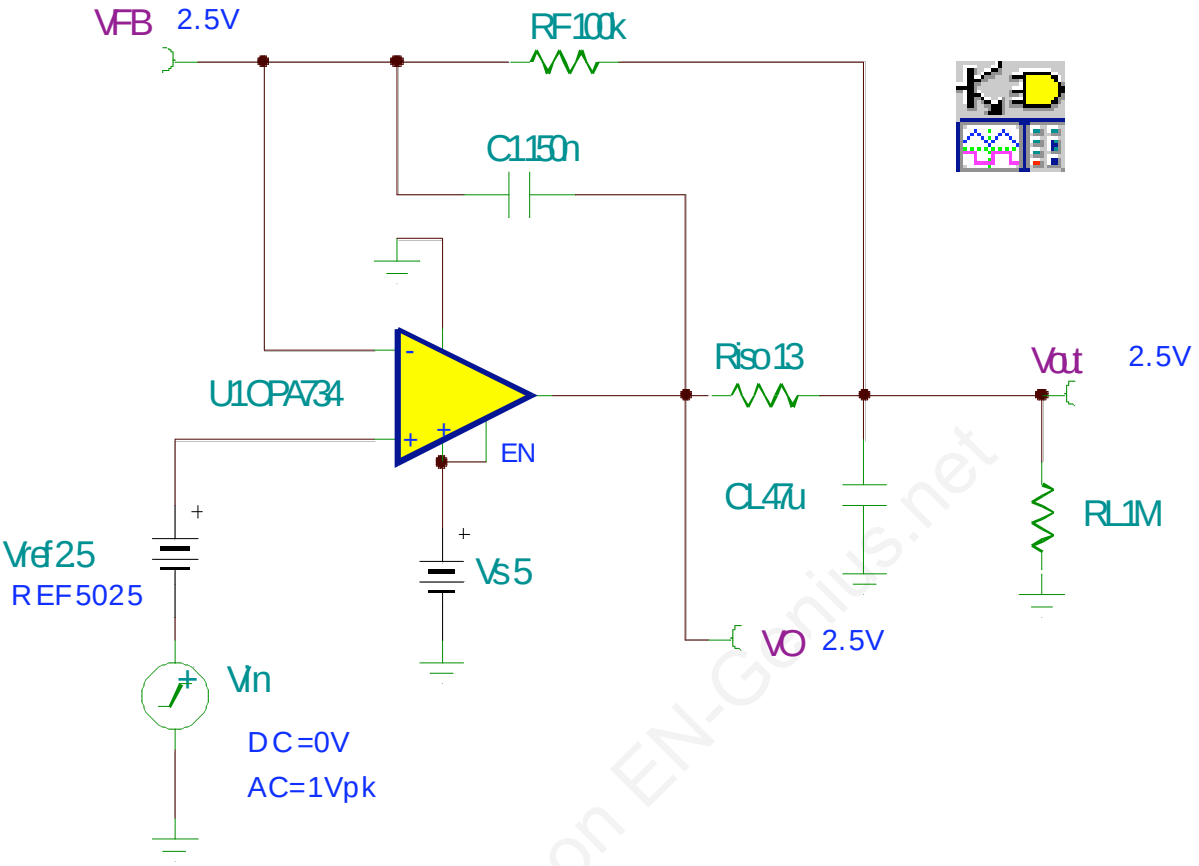


Fig. 10.65: Final Vout/Vin Transfer Function Circuit: CMOS RRO

We see that the results of our Vout/Vin test (Fig. 10.66) match our predicted first-order results with a single pole roll-off at 253.88 Hz and a second at about 167 kHz where FB#2 intersects the Aol curve.

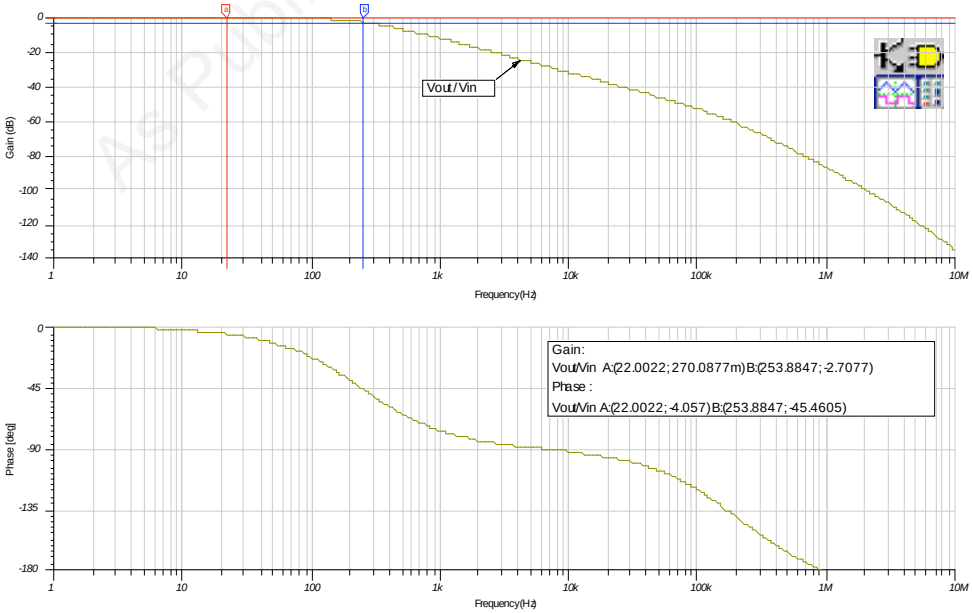


Fig. 10.66: Final Vout/Vin Transfer Function: CMOS RRO

Fig. 10.67 summarizes an easy-to-use step-by-step procedure for the Riso w/Dual Feedback capacitive load stability technique on CMOS RRO output op amps.

FB#1 1/β Formulae:

$$\text{Zero: } fzx = \frac{1}{2\pi \cdot \left(\frac{CO \cdot CL}{CL+CO}\right) \cdot (Riso+RO)}$$

Note: $\frac{CO \cdot CL}{CL+CO}$ is series combination of CO and CL

$$\frac{1}{\beta} = \frac{CL+CO}{CO} \text{ for Low-f } 1/\beta$$

CO and CL form a Capacitive Divider

FB#2 1/β Formulae:

Assume:
CL & CO > 10 ·CF
RF > 10 ·Riso

Pole: At Origin

$$\text{Zero: } fza = \frac{1}{2\pi \cdot RF \cdot CF}$$

High Frequency 1/β:
CO & CL = short
By Inspection:

$$1/\beta = \frac{RO+Riso}{Riso} \text{ for High-f } 1/\beta$$

1. Measure Aol of op amp
2. Measure & Plot Zo of op amp
3. Determine RO
4. Create Zo external model
5. Compute FB#1 Low-f 1/β: equals 1 for unity gain voltage buffer
6. Set FB#2 High-f 1/β = +10 dB higher than FB#1 Low-f 1/β (For best Vout/Vin transient response and least amount of phase shift within loop-gain bandwidth)
7. Choose Riso from FB#2 High-f 1/β and RO
8. Compute FB#1 1/β fzx from CL, Riso, RO
9. Set FB#2 1/β fza = 1/10 fzx
10. Choose RF and CF with practical values to yield fza
11. Run simulation with final values for Aol, 1/β, loop gain, Vout/Vin, transient analysis to confirm design
12. Check for loop-gain Phase shift NOT to dip more than 135° (>45° phase margin)
13. For low noise applications: check for flat Vout/Vin response to avoid gain peaking leading to noise peaking in Vout/Vin

Fig. 10.67: Riso w/Dual Feedback Compensation Procedure: CMOS RRO

About The Author

After earning a BSEE from the University of Arizona, Tim Green has worked as an analog and mixed-signal board/system level design engineer for over 23 years, including brushless motor control, aircraft jet engine control, missile systems, power op amps, data acquisition systems, and CCD cameras. Tim's recent experience includes analog & mixed-signal semiconductor strategic marketing. He is currently the Linear Applications Engineering Manager at Burr-Brown, a division of Texas Instruments, in Tucson, AZ and focuses on instrumentation amplifiers and digitally-programmable analog conditioning ICs. He can be contacted at green_tim@ti.com