**AFE4300 FAQ**

1. What is the calibration procedure for the AFE4300?

There is an application report on 'Impedance Measurement with [AFE4300](http://www.ti.com/product/AFE4300)' which explains how to enable calibration block on [AFE4300](http://www.ti.com/product/AFE4300) GUI and perform calibration. The link is included below.

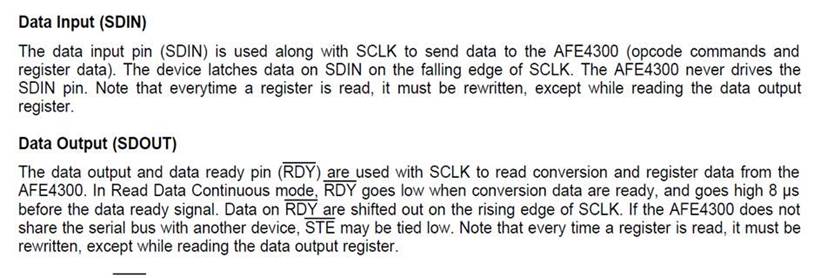
[7215.SBAA202-17Jan.pdf](http://e2e.ti.com/cfs-file.ashx/__key/communityserver-discussions-components-files/30/7215.SBAA202_2D00_17Jan.pdf)

1. How do I request the firmware for the AFE4300?

We have posted our firmware on our product folder. Link below

<http://www.ti.com/product/AFE4300/toolssoftware#softTools>

1. Can you explain what is meant by the following paragraphs in the datasheet? How do I have to read the registers?



This means that anytime you read a register (except the data out register) you must then write back what was just read. It basically works like a destructive read.

1. Is there any information to show how body composition is calculated?

Here are some links to academic papers/articles:

<http://digitalcommons.wku.edu/ijes/vol4/iss3/2/>

<http://ajcn.nutrition.org/content/64/3/388S.full.pdf>

<http://jap.physiology.org/content/jap/60/4/1327.full.pdf>

1. Are there any recommendations on how to implement patient protection with the AFE4300?

Our datasheet gives a functional block diagram on the first page to show where the Patient & ESD protection block is located. For our EVM, protection is provided through the 1uF capacitors.

Make sure IEC standards are followed.

You will also need to make sure your calibration routine is accurate.

1. What is the accuracy measurement when using 250 kHz (maximum attainable frequency) and 80 kHz as the source signal frequency?

There is a low-pass filter after the DAC with a cutoff frequency of 150 kHz +/- 30 kHz. So, to keep the signal from attenuating we made the max excitation frequency to be 80 kHz.

After calibration you can get an accuracy of 1%.

1. With Calibration of FWR Mode is appears that the reference resistors run through RP1 and RN1 through the resistor R57 which is labelled in the AFE4300 User Development Guide as 10KOhms. The "Impedance Measurement with the AFE4300" document on page 6 shows that R57 is 950Ohms and also after measuring it the resistance was 950Ohms. Was the 10KOhm label a typo of some sort?

10kOhms is the actual value of the resistor that is placed in that position. The 950Ohms is the effective resistance in that position since there are other resistances in the circuit that affect it.

1. Why is the accuracy off when using IQ mode?

**Issue Background:** During the normal operation in IQ mode, if BCM DAC frequency or if IQ demod clock divider is changed and then again brought back to initial value, the ADC output observed for a given impedance would be different than the initial observation.

**Cause:** The DAC frequency generator DDS is initialized on the register update of the DAC frequency register. The IQ demod clock divider is also updated on the divider register value. The DAC frequency and IQ demod clock divider values are also changed during reset. Since these are written by SPI that is asynchronous to the device clock, every time the DAC frequency or the divider is written, there is no definite relation between them and hence they can start with different phase relations between them which is dependent on how the divider starts (for example for div by 2, 2 phases are possible, div by 4, 4 phases are possible and so on). So though sqrt(I^2 + Q^2) will be same, individual I and Q measurements might be different as I, Q are the DAC frequency being demodulated with respect to the demodulator clock phase relationship.

**Design:** The DAC frequency generator (DDS) initializes the phase of the DAC waveform whenever there is change in the DAC frequency register values. The next device clock after the register value change, the DDS initializes and starts the new waveform.

The IQ DEMOD Clock divider is reset on global reset pin and the default is Div by 1. Later whenever there is an update in the divider value register, the divider clock initializes and starts with a fixed phase.

**Solution:** Have the SPI clock synchronous with the device clock of 1MHz which is possible in the system as there will be a central microcontroller that will have a global source clock which will be used for the device and the SPI with different dividers.

Follow the sequence below to ensure that there is definite relation between the DAC frequency generator and the Demodulator divider clock to ensure repeatable value.

**Sequence to be followed to avoid this issue:** If during normal operation DACOUT freq. is to be changed, the following steps ensure proper operation:

1.) Write 0 to Reg.15 (Making IQ divider as 1)

2.) Write 0 to Reg. 14 (DACOUT freq. is cleared)

3.) Write required DAC freq. to Reg.14

4.) Write required IQ\_DEMOD\_CLK\_DIV to Reg.15

**Please Note the Following:**

- The SPI SCLK must be Sync’ed to the 1MHz clock which is fed as CLKIN to AFE4300.

- With asynchronous SCLK the above mentioned sequence may not work as intended.

- Even after Device RST, it is recommended to follow above sequence to configure DACOUT and IQ divider

- This sequence is not required in FWR mode