Octal-Channel 12-Bit 80-MSPS and Low-Power ADC

1 FEATURES

- Maximum Sample Rate: 80 MSPS/12-Bit
- High Signal-to-Noise Ratio
  - 70-dBFS SNR at 5 MHz/80 MSPS
  - 71.5-dBFS SNR at 5 MHz/80 MSPS and Decimation Filter = 2
  - 85-dBc SFDR at 5 MHz/80 MSPS
- Low Power Consumption
  - 48 mW/CH at 50 MSPS
  - 54 mW/CH at 65 MSPS
  - 66 mW/CH at 80 MSPS (2 LVDS Wire Per Channel)
- Digital Processing Block
  - Programmable FIR Decimation Filter and Oversampling to Minimize Harmonic Interference
  - Programmable IIR High-Pass Filter to Minimize DC Offset
  - Programmable Digital Gain: 0 dB to 12 dB
  - 2- or 4-Channel Averaging
- Flexible Serialized LVDS Outputs:
  - One or Two wires of LVDS Output Lines per Channel Depending on ADC Sampling Rate
  - Programmable Mapping Between ADC Input Channels and LVDS Output Pins-Eases Board Design
  - Variety of Test Patterns to Verify Data Capture by FPGA/Receiver
- Internal and External References
- 1.8-V Operation for Low Power Consumption
- Low-Frequency Noise Suppression
- Recovery From 6-dB Overload within 1 Clock Cycle
- Package: 12-mm × 12-mm 80-Pin QFP

2 APPLICATIONS

- Ultrasound Imaging
- Communication Applications
- Multi-channel Data Acquisition

3 DESCRIPTION

Using CMOS process technology and innovative circuit techniques, the ADS5292 is a low-power 80-MSPS 8-Channel ADC. Low power consumption, high SNR, low SFDR, and consistent overload recovery allow users to design high performance systems.

The ADS5292 has a digital processing block that integrates several commonly used digital functions for improving system performance. The device includes a digital filter module that has built-in decimation filters (with low-pass, high-pass and band-pass characteristics). The decimation rate is also programmable (by 2, by 4, or by 8) which makes the device useful for narrow-band applications, where the filters are conveniently used to improve SNR and knock-off harmonics, while at the same time reducing the output data rate. The device includes an averaging mode where two channels (or even four channels) are averaged to improve SNR.

Serial LVDS outputs reduce the number of interface lines and enable the highest system integration. The digital data from each channel ADC is output over one or two wires of LVDS output lines depending on the ADC sampling rate. This 2-wire interface maintains a low serial data rate, allowing low-cost FPGA based receivers to be used even at high sample rate. A unique feature is the programmable mapping module that allows flexible mapping between the input channels and the LVDS output pins. This module greatly reduces the complexity of LVDS output routing which potentially results in cheaper system boards by reducing the number of PCB layers.

The device integrates an internal reference trimmed to accurately match across devices. The internal reference mode achieves the best performance, however, external references can also drive the device.

The device is available in a 12-mm × 12-mm 80-pin QFP. The device is specified over a –40°C to 85°C operating temperature range. The ADS5292 is completely pin-to-pin and register compatible to ADS5294.

3.1 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

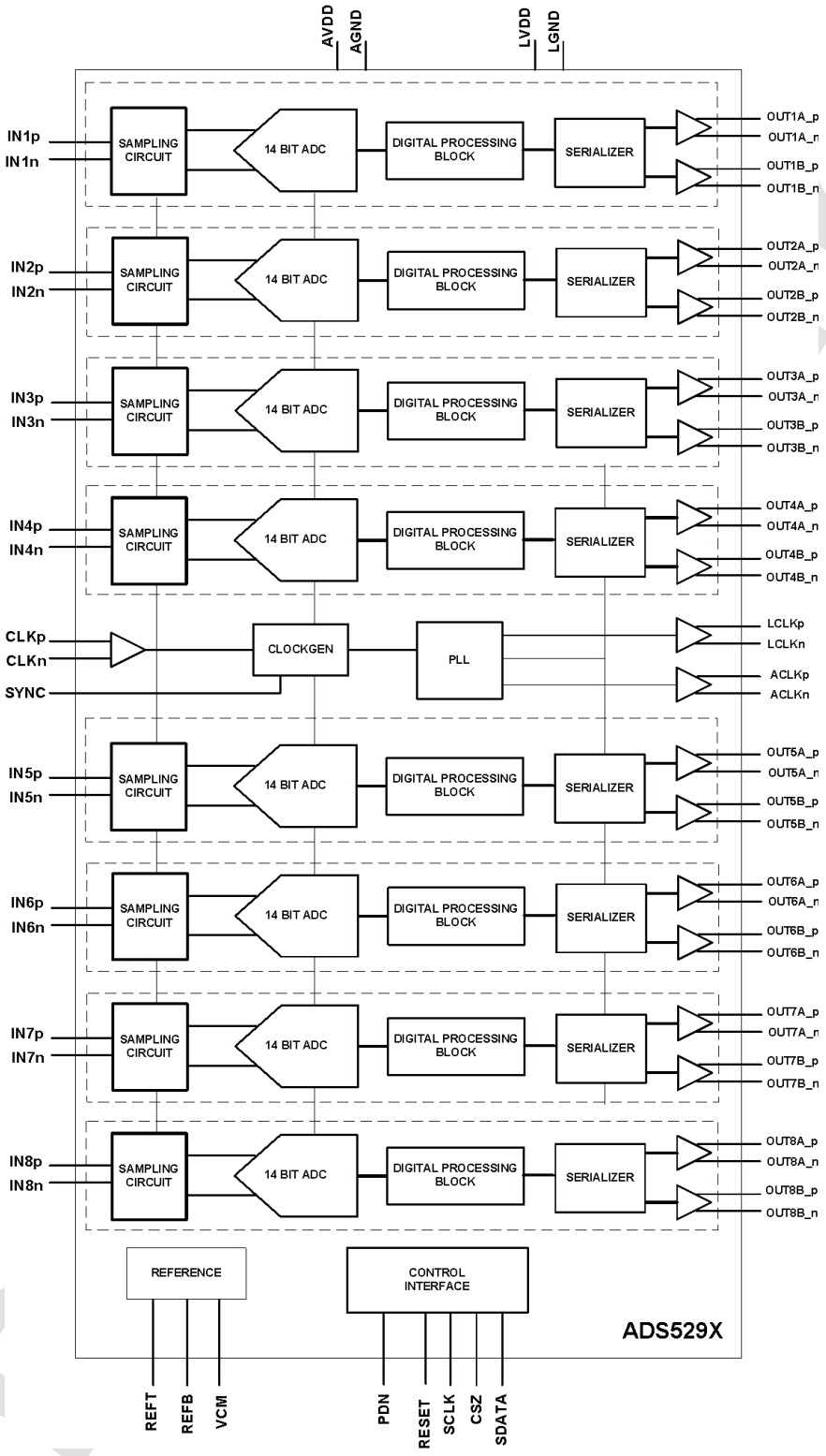
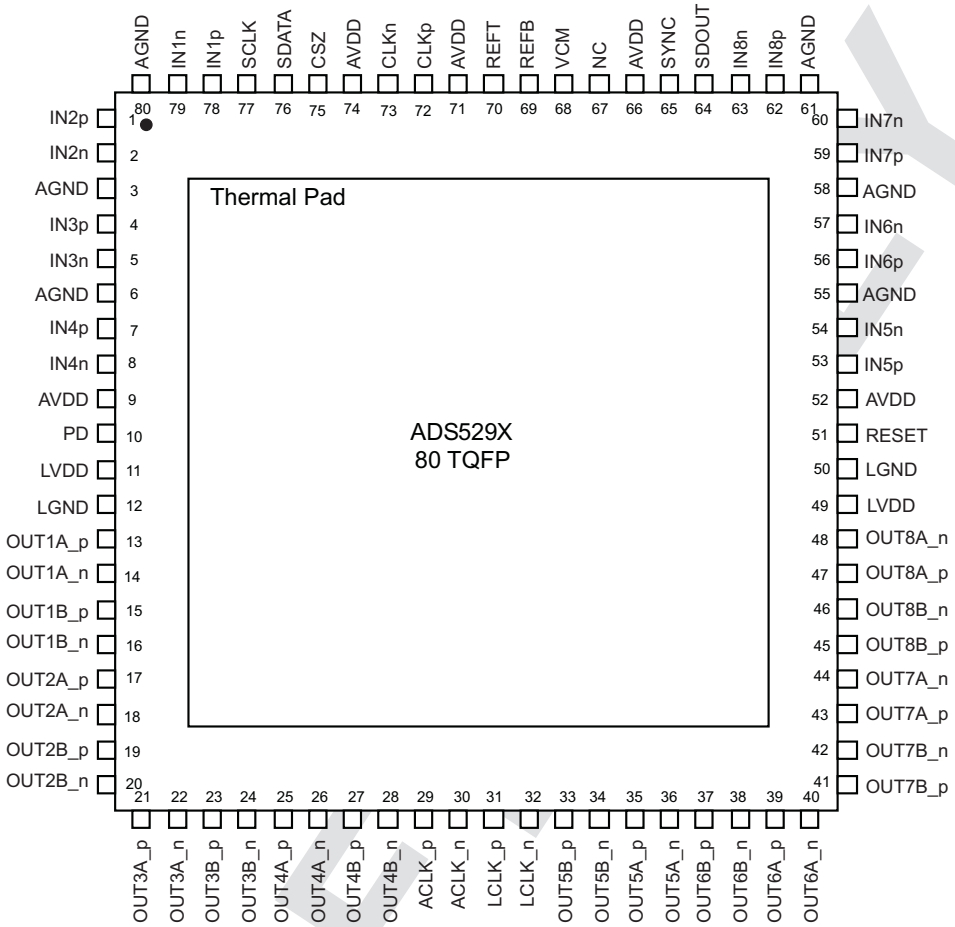


Figure 1. Block Diagram

4 PIN CONFIGURATION

80-PIN TQFP WITH THERMAL PAD
PFP PACKAGE (TOP VIEW)



PIN FUNCTIONS

NUMBER OF PINS	PIN		DESCRIPTION
	NAME	NUMBER	
5	AVDD	9, 52, 66, 71, 74	Analog power supply, 1.8 V
6	AGND	3, 6, 55, 58, 61, 80	Analog ground
2	LVDD	11, 49	Digital and I/O power supply, 1.8 V
2	LGND	12, 50	Digital ground
1	CLKN	73	Negative differential clock — Tie CLKN to GND for single-ended clock
1	CLKP	72	Positive differential clock
2	LCLKP, LCLKN	31, 32	Differential LVDS bit clock (7X)
2	ACLKP, ACLKN	29, 30	Differential LVDS frame clock (1X)
2	IN1P, IN1N	78, 79	Differential input signal, Channel 1
2	IN2P, IN2N	1, 2	Differential input signal, Channel 2
2	IN3P, IN3N	4, 5	Differential input signal, Channel 3
2	IN4P, IN4N	7, 8	Differential input signal, Channel 4
2	IN5P, IN5N	53, 54	Differential input signal, Channel 5
2	IN6P, IN6N	56, 57	Differential input signal, Channel 6
2	IN7P, IN7N	59, 60	Differential input signal, Channel 7
2	IN8P, IN8N	62, 63	Differential input signal, Channel 8
2	OUT1A_P, OUT1A_N	13, 14	Differential LVDS data output, wire 1, channel 1

PIN FUNCTIONS (continued)

NUMBER OF PINS	PIN		DESCRIPTION
	NAME	NUMBER	
2	OUT1B_P, OUT1B_N	15, 16	Differential LVDS data output, wire 2, channel 1
2	OUT2A_P, OUT2A_N	17, 18	Differential LVDS data output, wire 1, channel 2
2	OUT2B_P, OUT2B_N	19, 20	Differential LVDS data output, wire 2, channel 2
2	OUT3A_P, OUT3A_N	21, 22	Differential LVDS data output, wire 1, channel 3
2	OUT3B_P, OUT3B_N	23, 24	Differential LVDS data output, wire 2, channel 3
2	OUT4A_P, OUT4A_N	25, 26	Differential LVDS data output, wire 1, channel 4
2	OUT4B_P, OUT4B_N	27, 28	Differential LVDS data output, wire 2, channel 4
2	OUT5A_P, OUT5A_N	35, 36	Differential LVDS data output, wire 1, channel 5
2	OUT5B_P, OUT5B_N	33, 34	Differential LVDS data output, wire 2, channel 5
2	OUT6A_P, OUT6A_N	39, 40	Differential LVDS data output, wire 1, channel 6
2	OUT6B_P, OUT6B_N	37, 38	Differential LVDS data output, wire 2, channel 6
2	OUT7A_P, OUT7A_N	43, 44	Differential LVDS data output, wire 1, channel 7
2	OUT7B_P, OUT7B_N	41, 42	Differential LVDS data output, wire 2, channel 7
2	OUT8A_P, OUT8A_N	47, 48	Differential LVDS data output, wire 1, channel 8
2	OUT8B_P, OUT8B_N	45, 46	Differential LVDS data output, wire 2, channel 8
1	PD	10	Power down control input. Active High. The pin has an internal 220-kΩ pulldown resistor.
1	REFB	69	Negative reference input/ output. Internal reference mode: Reference bottom voltage (0.45 V) is output on this pin. A decoupling capacitor is not required on this pin. External reference mode: Reference bottom voltage (0.45 V) must be externally applied to this pin. Please see External Reference Mode of Operation.
1	REFT	70	Positive reference input/ output. Internal reference mode: Reference top voltage (1.45 V) is output on this pin. A decoupling capacitor is not required on this pin. External reference mode: Reference top voltage (1.45 V) must be externally applied to this pin. Please see External Reference Mode of Operation.
1	VCM	68	Common-mode output pin, 0.95-V output. This pin can be configured as the external reference voltage (1.5 V) input pin as well. See Reg 0x42 and External Reference Mode of Operation.
1	RESET	51	Active HIGH RESET input. The pin has an internal 220-kΩ pulldown resistor.
1	SCLK	77	Serial clock input. The pin has an internal 220-kΩ pulldown resistor.
1	SDATA	76	Serial data input. The pin has an internal 220-kΩ pulldown resistor.
1	SDOUT	64	Serial data readout. This pin is in the high-impedance state after reset. When the <READOUT> bit is set, the SDOUT pin becomes active. This is a CMOS digital output running from the AVDD supply.
1	CSZ	75	Serial enable chip select — active-low digital input
1	SYNC	65	Input signal to synchronize channels and chips when used with reduced output data rates. If SYNC is not used, add a ≤10-KΩ pulldown resistor.
1	NC	67	No Connection. Must leave floated

4.1 ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	AVDD	–0.3	2.2	V
	LVDD	–0.3	2.2	V
Voltage	between AGND and LGND	–0.3	0.3	V
	at analog inputs	–0.3	min[2.2, AVDD+0.3]	V
	at digital inputs, CLKN, CLKP(2), RESET, SCLK, SDATA, CSZ	–0.3	3.6	V
	at digital outputs	–0.3	min[2.2,LVDD+0.3]	V
Maximum junction temperature (T_J), any condition			105	°C
Storage temperature range		–55	150	°C
Operating temperature range		–40	85	°C
ESD Ratings	Human Body Model (HBM)		2000	V
	Charged Device Model (CDM)		500	V

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) When AVDD is turned off, TI recommends to switch off the input clock (or ensure the voltage on CLKP, CLKN is < |0.3 V|. This prevents the ESD protection diodes at the clock input pins from turning on.

4.2 THERMAL INFORMATION

THERMAL METRIC(1)		ADS5292	UNITS
		PFP (80 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	30.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	6.3	
θ_{JB}	Junction-to-board thermal resistance	8.3	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	8.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

4.3 RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
LVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS / OUTPUTS						
	Differential input voltage range			2		V_{PP}
	Input common-mode voltage			0.95±0.05		V
REF_T	External reference mode			1.45		V
REF_B	External reference mode			0.45		V
VCM	External Reference mode Input			1.5		V
	Common-mode voltage output			0.95		V
	Maximum Input Frequency (1)	2 V_{PP} amplitude		80		MHz
CLOCK INPUTS						
	ADC Clock input sample rate		10		80	MSPS
	Input Clock amplitude differential ($V_{(CLKP)}$ – $V_{(CLKN)}$) peak-to-peak	Sine wave, AC-coupled	0.2	1.5		V_{PP}
		LVPECL, AC-coupled	0.2	1.6		
		LVDS, AC-coupled	0.2	0.7		
V_{IL}	Input Clock CMOS single-ended ($V_{(CLKP)}$)			<0.3		V
V_{IH}				>1.5		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
	ACLKP and ACLKN outputs (LVDS), 1-wire interface			1x (sample rate)		MSPS
	LCLKP and LCLKN outputs (LVDS), 1-wire interface			6x (sample rate)		MSPS
	ACLKP and ACLKN outputs (LVDS), 2-wire interface			0.5x (sample rate)		MSPS
	LCLKP and LCLKN outputs (LVDS), 2-wire interface			3x (sample rate)		MSPS
	Maximum data rate, 2-wire interface			480		MBPS
	Maximum data rate, 1-wire interface			960		MBPS
C_{LOAD}	Maximum external capacitance from each output pin to LGND			5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs			100		Ω
T_A	Operating free-air temperature		–40		85	°C

(1) See the Large and Small Signal Input Bandwidth section.

4.4 ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12-Bit/80-MSPS, ADC is configured in internal reference mode (unless otherwise noted). MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.8 V.

PARAMETERS		CONDITIONS		MIN	TYP	MAX	UNITS
AC PERFORMANCE							
SNR	Signal-to-noise ratio	f_{in} = 5 MHz, 80 MSPS. 14-bits mode(1)			72		dBFS
		f_{in} = 5 MHz, 80 MSPS		67.5	70		
		f_{in} = 30 MHz, 80 MSPS			69.8		
		f_{in} = 5 MHz, 80 MSPS, Decimation filter=2			71.5		
SINAD	Signal-to-noise and distortion ratio	f_{in} = 5 MHz, 80 MSPS			69.8		dBFS
		f_{in} = 30 MHz, 80 MSPS			69.3		
ENOB	Effective number of bits	f_{in} = 5 MHz			11.3		LSB
DNL	Differential nonlinearity	f_{in} = 5 MHz		–0.8	±0.05	0.8	LSB
INL	Integral nonlinearity	f_{in} = 5 MHz			0.4	1	LSB
SFDR	Spurious-free dynamic range	f_{in} = 5 MHz		72.5	85		dBc
		f_{in} = 30 MHz			80		
THD	Total harmonic distortion	f_{in} = 5 MHz		71	81.5		dBc
		f_{in} = 30 MHz			78		
HD2	Second-harmonic distortion	f_{in} = 5 MHz		72.5	88		dBc
		f_{in} = 30 MHz			80		
HD3	Third-harmonic distortion	f_{in} = 5 MHz		72.5	85		dBc
		f_{in} = 30 MHz			78.5		
	Worst spur excluding HD2, HD3	f_{in} = 5 MHz			91		dBc
		f_{in} = 30 MHz			83		
		f_{in} = 65 MHz			76		
IMD3	Intermodualtion distortion	f_{in} = 5 MHz at –7 dBFS, f_2 = 10 MHz at –7 dBFS			82		dBc
	Overload recovery	Recovery to within 1% of full scale value for 6-dB overload with sine wave input			1		Clock Cycle
XTALK	Cross-talk	f_{in} = 10 MHz; V_{OUT} = –1 dBFS signal applied on aggressor channel no signal applied on victim channel	far channel		90		dB
			near channel		85		
	Phase noise	5 MHz, 1 kHz off carrier			–138		dBc/Hz
ANALOG INPUT/OUTPUT							
	Differential input voltage range (0-dB gain)				2		Vpp
Rin	Differential Input Resistance	At DC			2		kΩ
Cin	Differential Input Capacitance	At DC			2.2		pF
	Analog input bandwidth	With a 50-Ω source impedance			550		MHz
	Analog input common-mode current (per input pin)				1.6		µA/MSPS
	VCM common-mode output voltage				0.95		V
	VCM output current capability				5		mA
DC ACCURACY							
	Offset error	Across devices and across channels within a device		–20		20	mV
	Temperature coefficient of offset error				<0.01		mV/°C
E_{GREF}	Gain error due to internal reference inaccuracy alone			–2		2	%FS
E_{GCHAN}	Gain error of channel alone				0.5		%FS
	Temperature coefficent of E_{GCHAN}				<0.01		%FS/°C

(1) 14-bit SNR is ensured by design and characterization and not tested in production.

ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12-Bit/80-MSPS, ADC is configured in internal reference mode (unless otherwise noted). MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.8 V.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY					
Power consumption	80 MSPS/12 Bit, 2-wire LVDS		66		mW/CH
	50 MSPS/12 Bit, 1-wire LVDS		48		
	40 MSPS/12 Bit, 1-wire LVDS		43		
	80 MSPS/12 Bit, 1-wire decimation filter = 2, 1-wire LVDS		87		
AVDD	80 MSPS, 12 Bit		182	206	mA
	65 MSPS, 12 Bit		162		
	40 MSPS, 12 Bit		130		
LVDD	80 MSPS/12 Bit, 2-wire LVDS		112	125	mA
	50 MSPS/12 Bit,1-wire LVDS		67		
	40 MSPS/12 Bit,1-wire LVDS		61		
	80 MSPS/12 Bit, Decimation filter = 2, 1-wire LVDS		198		
Power-down power consumption	Partial power down, 80 MHz, 2-wire LVDS		175		mW
	Complete power down			50	
Power supply modulation ratio	Carrier = 5 MHz, f_N = 10 kHz at 50 mV_{PP} signal on AVDD		30		dBc
Power supply rejection ratio	AC power supply rejection ratio f = 10 kHz		55		dBc

4.5 DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 1.8 V, LVDD = 1.8 V

PARAMETERS		CONDITION	MIN	TYP	MAX	UNITS
DIGITAL INPUTS/OUTPUTS						
V_{IH}	Logic-high input voltage	All digital inputs support 1.8-V and 3.3-V CMOS logic levels.	1.3			V
V_{IL}	Logic-low input voltage				0.4	V
I_{IH}	Logic-high input current	V_{HIGH} = 1.8 V		6		µA
I_{IL}	Logic-low input current	V_{LOW} = 0 V		<0.1		µA
V_{OH}	Logic-high output voltage		AVDD-0.1			V
V_{OL}	Logic-low output voltage			0.2		V
LVDS OUTPUTS						
V_{ODH}	High-level output differential voltage	100-Ω external termination	240	350	405	mV
V_{ODL}	Low-level output differential voltage	100-Ω external termination	–240	–350	–405	mV
V_{OCM}	Output common-mode voltage		900	1100	1300	mV

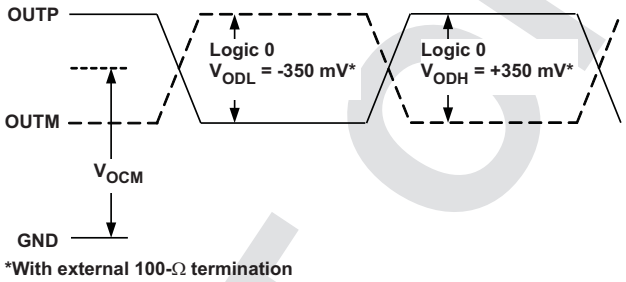


Figure 2. LVDS Output Voltage Levels

4.6 TIMING REQUIREMENTS(1)(2)(3)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, sampling frequency = 80-MSPS, 12-bit, sine-wave input clock = 1.5-Vpp clock amplitude, C_{LOAD} = 5 pF, R_{LOAD} = 100 Ω, unless otherwise noted. MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.7 V to 1.9 V.

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
t_a	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs		4		ns
	Aperture delay variation	Across channels within the same device		±175		ps
		Across devices at same temperature and LVDD supply voltage		2.5		ns
t_j	Aperture jitter RMS			320		fs rms
t_d	Data latency	1-wire LVDS output interface		11		Clock cycles
		2-wire LVDS output interface		15		Clock cycles
t_{SU}	Data setup time	80-MSPS, 2 wire LVDS, 6x-serialization	0.25	0.63		ns
t_H	Data hold time	80-MSPS, 2 wire LVDS, 6x-serialization	0.65	1		ns
t_{PROG}	Clock propagation delay	Input clock rising edge(zero cross) to frame clock rising edge(zero cross)		See Table 1 and Table 2		ns
	Variation of t_{PROG}	Between two devices under the same conditions		±0.75		ns
	LVDS bit clock duty cycle			50%		
	Bit clock cycle-to-cycle jitter			40		ps rms
	Frame clock cycle-to-cycle jitter			70		ps rms
t_{RISE}	Data rise time	Rise time is from –100 mV to +100 mV		0.2		ns
t_{FALL}	Data fall time	Fall time is from +100 mV to –100 mV		0.2		ns
$t_{CLKRISE}$	Output clock rise time	Rise time is from –100 mV to +100 mV		0.18		ns
$t_{CLKFALL}$	Output clock fall time	Fall time is from +100 mV to –100 mV		0.16		ns
t_{WAKE}	Wake-up Time	Time to valid data after coming out of COMPLETE POWER-DOWN mode		100		µs
		Time to valid data after coming out of PARTIAL POWER-DOWN mode (with clock continuing to run during power-down)		5		µs

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(3) Data valid refers to logic HIGH of 100 mV and logic LOW of –100 mV.

Table 1. LVDS Timing at Different Sampling Frequencies — 2-Wire Interface, 6x-Serialization (12-bit Output Resolution) , Digital Filter Disabled(1)

ADC CLK Frequency (MSPS)	Setup Time (t_{su}), ns			Hold Time (t_H), ns			t_{PROG} = (11/12) × T + t_{delay}, ns(2)		
Fs (1/T)	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			t_{PROG} = delay from Input clock zero-cross rising edge to frame clock zero cross rising edge		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	0.25	0.63		0.65	1			8.6	
65	0.42	0.8		1	1.3			8.6	
50	0.85	1.1		1.4	1.7			8.6	
40	1.2	1.5		1.8	2.1			8.6	
30	2.1	2.4		2.3	2.6			8.6	
20	3.5	3.8		3.7	4			8.6	
10	7.7	8		7.8	8.4			8.6	

(1) Bit-clock and Frame-clock jitter is included in the setup and hold timing.
(2) Values below correspond to t_{delay}, NOT t_{PROG}

Table 2. LVDS Timing at Different Sampling Frequencies - 1-Wire Interface, 12x Serialization (12-bit Output Resolution), Digital Filter Disabled(1)

ADC CLK Frequency (MSPS)	Setup Time (t_{su}), ns			Hold Time (t_H), ns			t_{PROG} = (9/12) × T + t_{delay}, ns (2)		
Fs (1/T)	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			t_{PROG} = delay from Input clock zero-cross rising edge to frame clock zero cross rising edge)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	0.22	0.35		0.21	0.38			9	
50	0.38	0.6		0.45	0.6			9	
40	0.4	0.7		0.7	1			9	
25	1	1.3		1.4	1.7			9	
10	3.6	3.9		3.7	4			9	

(1) Bit-clock and Frame-clock jitter is included in the setup and hold timing.
(2) Values below correspond to t_{delay}, NOT t_{PROG}

NOTE

For Fs>=65MSPS, 2-wire mode is recommended.

The above LVDS timing specification is only valid when digital decimation filters are disabled. When digital filters are enabled, the setup time decreases as the corresponding hold time increases as shown in Table 1 to Table 2. The change on LVDS timing also depends on the internal PLL setting of the ADS5292. See PLL Operation Versus LVDS Timing for more information.

At the highest sampling frequency, 80-MSPS, and decimation of 2 (for example: effective data rate = 560-Mbps in one-wire mode), the setup time is reduced by 70 ps, (for example: setup time, min = 0.43 ns hold time, min = 0.54 ns). This scenario assumes that the recommended PLL settings are configured as shown in PLL Operation Versus LVDS Timing.

5 LVDS TIMING DIAGRAM

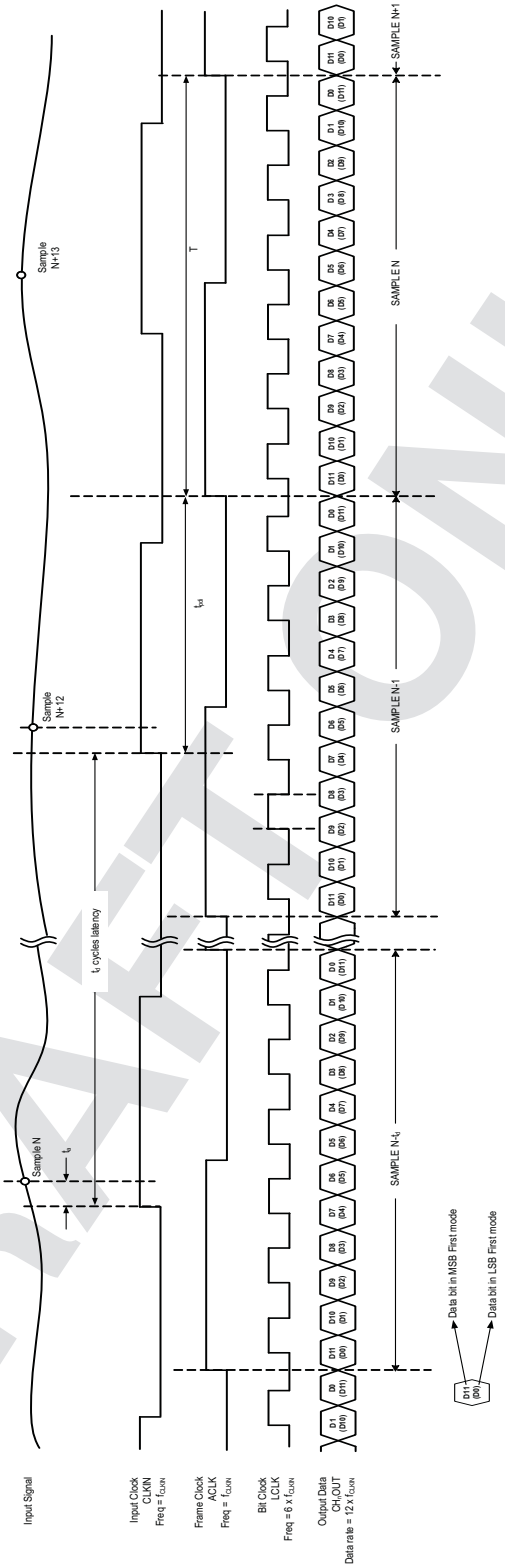


Figure 3. 12-bit 2-wire LVDS Timing Diagram

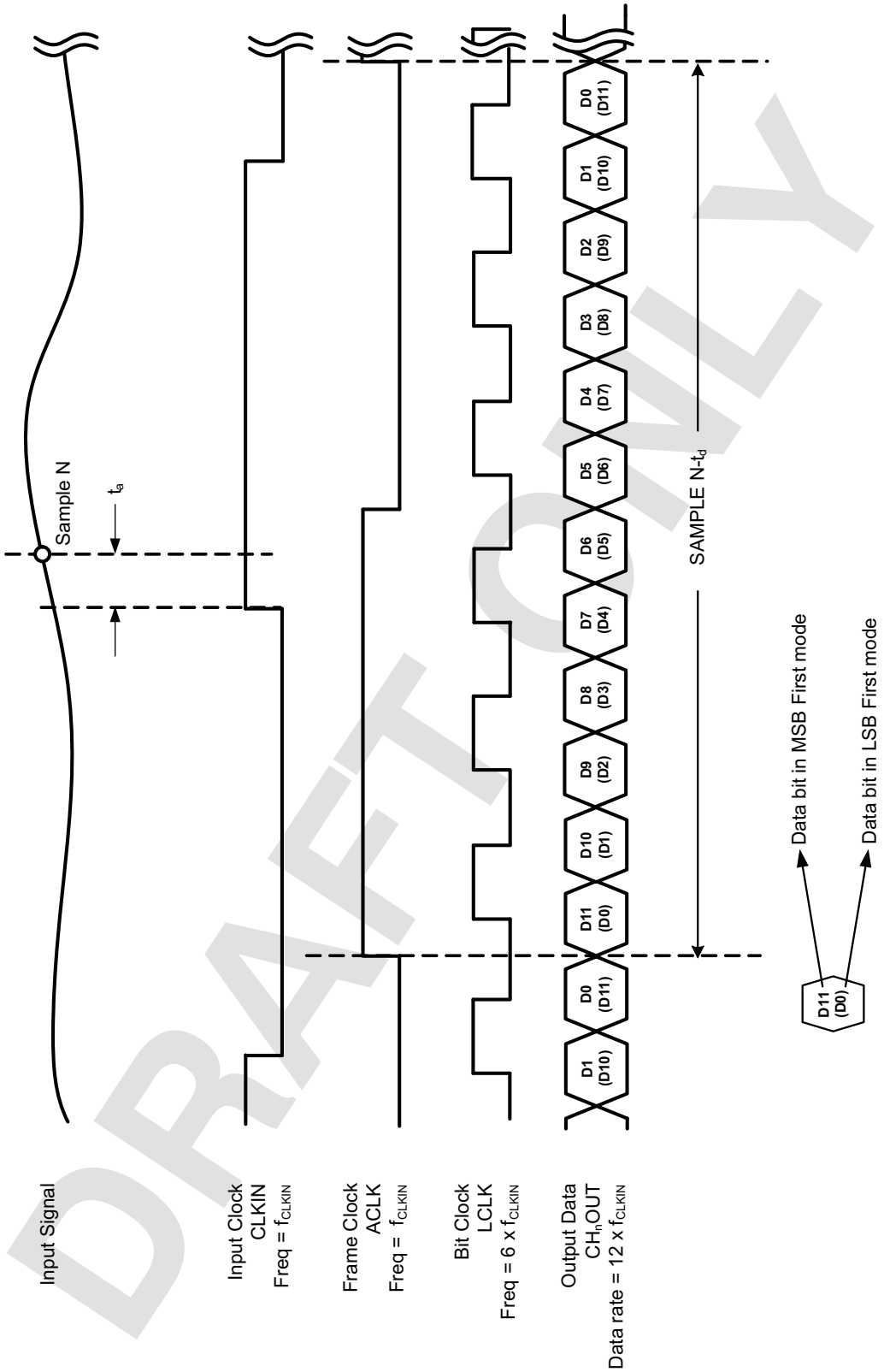


Figure 4. Timing Diagram

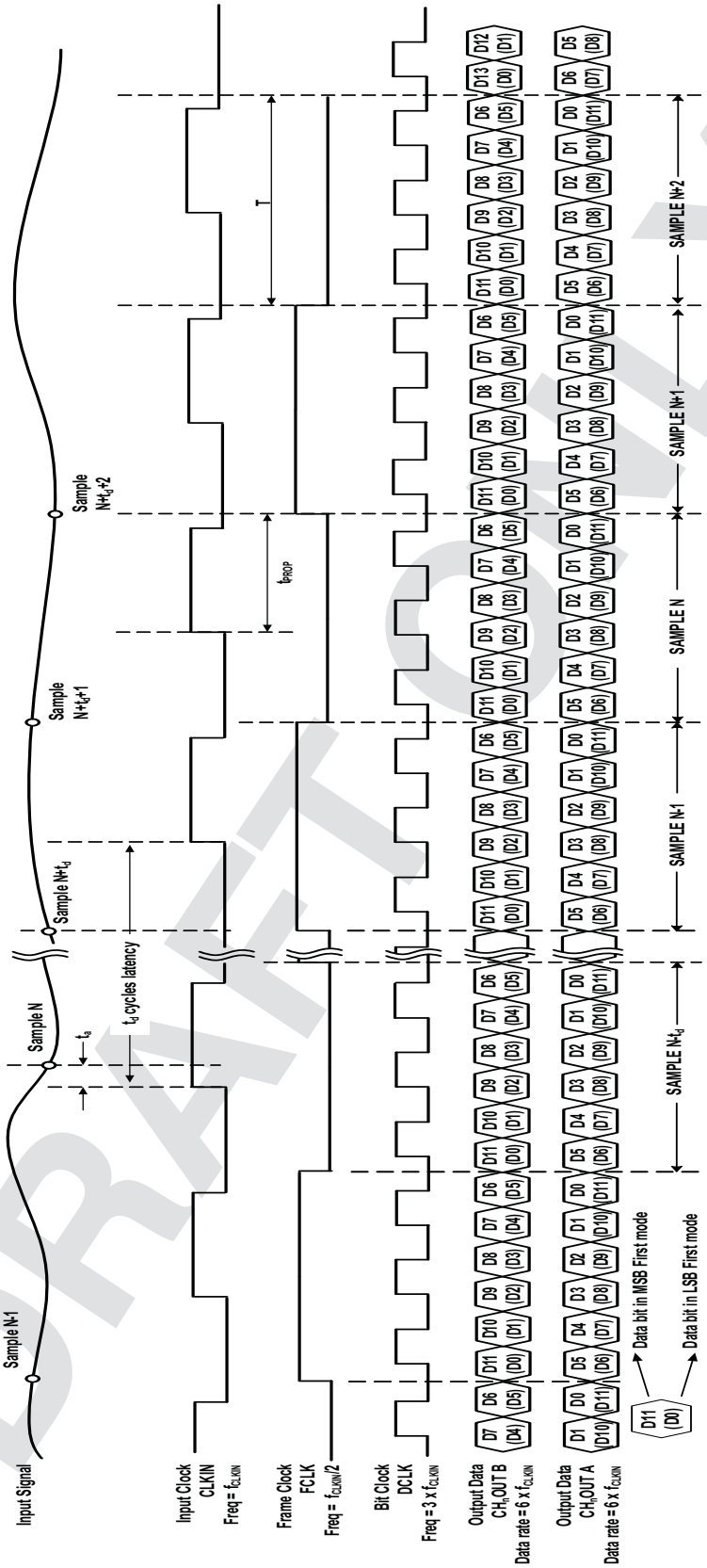


Figure 5.

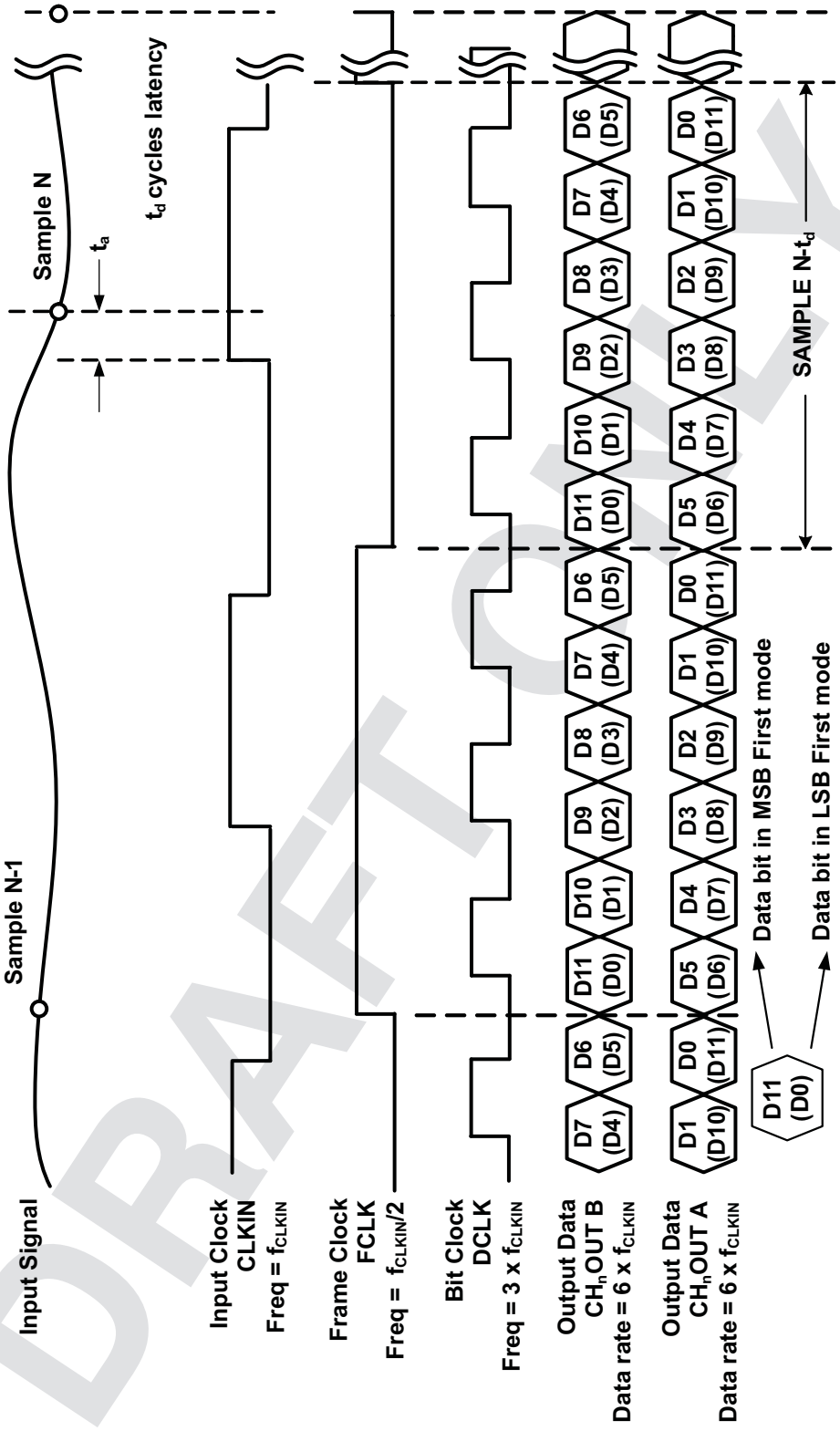


Figure 6. Enlarged 2-Wire LVDS Timing Diagram (12 bit)

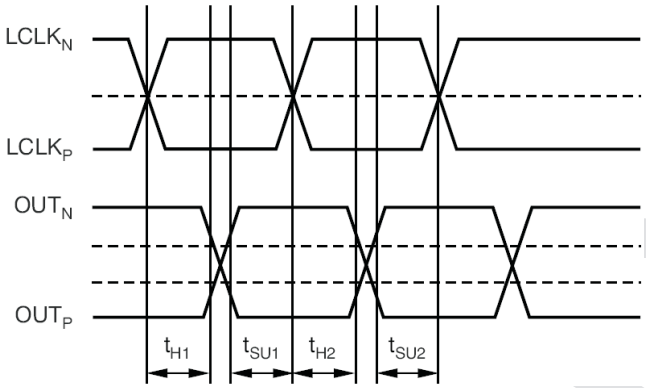


Figure 7. Definition of Setup and Hold Times t_{SU} = min(t_{SU1}, t_{SU2}); t_H = min(t_{H1}, t_{H2})

6 TYPICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 12-bit/80-MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

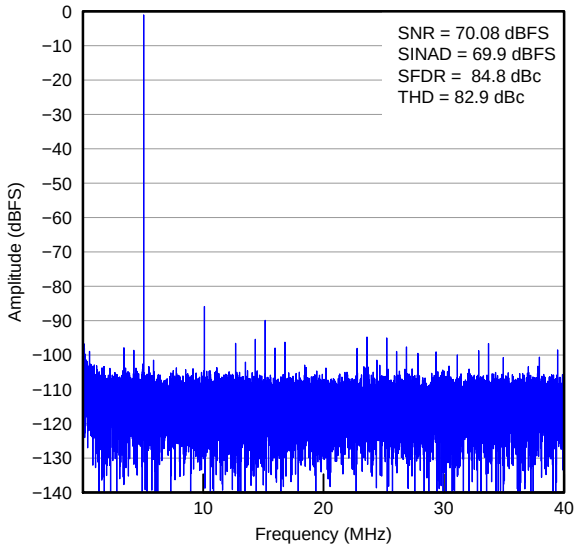


Figure 8.

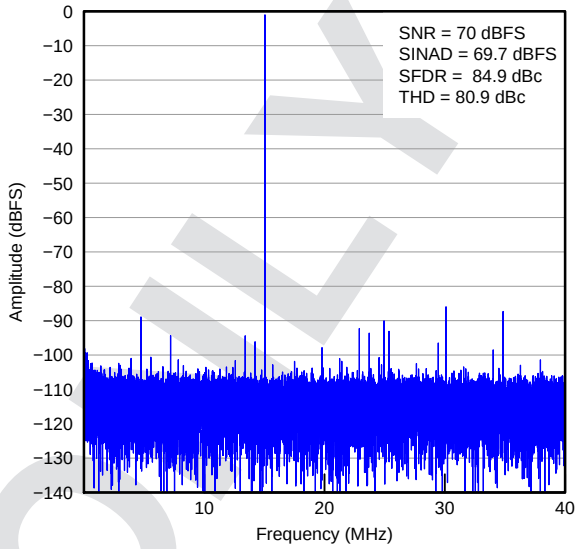


Figure 9.

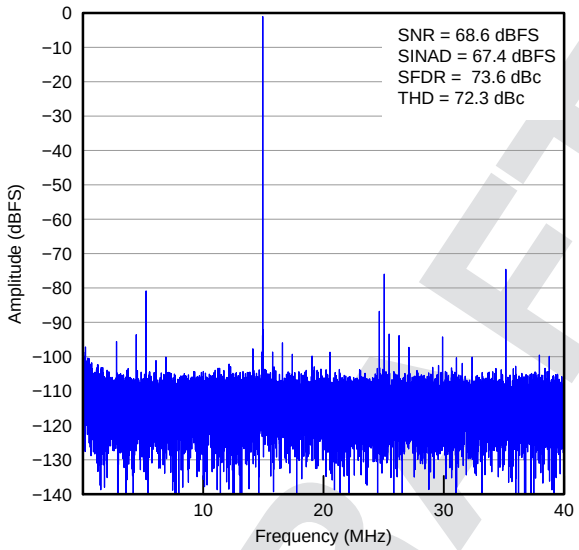


Figure 10.

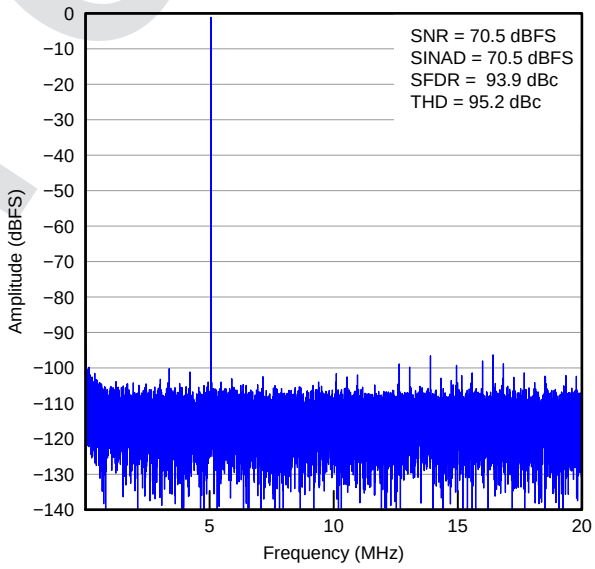


Figure 11.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 12-bit/80-MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

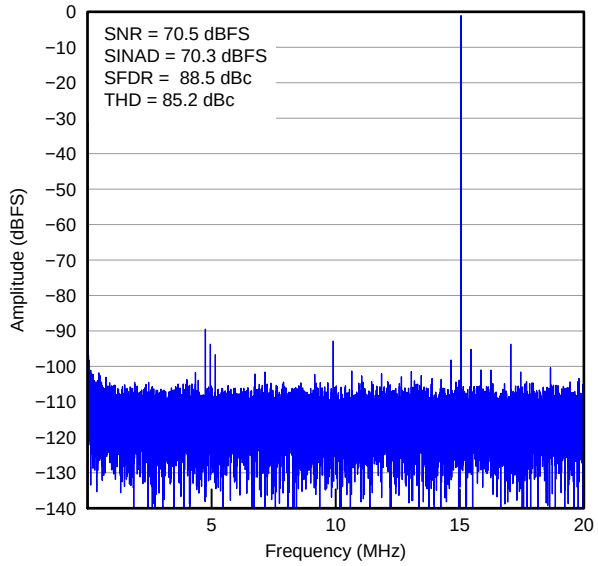


Figure 12.

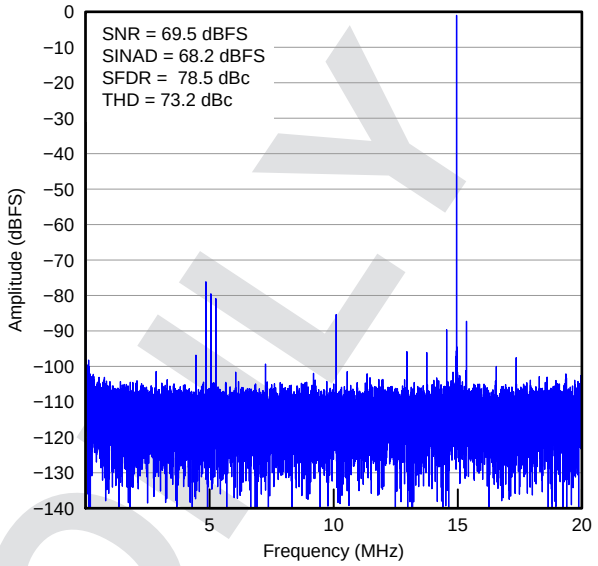


Figure 13.

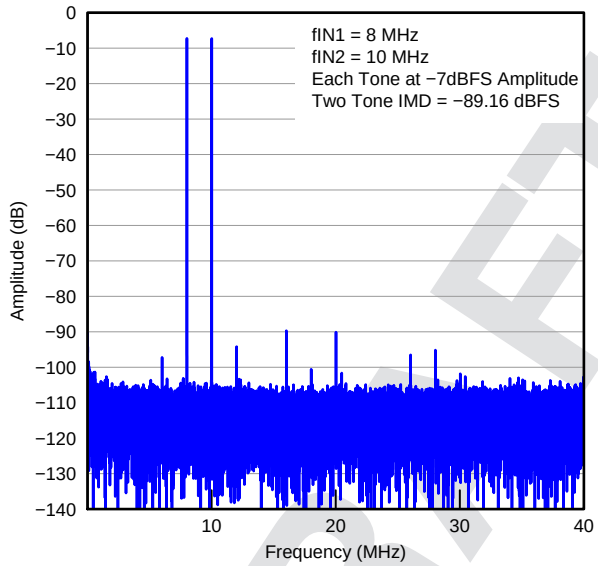


Figure 14.

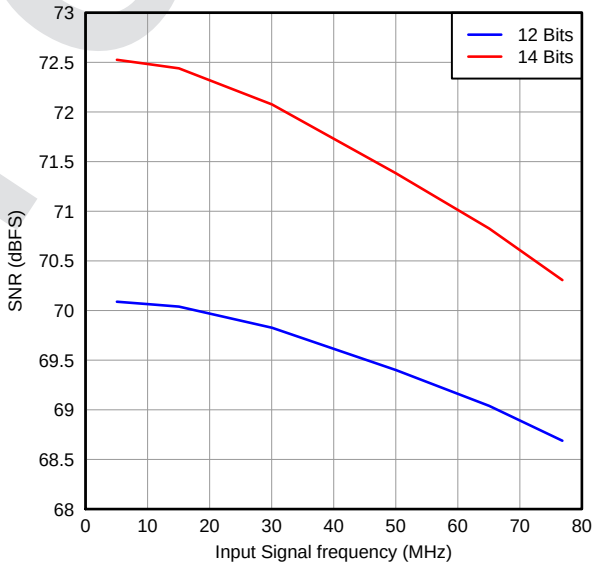


Figure 15.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 12-bit/80-MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

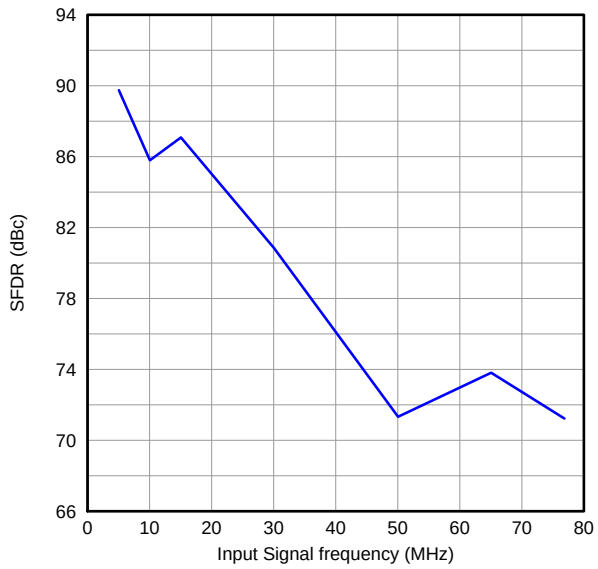


Figure 16.

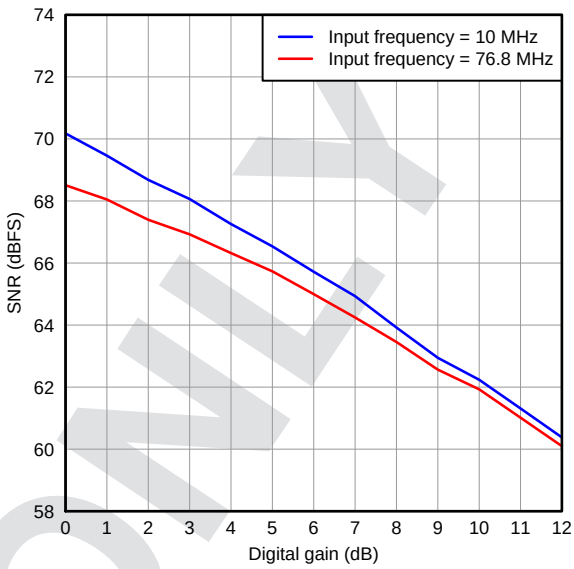


Figure 17.

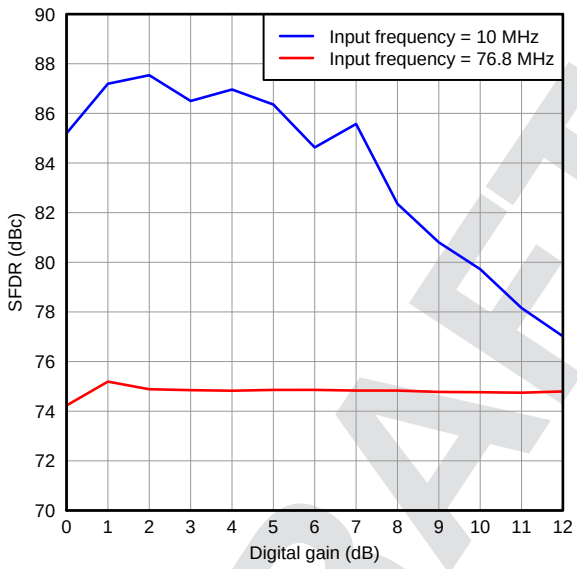


Figure 18.

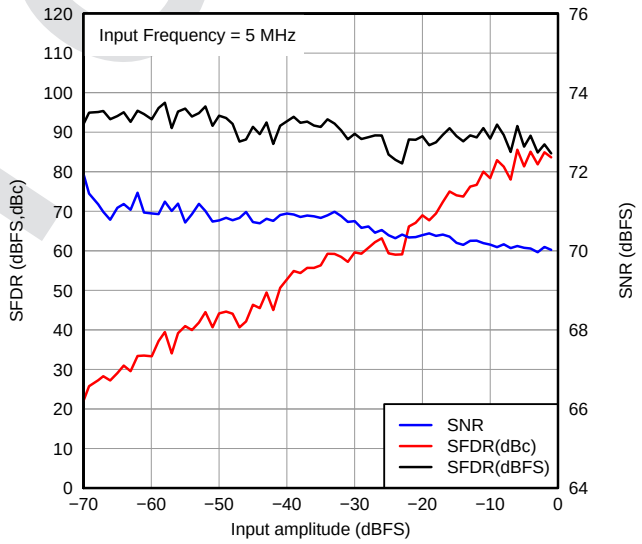


Figure 19.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 12-bit/80-MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

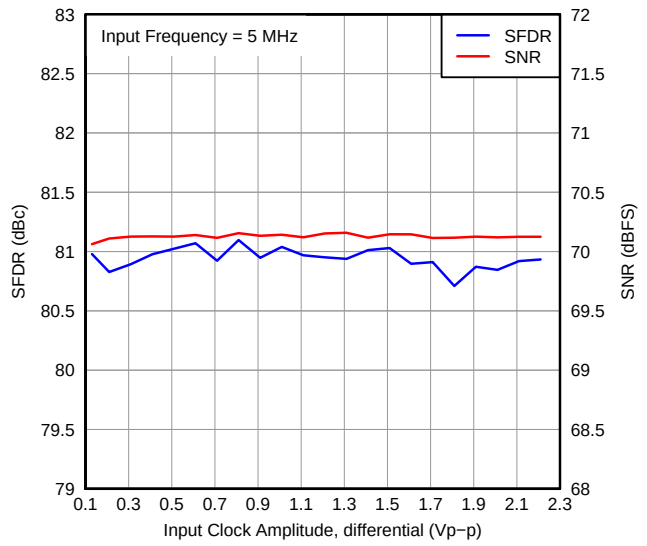


Figure 20.

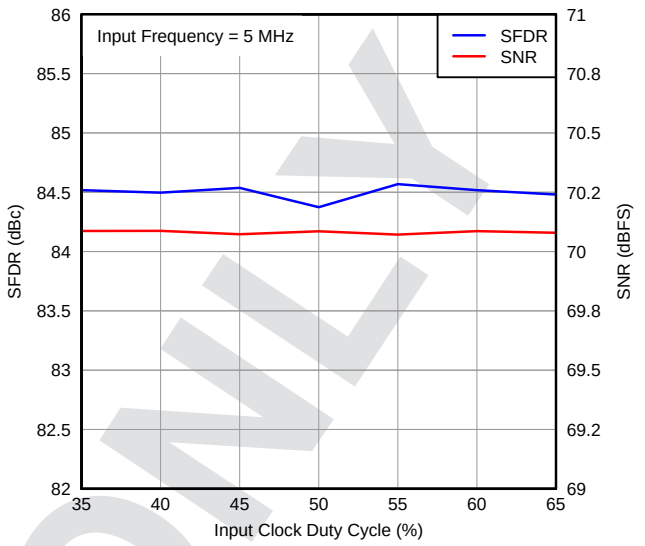


Figure 21.

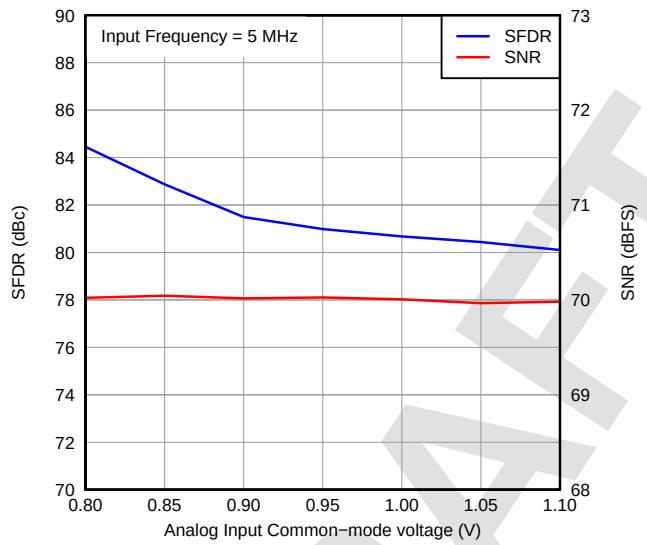


Figure 22.

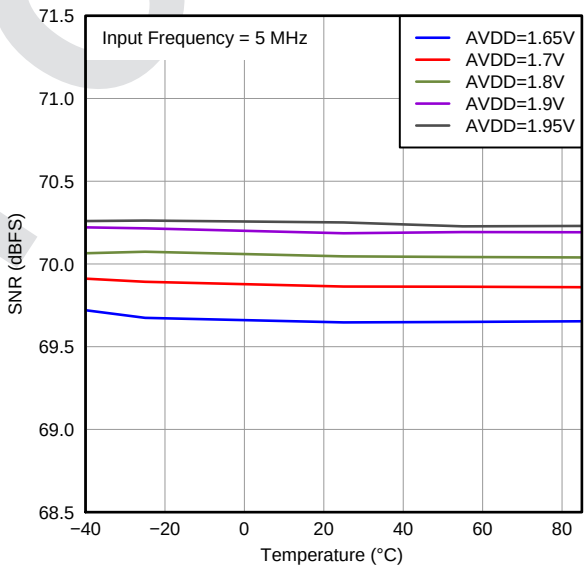


Figure 23.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 12-bit/80-MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

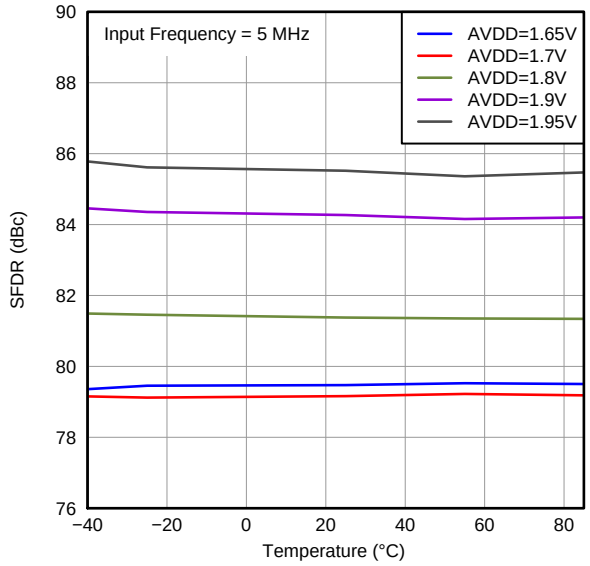


Figure 24.

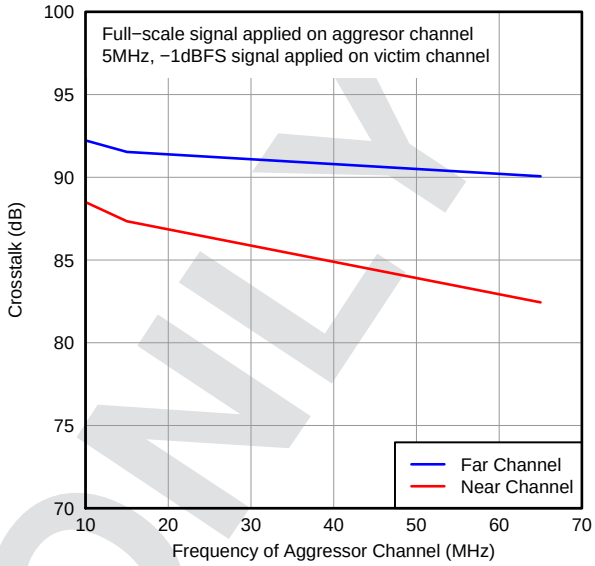


Figure 25.

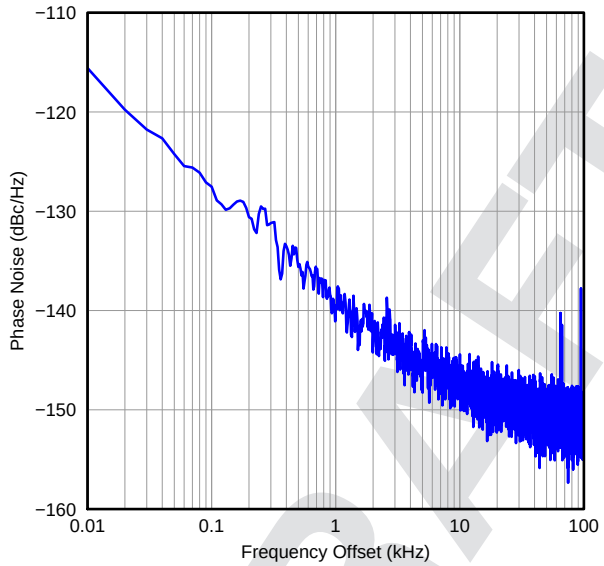


Figure 26.

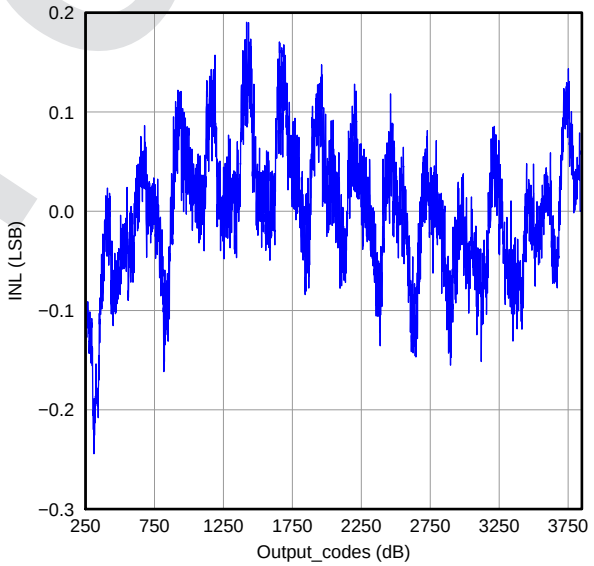


Figure 27.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 12-bit/80-MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

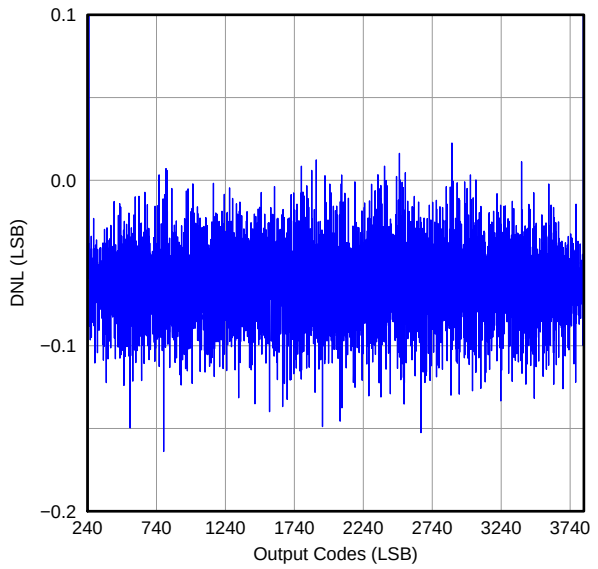


Figure 28.

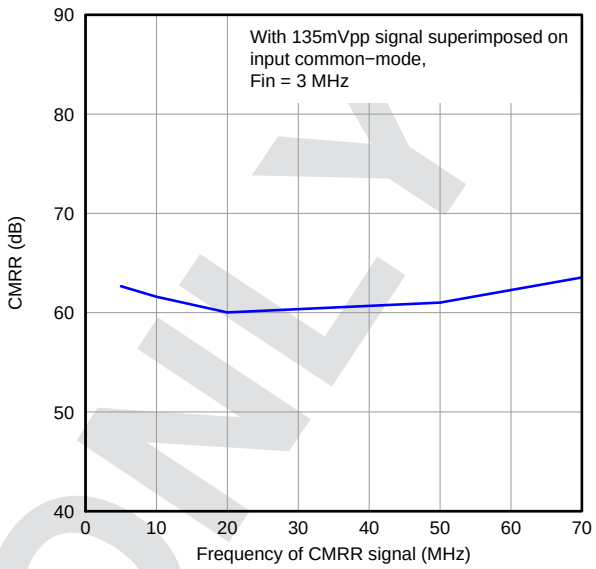


Figure 29.

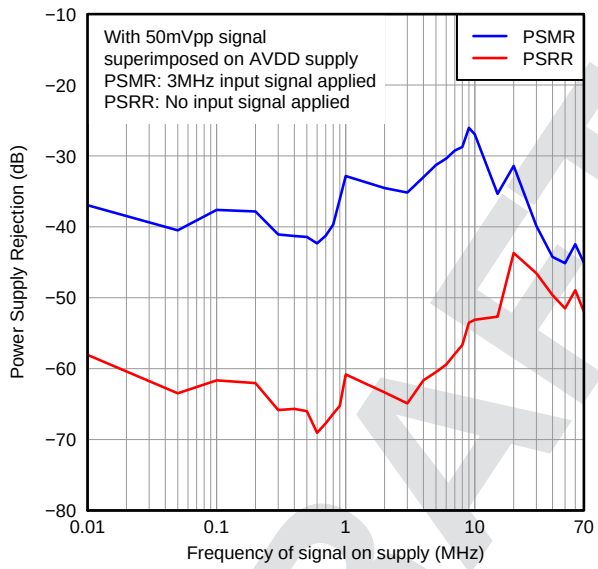


Figure 30.

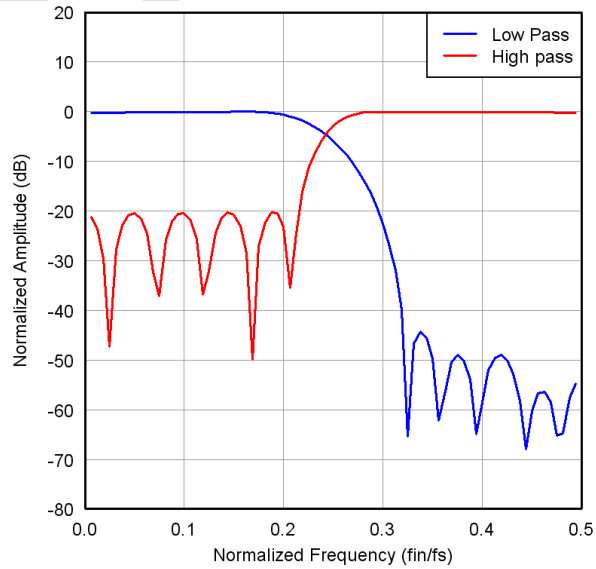


Figure 31.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 12-bit/80-MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

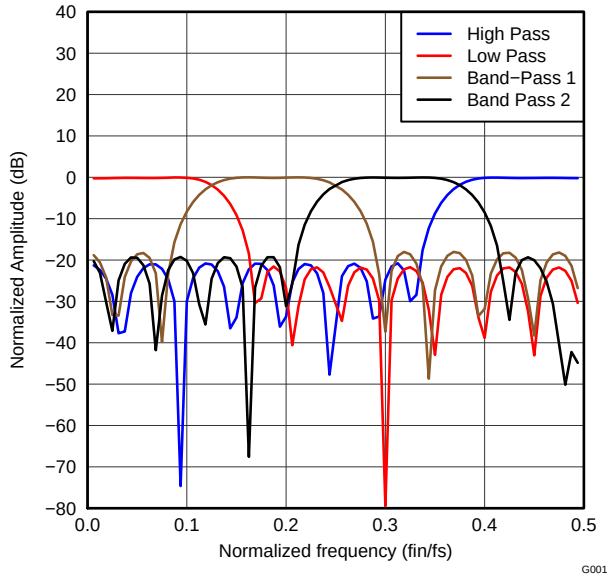


Figure 32.

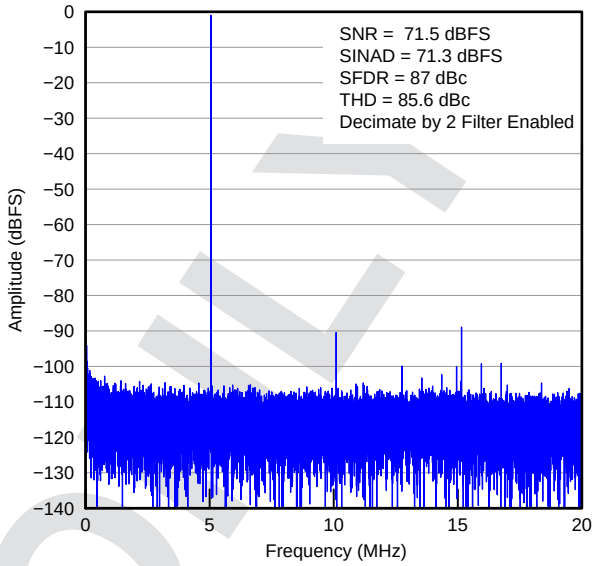


Figure 33.

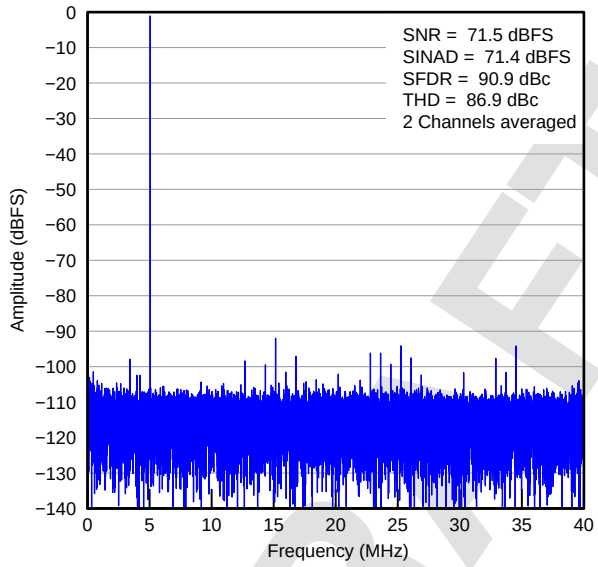


Figure 34.

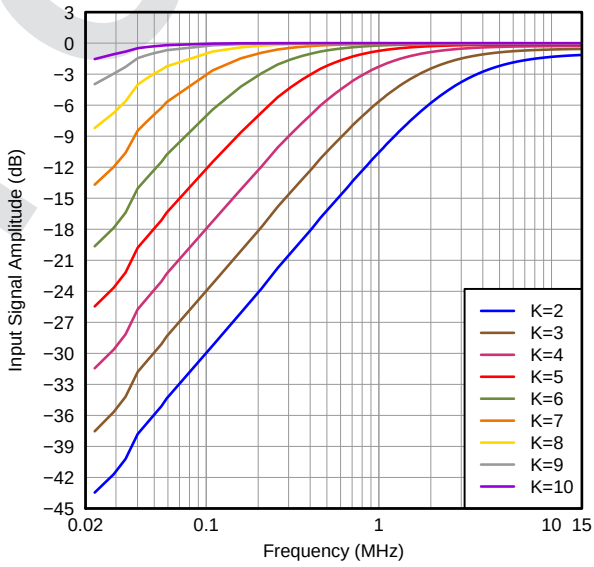


Figure 35.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 12-bit/80-MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

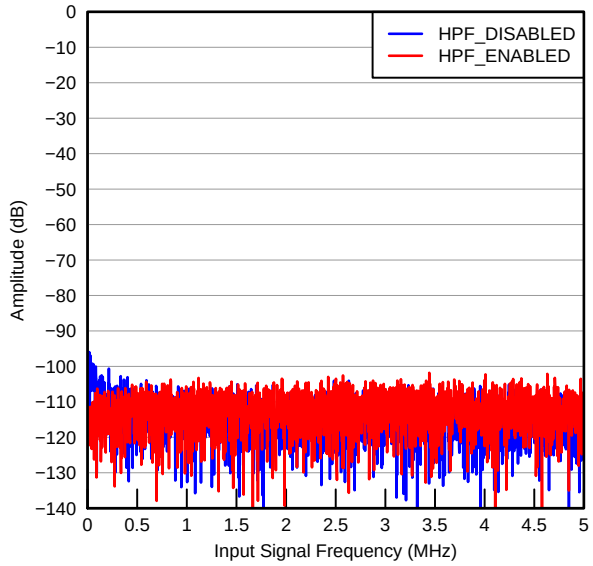


Figure 36.

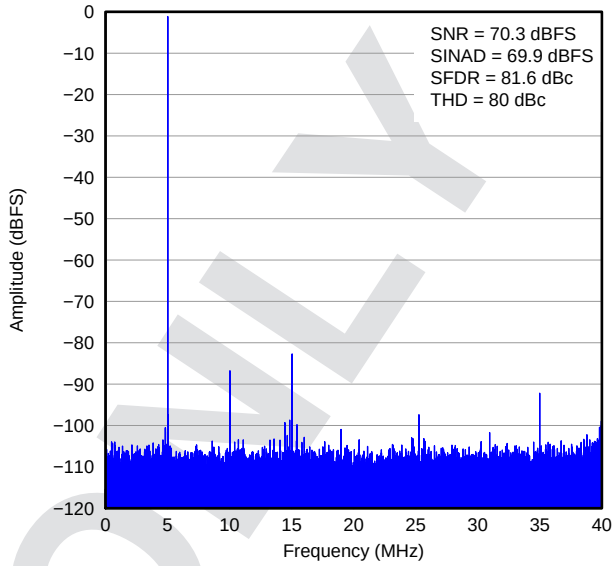


Figure 37.

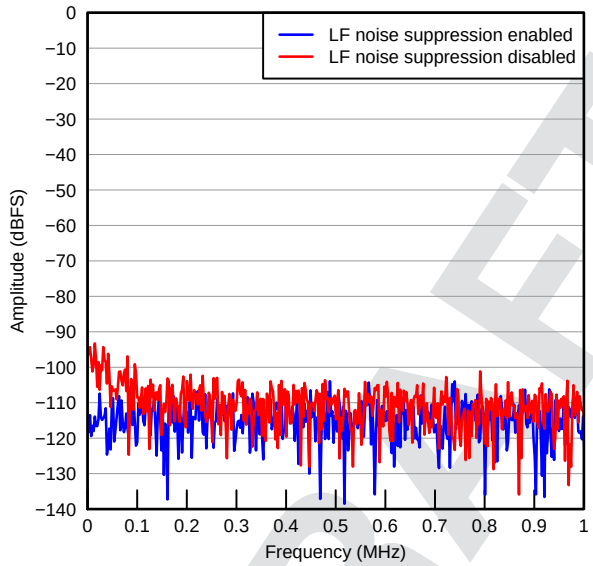


Figure 38.

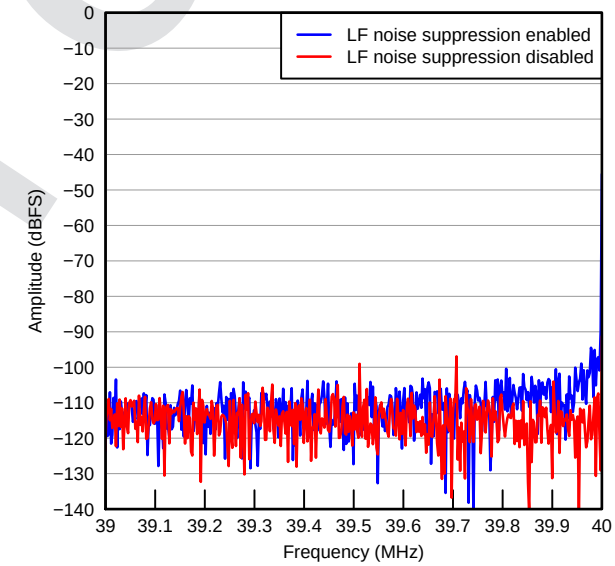


Figure 39.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 12-bit/80-MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

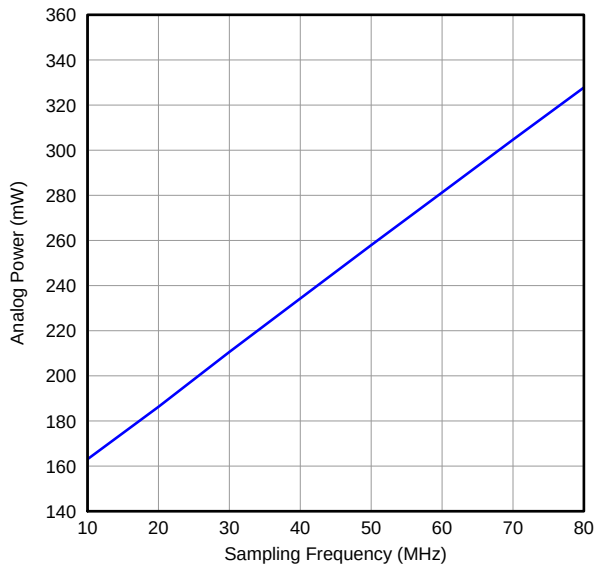


Figure 40.

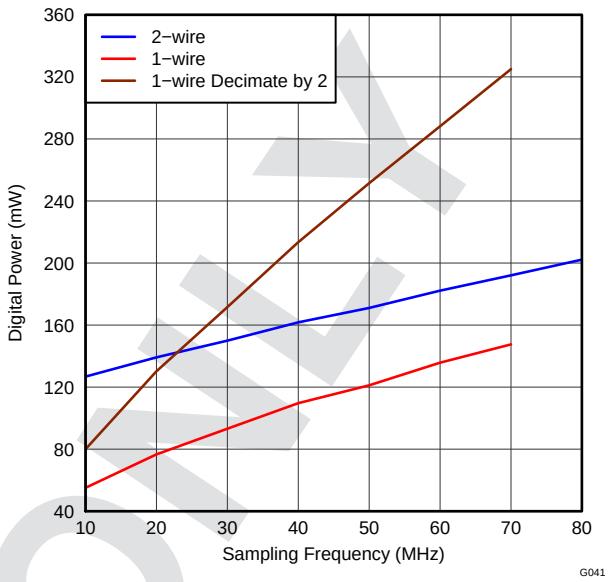


Figure 41.

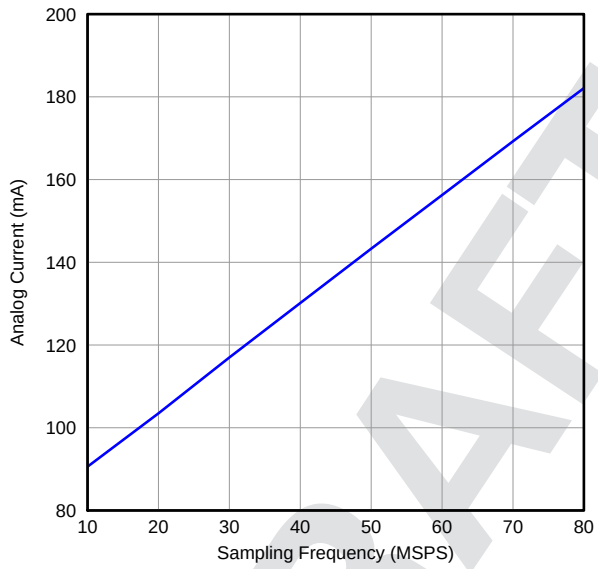


Figure 42.

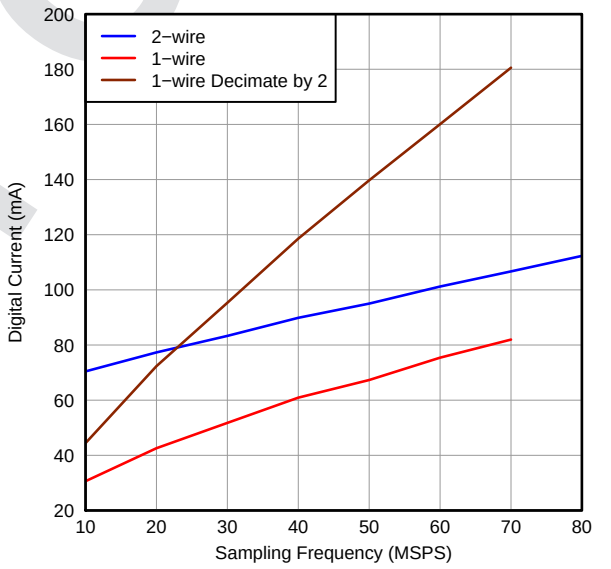


Figure 43.

6.1 SERIAL INTERFACE

The ADS5292 has a set of internal registers that are accessed by the serial interface formed by pins $\overline{CS}$ (Serial interface Enable — Active Low), SCLK (Serial Interface Clock), and SDATA (Serial Interface Data).

When $\overline{CS}$ is low,

- Serial shift of bits into the device is enabled.
- Serial data (SDATA) is latched at every rising edge of SCLK.
- SDATA is loaded into the register at every 24th SCLK rising edge.

If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data is loaded in multiples of 24-bit words within a single active $\overline{CS}$ pulse. The first eight bits form the register address and the remaining 16 bits from the register data. The interface works with SCLK frequencies from 15 MHz down to very low speeds (a few Hertz) and also with non-50% SCLK duty cycle.

6.2 Register Initialization

After power-up, the internal registers must be initialized to the respective default values. Initialization occurs in one of two ways:

1. Through a hardware reset, by applying a high pulse on the RESET pin.
2. Through a software reset: using the serial interface, set the RST bit high. Setting this bit initializes the internal registers to the respective default values and then self-resets the bit low. In this case, the RESET pin stays low (inactive).

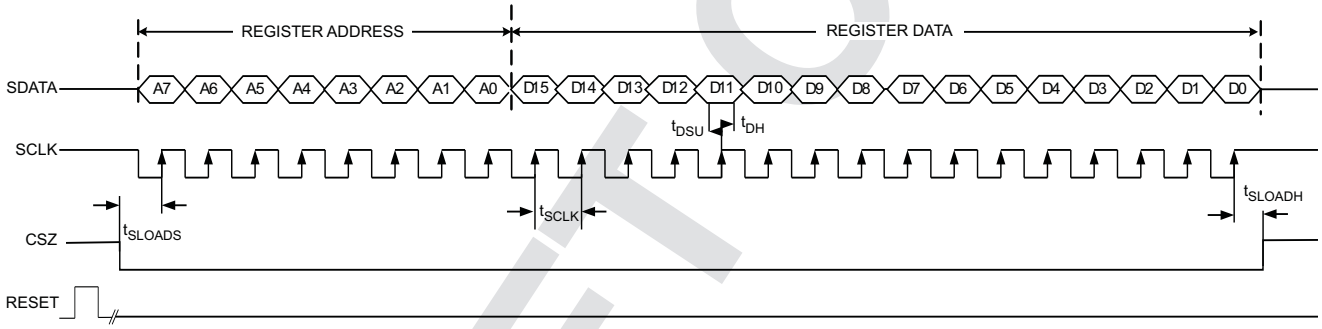


Figure 44. Serial Interface Timing

6.3 SERIAL INTERFACE TIMING CHARACTERISTICS

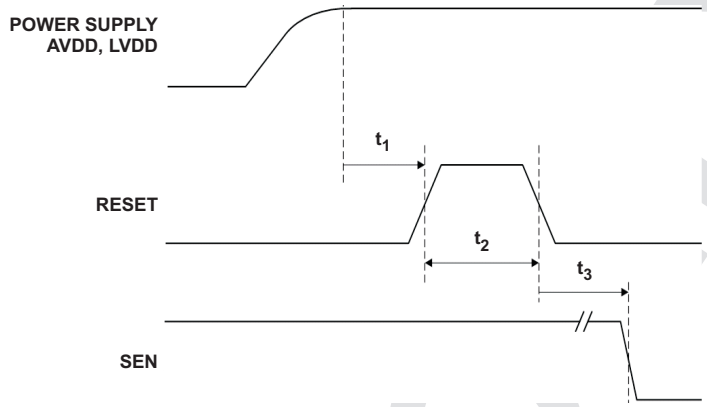
Typical values at 25°C, MIN and MAX values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.8 V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1/ t_{SCLK})	> DC		15	MHz
t_{SLOADS}	$\overline{CS}$ to SCLK setup time	33			ns
t_{SLOADH}	SCLK to $\overline{CS}$ hold time	33			ns
t_{DS}	SDATA setup time	33			ns
t_{DH}	SDATA hold time	33			ns

6.4 RESET TIMING

Typical values at 25°C, MIN and MAX values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power up of AVDD and LVDD to RESET pulse active		1		ms
t_2	Reset pulse duration	Pulse duration of active RESET signal	50			ns
t_3	Register write delay	Delay from RESET disable to $\overline{CS}$ active		100		ns



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET must be tied permanently HIGH.

Figure 45. Reset Timing Diagram

6.1 Serial Register Readout

The device includes a mode where the contents of the internal registers are read back on the SDOUT pin. This mode is a useful diagnostic check to verify the serial interface communication between the external controller and the ADC.

By default, after power-up and device reset, the SDOUT pin is in the high-impedance state. When the readout mode is enabled using the register bit <READOUT>, SDOUT outputs the contents of the selected register serially, which is described as follows.

- Set register bit <READOUT> = 1 to put the device in serial readout mode. This disables any further writes into the internal registers, EXCEPT the register at address 1.
  - Note that the <READOUT> bit itself is also located in register 1.

  The device exits readout mode by writing <READOUT> to 0.

  Only the contents of register at address 1 cannot be read in the register readout mode.
- Initiate a serial interface cycle specifying the address of the register (A7-A0) whose content is to be read.
- The device serially outputs the contents (D15–D0) of the selected register on the SDOUT pin.
- The external controller can latch the contents at the rising edge of SCLK.
- To exit the serial readout mode, reset register bit <READOUT> = 0, which enables writes into all registers of the device. At this point, the SDOUT pin enters the high-impedance state.

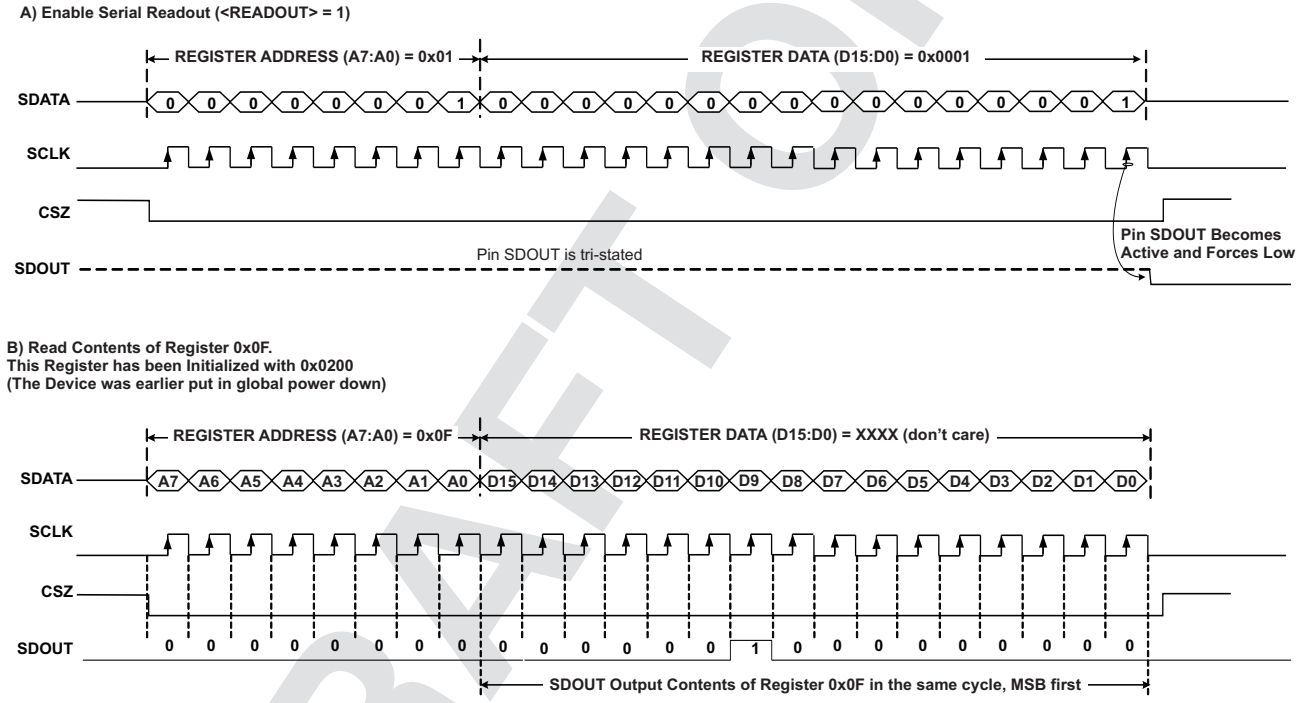


Figure 46. Serial Readout Timing

6.2 DEFAULT STATES AFTER RESET

- Device is in normal operation mode with 12-bit ADC enabled for all channels
- Output interface is 1-wire, 12×-serialization with 6×-bit clock and 1×-frame clock frequency
- Serial readout is disabled
- PDN pin is configured as global power-down pin
- Digital gain is set to 0 dB
- Digital modes such as LFNS and digital filters are disabled

6.3 Register Map

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
00																X	RST	1: Self-clearing software RESET; . After reset, this bit is set to 0 0: Normal operation.
01																X	EN_READOUT	1: READOUT of registers mode;0: Normal operation
												X					EN_HIGH_ADDRS	0 – Disable access to register at address 0xF0 1 – Enable access to register at address 0xF0
02			X														EN_SYNC	1:Enable SYNC feature to synchronize the test patterns; 0: SYNC feature is disabled for the test patterns. Note: this bit needs to be set as 1 when software or hardware test pattern SYNC feature is used. see Reg.0x25[8] and 0x25[15].
0A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RAMP_PAT_RESET_VAL	Ramp pattern reset value
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>	1:Channel-specific ADC power-down mode; 0: Normal operation
								X									PDN_PARTIAL	1:Partial power-down mode - fast recovery from power-down; 0: Normal operation
							X										PDN_COMPLETE	1:Register mode for complete power-down - slower recovery; 0: Normal operation
						X											PDN_PIN_CFG	1:Configures PD pin for partial power-down mode; 0:Configures PD pin for complete power-down mode
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>	1: Channel-specific low frequency noise suppression mode enable; 0: LFNS disabled
1C		X															EN_FRAME_PAT	1: Enables output frame clock to be programmed through a pattern; 0: Normal operation on frame clock
			X	X	X	X	X	X	X	X	X	X	X	X	X	X	ADCLKOUT<13:0>	14-bit pattern for frame clock on ADCLKP/ADCLKN pins
23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PRBS_SEED<15:0>	PRBS pattern starting seed value lower 16 bits
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>	1: Swaps the polarity of the analog input pins electrically; 0: Normal configuration
	X	X	X	X	X	X	X										PRBS_SEED<22:16>	PRBS seed starting value upper 7 bits

(1) The unused bits in each register (identified as blank table cells) must be programmed as '0'.
(2) X = Register bit referenced by the corresponding name and description
(3) Bits marked as '0' should be forced to 0, and bits marked as '1' should be forced to 1 when the particular register is programmed.
(4) A single write operation programs multiple functions in a register.

Register Map (continued)

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
25										X	0	0					EN_RAMP	1: Enables a repeating full scale ramp pattern on the outputs; 0: Normal operation
										0	X	0					DUALCUSTOM_PAT	1:Enables mode wherein output toggles between 2 defined codes; 0: Normal operation
										0	0	X					SINGLE_CUSTOM_PAT	1: Enables mode wherein output is a constant specified code; 0: Normal operation
															X	X	BITS_CUSTOM1<13:12>	2 MSBs for single custom pattern (and for the first code of the dual custom patterns)
													X	X			BITS_CUSTOM2<13:12>	2 MSBs for second code of the dual custom patterns
								X									TP_SOFT_SYNC	1: Software sync bit for Test patterns on all 8 CHs; 0: No sync. Note: in order to synchronize the digital filters using the SYNC pin, this bit must be set as 0.
				X													PRBS_TP_EN	1: PRBS test pattern enable bit; 0: PRBS test pattern disabled
			X														PRBS_MODE_2	PRBS 9 bit LFSR (23bit LFSR is default)
		X															PRBS_SEED_FROM_REG	1: Enable PRBS seed to be chosen from register 0x23 and 0x24; 0: Disabled
	X																TP_HARD_SYNC	1: Enable the external SYNC feature for syncing test patterns. 0: Inactive. Note: in order to synchronize the digital filters using the SYNC pin, this bit must be set as 0.
26	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM1<11:0>	12 lower bits for single custom pattern (and for the first code of the dual custom pattern).
27	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM2<11:0>	12 lower bits for second code of the dual custom pattern
28	X																EN_BITORDER	Enables the bit order output. 0 = Byte wise, 1 = Word wise
	0							X									BIT_WISE	Selects between bytewise and bit wise 1: bit-wise, odd bits come out on one wire and even bits come out on other wire 0: byte-wise, upper bits on one wire and lower bits on other wire. Note: D15 must be set to '0' for this mode
	1								X	X	X	X	X	X	X	X	EN_WORDWISE__BY_CH<7:0>	1: Output format is one sample on one LVDS wire and next sample on other LVDS wire. 0: Data comes out in two-wire mode with upper set of bits on one channel and lower set of bits on the other. Note: D15 must set '1' for this mode.
29															X		GLOBAL_EN_FILTER	1: Enables filter blocks - global control; 0: Inactive
																X	EN_CHANNEL_AVG	1: Enables channel averaging mode; 0: Inactive
2A													X	X	X	X	GAIN_CH1<3:0>	Programmable gain - Channel 1
									X	X	X	X					GAIN_CH2<3:0>	Programmable gain - Channel 2
					X	X	X	X									GAIN_CH3<3:0>	Programmable gain - Channel 3
	X	X	X	X													GAIN_CH4<3:0>	Programmable gain - Channel 4

Register Map (continued)

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
2B	X	X	X	X													GAIN_CH5<3:0>	Programmable gain - Channel 5
					X	X	X	X									GAIN_CH6<3:0>	Programmable gain - Channel 6
									X	X	X	X					GAIN_CH7<3:0>	Programmable gain - Channel 7
													X	X	X	X	GAIN_CH8<3:0>	Programmable gain - Channel 8
2C						X	X										AVG_CTRL4<1:0>	1: Averaging control for what comes out on LVDS output OUT4
									X	X							AVG_CTRL3<1:0>	Averaging control for what comes out on LVDS output OUT3
												X	X				AVG_CTRL2<1:0>	Averaging control for what comes out on LVDS output OUT2
															X	X	AVG_CTRL1<1:0>	Averaging control for what comes out on LVDS output OUT1
2D						X	X										AVG_CTRL8<1:0>	Averaging control for what comes out on LVDS output OUT8
									X	X							AVG_CTRL7<1:0>	Averaging control for what comes out on LVDS output OUT7
												X	X				AVG_CTRL6<1:0>	Averaging control for what comes out on LVDS output OUT6
															X	X	AVG_CTRL5<1:0>	Averaging control for what comes out on LVDS output OUT5
2E							X	X	X								FILTER1_COEFF_SET<2:0>	Select stored coefficient set for filter 1
										X	X	X					FILTER1_RATE<2:0>	Set decimation factor for filter 1
														X			ODD_TAP1	Use odd tap filter 1
																X	USE_FILTER1	1: Enables filter for channel 1; 0: Disables
			X	X	X	X											HPF_CORNER _CH1	HPF corner in values k from 2 to 10
		X															HPF_EN_CH1	1: HPF filter enable for the channel; 0: Disables
2F							X	X	X								FILTER2_COEFF_SET<2:0>	Select stored coefficient set for filter 2
										X	X	X					FILTER2_RATE<2:0>	Set decimation factor for filter 2
														X			ODD_TAP2	Use odd tap filter 2
																X	USE_FILTER2	1: Enables filter for channel 2; 0: Disables
			X	X	X	X											HPF_CORNER _CH2	HPF corner in values k from 2 to 10
		X															HPF_EN_CH2	1: HPF filter enabled for the channel; 0: Disabled
30							X	X	X								FILTER3_COEFF_SET<2:0>	Select stored coefficient set for filter 3
										X	X	X					FILTER3_RATE<2:0>	Set decimation factor for filter 3
														X			ODD_TAP3	Use odd tap filter 3
																X	USE_FILTER3	1: Enables filter for channel 3; 0: Disables
			X	X	X	X											HPF_CORNER _CH3	HPF corner in values k from 2 to 10
		X															HPF_EN_CH3	1: HPF filter enabled for the channel; 0: Disabled

Register Map (continued)

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
31							X	X	X								FILTER4_COEFF_SET<2:0>	Select stored coefficient set for filter 4
										X	X	X					FILTER4_RATE<2:0>	Set decimation factor for filter 4
														X			ODD_TAP4	Use odd tap filter 4
																X	USE_FILTER4	1: Enables filter for channel 4; 0: Disables
			X	X	X	X											HPF_CORNER _CH4	HPF corner in values k from 2 to 10
		X															HPF_EN_CH4	1: HPF filter enabled for the channel; 0: Disabled
32							X	X	X								FILTER5_COEFF_SET<2:0>	Select stored coefficient set for filter 5
										X	X	X					FILTER5_RATE<2:0>	Set decimation factor for filter 5
														X			ODD_TAP5	Use odd tap filter 5
																X	USE_FILTER5	1: Enables filter for channel 5; 0: Disables
			X	X	X	X											HPF_CORNER _CH5	HPF corner in values k from 2 to 10
		X															HPF_EN_CH5	1: HPF filter enabled for the channel; 0: Disabled
33							X	X	X								FILTER_TYPE6<2:0>	Select stored coefficient set for filter 6
										X							DECBY8_6	Enables decimate by 8 filter 6
											X	X					FILTER_MODE6<1:0>	Set decimation factor for filter 6
														X			ODD_TAP6	Use odd tap filter 6
																X	USE_FILTER6	Enables filter for channel 6
			X	X	X	X											HPF_CORNER _CH6	HPF corner in values k from 2 to 10
		X															HPF_EN_CH6	Hpf filter enable for the channel
34							X	X	X								FILTER_TYPE7<2:0>	Select stored coefficient set for filter 7
										X							DECBY8_7	Enables decimate by 8 filter 7
											X	X					FILTER_MODE7<1:0>	Set decimation factor for filter 7
														X			ODD_TAP7	Use odd tap filter 7
																X	USE_FILTER7	Enables filter for channel 7
			X	X	X	X											HPF_CORNER _CH7	HPF corner in values k from 2 to 10
		X															HPF_EN_CH7	Hpf filter enable for the channel
35							X	X	X								FILTER_TYPE8<2:0>	Select stored coefficient set for filter 8
										X							DECBY8_8	Enables decimate by 8 filter 8
											X	X					FILTER_MODE8<1:0>	Set decimation factor for filter 8
														X			ODD_TAP8	Use odd tap filter 8
																X	USE_FILTER8	1: Enables filter for channel 8; 0: Disables
			X	X	X	X											HPF_CORNER_CH8	HPF corner in values k from 2 to 10
		X															HPF_EN_CH8	1: HPF filter enable for the channel; 0: Disables

Register Map (continued)

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
38															X	X	DATA_RATE<1:0>	Select output frame clock rate (see OUTPUT DATA-RATE CONTROL)
42	X												X				EXT_REF_VCM	Drive external reference mode through: D15=D3=1: the VCM pin; D15=D3=0: REFT/REFB pins. Note: 0xF[15] should be set as '1' to enable the external reference mode
										X	X						PHASE_DDR<1:0>	Controls phase of LCLK output relative to data
45															0	X	PAT_DESKEW	1: Enable deskew pattern mode; 0: Inactive
															X	0	PAT_SYNC	1: Enable sync pattern mode; 0: Inactive
46	1															X	EN_2WIRE	1: 2 wire LVDS output; 0: 1 wire LVDS output
	1													X			BTC_MODE	1: 2's complement; (ADC data output format) 0: Binary Offset (ADC data output format)
	1												X				MSB_FIRST	1: MSB First; 0: LSB First
	1											X					EN_SDR	1:SDR Bit Clock; 0: DDR Bit Clock
	1				X	X	X	X									EN_BIT_SER	Output serialization mode. 0001: 10 bit (EN_10BIT) 0010: 12 bit (EN_12BIT) 0100: 14 bit (EN_14BIT) 1000: 16 bit (EN_16BIT)
	1		X														FALL_SDR	1: Controls LCLK rising or falling edge comes in the middle of data window when operating in SDR output mode; 0: At the edge of data window.
50	1												X	X	X	X	MAP_Ch1234_to_OUT1A	OUT1A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT1B	OUT1B Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch1234_to_OUT2A	OUT2A Pin pair to channel data mapping selection
51	1												X	X	X	X	MAP_Ch1234_to_OUT2B	OUT2B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT3A	OUT3A Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch1234_to_OUT3B	OUT3B Pin pair to channel data mapping selection
52	1												X	X	X	X	MAP_Ch1234_to_OUT4A	OUT4A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT4B	OUT4B Pin pair to channel data mapping selection
53	1												X	X	X	X	MAP_Ch5678_to_OUT5B	OUT5B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT5A	OUT5A Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch5678_to_OUT6B	OUT6B Pin pair to channel data mapping selection
54	1												X	X	X	X	MAP_Ch5678_to_OUT6A	OUT6A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT7B	OUT7B Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch5678_to_OUT7A	OUT7A Pin pair to channel data mapping selection

Register Map (continued)

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
55	1												X	X	X	X	MAP_Ch5678_to_OUT8B	OUT8B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT8A	OUT8A Pin pair to channel data mapping selection
F0	X																EN_EXT_REF	0 - Default: internal reference mode 1 - Enable external reference mode. the voltage reference can be applied on either REFP/B pins or VCM pin

7 DESCRIPTION OF SERIAL REGISTERS

7.1 POWER-DOWN MODES

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>
								X									PDN_PARTIAL
							X										PDN_COMPLETE
						X											PDN_PIN_CFG

Each of the eight channels can power down individually. PDN_CH<N> controls the power-down mode for ADC channel <N>. In addition to channel-specific power-down, the ADS5292 also has two global power-down modes:

1. The partial power-down mode which partially powers down the chip. Recovery from this mode is faster in 5 µs, provided that the clock has been running for at least 50 µs before exiting this mode.
2. The complete power-down mode which completely powers down the chip, and involves a much longer recovery time 100 µs.

In addition to programming the chip in either of these two power-down modes (through either the PDN_PARTIAL or PDN_COMPLETE bits), the PD pin is configured as either a partial power-down pin or a complete power-down pin control. For example, if PDN_PIN_CFG=0 (default), when the PD pin is high, the device enters complete power-down mode. However, if PDN_PIN_CFG=1, when the PD pin is high, the device enters partial power-down mode.

7.2 LOW-FREQUENCY NOISE-SUPPRESSION MODE

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>

The low-frequency noise-suppression mode is specifically useful in applications where good noise performance is desired in the frequency band of 0 to 1 MHz (around DC). Setting this mode shifts the low-frequency noise of the ADS5292 to approximately Fs / 2, thereby, moving the noise floor around DC to a much lower value. LFNS_CH<8:1> enables this mode individually for each channel. See Figure 38 and Figure 39.

7.3 ANALOG INPUT INVERT

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>

Generally, the IN_P pin represents the positive analog input pin, and IN_N represents the complementary negative input. Setting the bits marked INVERT_CH<8:1> (individual control for each channel) causes the inputs to swap. IN_N now represents the positive input, and IN_P the negative input.

7.4 LVDS TEST PATTERNS

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PRBS_SEED<15:0>
24	X	X	X	X	X	X	X										PRBS_SEED<22:16>
25										X	0	0					EN_RAMP
										0	X	0					DUALCUSTOM_PAT
										0	0	X					SINGLE_CUSTOM_PAT
															X	X	BITS_CUSTOM1<13:12>
													X	X			BITS_CUSTOM2<13:12>
								X									TP_SOFT_SYNC
				X													PRBS_TP_EN
			X														PRBS_MODE_2
		X															PRBS_SEED_FROM_REG
	X																TP_HARD_SYNC
26	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM1<11:0>
27	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM2<11:0>
45															0	X	PAT_DESKEW
															X	0	PAT_SYNC

The ADS5292 outputs a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. All these patterns can synchronize across devices by the sync function either through the hardware SYNC pin or the software sync bit TP_SOFT_SYNC bit in register 0x25. TP_HARD_SYNC bit when set enables the test patterns to synchronize by the hardware SYNC Pin. When the software sync bit TP_SOFT_SYNC bit is set, special timing is required.

- Setting EN_RAMP to 1 causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1 LSB every clock cycle. After hitting the full scale code, the ramp returns back to zero code and ramps again.
- The device is also programmed to output a constant code by setting SINGLE_CUSTOM_PAT to 1, and programming the desired code in BITS_CUSTOM1<13:0>. In this mode, BITS_CUSTOM1<13:0> take the place of the 12-bit ADC data at the output, and are controlled by LSB-first and MSB-first modes the same way as normal ADC data are.
- The device can toggle between two consecutive codes, by programming DUAL_CUSTOM_PAT to 1. The two codes are represented by the contents of BITS_CUSTOM1<13:0> and BITS_CUSTOM2<13:0>.
- In addition to custom patterns, the device can also output two preset patterns:
  - **Deskew pattern –** Set using PAT_DESKEW, this mode replaces the 12-bit ADC output D<13:0> with the 0101010101010101 word.
  - **Sync pattern –** Set using PAT_SYNC, the normal ADC word is replaced by a fixed 11111110000000 word.
  - **PRBS patterns –** The device gives a 9-bit or 23-bit LFSR pseudo-random pattern on the channel outputs that are controlled by the register 0x25. To enable the PRBS pattern **PRBS_TP_EN** bit in the register 0x25 must be set. The default is the 23-bit LFSR but a 9-bit LFSR is chosen by setting **PRBS_MODE_2** bit. The seed value for the PRBS patterns is chosen by enabling the **PRBS_SEED_FROM_REG** bit to 1 and the value written to the PRBS_SEED registers in 0x24 and 0x23.

Note that only one of the above patterns should be active at any given instant.

7.5 BIT-BYTE-WORD WISE OUTPUT

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
28	x																EN_BITORDER
	0							x									BIT_WISE
	1								X	X	X	X	X	X	X	X	EN_WORDWISE_BY_CH<7:>

Register 0x28 selects the LVDS-ADC output as bit-wise, byte-wise, or word-wise in the 2-wire mode. See Figure 47 and Figure 48 for details.

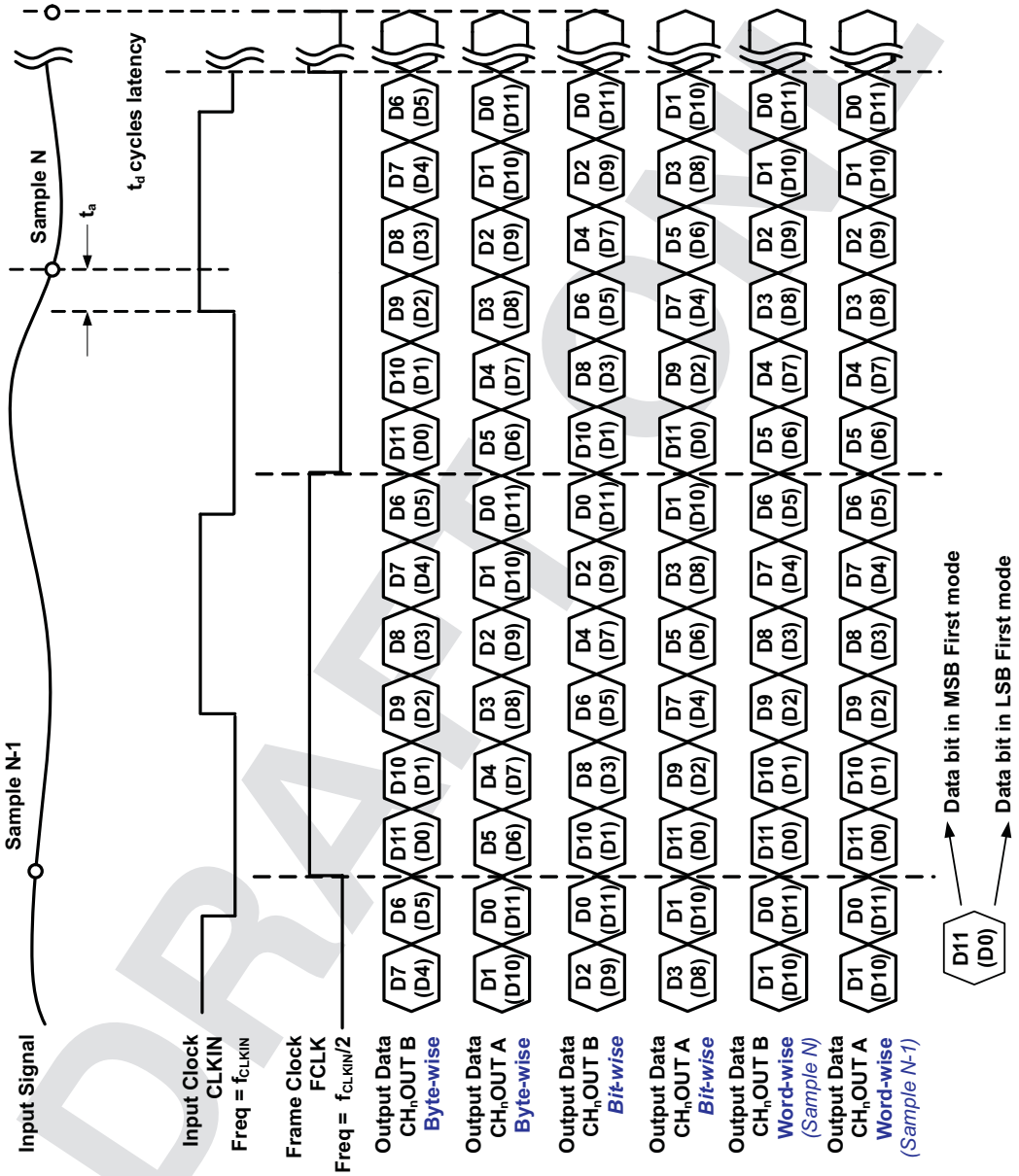


Figure 47. 12-Bit Word Wise

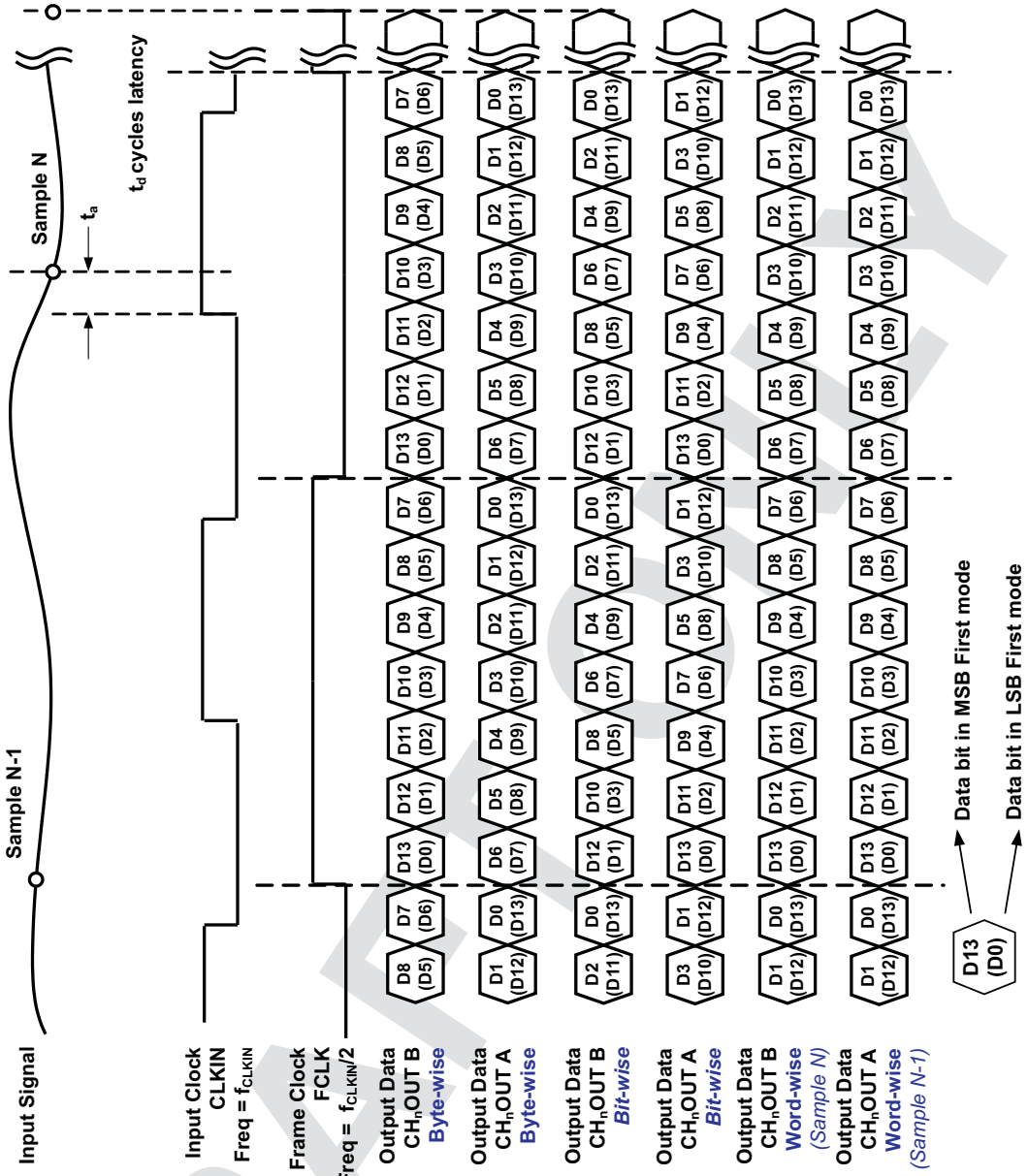


Figure 48. 14-Bit Word Wise

7.6 DIGITAL PROCESSING BLOCKS

The ADS5292 integrates a set of commonly-used digital functions to ease system design. These functions are shown in the digital block diagram of Figure 49 and described in the following sections.

DIGITAL PROCESSING BLOCKS (continued)

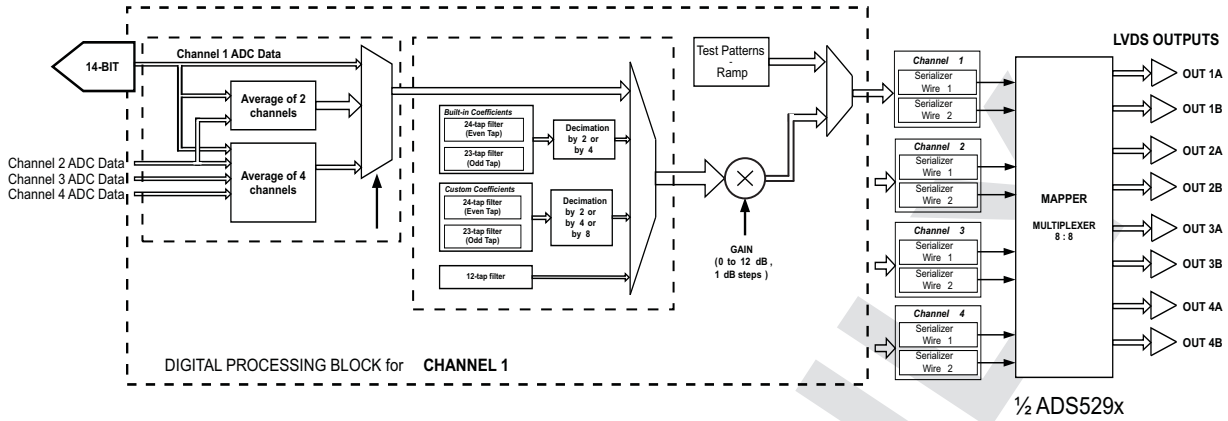


Figure 49. Digital Processing Block Diagram

7.7 PROGRAMMABLE DIGITAL GAIN

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2A													X	X	X	X	GAIN_CH1<3:0>
									X	X	X	X					GAIN_CH2<3:0>
					X	X	X	X									GAIN_CH3<3:0>
	X	X	X	X													GAIN_CH4<3:0>
2B	X	X	X	X													GAIN_CH5<3:0>
					X	X	X	X									GAIN_CH6<3:0>
									X	X	X	X					GAIN_CH7<3:0>
													X	X	X	X	GAIN_CH8<3:0>

In applications where the full scale swing of the analog input signal is much less than the 2 V_{PP} range supported by the ADS5292, a programmable digital gain is set to achieve the full-scale output code even with a lower analog input swing. The programmable gain for each channel is individually set using a set of four bits, indicated as GAIN_CHN<3:0> for Channel N. The gain setting is coded in binary from 0-12 dB as shown in Table 4.

Table 4. Gain Setting for Channel N

GAIN_CHN<3>	GAIN_CHN<2>	GAIN_CHN<1>	GAIN_CHN<0>	CHANNEL N GAIN SETTING
0	0	0	0	0 dB
0	0	0	1	1 dB
0	0	1	0	2 dB
0	0	1	1	3 dB
0	1	0	0	4 dB
0	1	0	1	5 dB
0	1	1	0	6 dB
0	1	1	1	7 dB
1	0	0	0	8 dB
1	0	0	1	9 dB
1	0	1	0	10 dB
1	0	1	1	11 dB
1	1	0	0	12 dB
1	1	0	1	Do not use
1	1	1	0	Do not use

Table 4. Gain Setting for Channel N (continued)

GAIN_CHN<3>	GAIN_CHN<2>	GAIN_CHN<1>	GAIN_CHN<0>	CHANNEL N GAIN SETTING
1	1	1	1	Do not use

7.8 CHANNEL AVERAGING

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
29																X	EN_CHANNEL_AVG
2C						X	X										AVG_CTRL4<1:0>
									X	X							AVG_CTRL3<1:0>
												X	X				AVG_CTRL2<1:0>
															X	X	AVG_CTRL1<1:0>
2D						X	X										AVG_CTRL8<1:0>
									X	X							AVG_CTRL7<1:0>
												X	X				AVG_CTRL6<1:0>
															X	X	AVG_CTRL5<1:0>

In the default mode of operation, the LVDS outputs <8..1> contain the data of the ADC Channels <8..1>. By setting the EN_CHANNEL_AVG bit to '1', the outputs from multiple channels can be averaged. The resulting outputs from the channel-averaging block (which is bypassed in the default mode) are referred to as Bins. The contents of the Bins <8..1> come out on the LVDS outputs <8..1>. The contents of each of the eight Bins are determined by the register bits marked AVG_CTRL*n*<1:0> where *n* stands for the Bin number. The different settings are shown below:

AVG_CTRL1<1>	AVG_CTRL1<0>	Contents of Bin 1
0	0	Zero
0	1	ADC Channel 1
1	0	Average of ADC Channel 1, 2
1	1	Average of ADC Channel 1, 2, 3, 4
AVG_CTRL2<1>	**AVG_CTRL2<0>**	**Contents of Bin 2**
0	0	Zero
0	1	ADC Channel 2
1	0	ADC Channel 3
1	1	Average of ADC Channel 3, 4
AVG_CTRL3<1>	**AVG_CTRL3<0>**	**Contents of Bin 3**
0	0	Zero
0	1	ADC Channel 3
1	0	ADC Channel 2
1	1	Average of ADC Channel 1, 2
AVG_CTRL4<1>	**AVG_CTRL4<0>**	**Contents of Bin 4**
0	0	Zero
0	1	ADC Channel 4
1	0	Average of ADC Channel 3, 4
1	1	Average of ADC Channel 1, 2, 3, 4
AVG_CTRL5<1>	**AVG_CTRL5<0>**	**Contents of Bin 5**
0	0	Zero
0	1	ADC Channel 5
1	0	Average of ADC Channel 5, 6
1	1	Average of ADC Channel 5, 6, 7, 8
AVG_CTRL6<1>	**AVG_CTRL6<0>**	**Contents of Bin 6**
0	0	Zero

AVG_CTRL1<1>	AVG_CTRL1<0>	Contents of Bin 1
0	1	ADC Channel 6
1	0	ADC Channel 7
1	1	Average of ADC Channel 7, 8
AVG_CTRL7<1>	**AVG_CTRL7<0>**	**Contents of Bin 7**
0	0	Zero
0	1	ADC Channel 7
1	0	ADC Channel 6
1	1	Average of ADC Channel 6, 5
AVG_CTRL8<1>	**AVG_CTRL8<0>**	**Contents of Bin 8**
0	0	Zero
0	1	ADC Channel 8
1	0	Average of ADC Channel 7, 8
1	1	Average of ADC Channel 5, 6, 7, 8

When the contents of a particular Bin is set to zero, then the LVDS buffer corresponding to that bin automatically powers down.

7.9 DECIMATION FILTER

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
29															X		GLOBAL_EN_FILTER
2E							X	X	X								FILTER1_COEFF_SET<2:0>
										X	X	X					FILTER1_RATE<2:0>
														X			ODD_TAP1
																X	USE_FILTER1
2F							X	X	X								FILTER2_COEFF_SET<2:0>
										X	X	X					FILTER2_RATE<2:0>
														X			ODD_TAP2
																X	USE_FILTER2
30							X	X	X								FILTER3_COEFF_SET<2:0>
										X	X	X					FILTER3_RATE<2:0>
														X			ODD_TAP3
																X	USE_FILTER3
31							X	X	X								FILTER4_COEFF_SET<2:0>
										X	X	X					FILTER4_RATE<2:0>
														X			ODD_TAP4
																X	USE_FILTER4
32							X	X	X								FILTER5_COEFF_SET<2:0>
										X	X	X					FILTER5_RATE<2:0>
														X			ODD_TAP5
																X	USE_FILTER5
33							X	X	X								FILTER6_COEFF_SET<2:0>
										X	X	X					FILTER6_RATE<2:0>
														X			ODD_TAP6
																X	USE_FILTER6
34							X	X	X								FILTER7_COEFF_SET<2:0>
										X	X	X					FILTER7_RATE<2:0>
														X			ODD_TAP7
																X	USE_FILTER7
35							X	X	X								FILTER8_COEFF_SET<2:0>
										X	X	X					FILTER8_RATE<2:0>
														X			ODD_TAP8
																X	USE_FILTER8

The decimation filter is implemented as 24-tap FIR with symmetrical coefficients (each coefficient is 12-bit signed). The filter equation is shown in Equation 1.

$$y(n) = \left(\frac{1}{2^{11}}\right) \times \left[(h_0 \times x(n) + h_1 \times x(n-1) + h_2 \times x(n-2) + \ldots + h_{11} \times x(n-11) + h_{11} \times x(n-12) \ldots + h_1 \times x(n-22) + h_0 \times x(n-23)\right] \quad (1)$$

By setting the register bit <ODD_TAPn> = 1, a 23-tap FIR is implemented:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times \left[(h_0 \times x(n) + h_1 \times x(n-1) + h_2 \times x(n-2) + \ldots + h_{10} \times x(n-10) + h_{11} \times x(n-11) + h_{10} \times x(n-12) \ldots + h_1 \times x(n-21) + h_0 \times x(n-22)\right] \quad (2)$$

In Equation 1 and Equation 2, *h0, h1 …h_{11}* are 12-bit signed representation of the coefficients, *x(n)* is the input data sequence to the filter and *y(n)* is the filter output sequence.

A decimation filter is introduced at the output of each channel. To enable this feature, the GLOBAL_EN_FILTER should be set to '1'. Setting this bit to '1' increases the overall latency of each channel to 20-clock cycles irrespective of whether the filter for that particular channel has been chosen or not (using the USE_FILTER bit). The bits marked FILTER*n*_COEFF_SET<2:0>, FILTER*n*_RATE<2:0>, ODD_TAP*n* and USE_FILTER*n* represent the controls for the filter for Channel *n*. Note that these bits are functional only when the GLOBAL_EN_FILTER is set to '1' and USE_FILTERn bit is set to '1'. For illustration, the controls for channel 1 are listed in Table 5:

The USE_FILTER1 bit determines whether the filter for Channel 1 is used or not. When this bit is set to '1', the filter for channel 1 is enabled. When this bit is set to '0', the filter for channel 1 is disabled but the channel data passes through a dummy delay so that the overall latency of channel 1 is 20 clock cycles. With the USE_FILTER1 bit set to '1', the characteristics of the filter are set by using the other sets of bits.

The ADS5292 has six sets of filter coefficients stored in memory. Each of these sets define a unique pass band in the frequency domain and contain 12 coefficients (each coefficient is 12-bit long). These 12 coefficients are used to implement either a symmetric 24-tap (even-tap) filter, or a symmetric 23-tap (odd-tap) filter. Setting the register bit ODD_TAP1 to '1' enables the odd-tap configuration (the default is even tap with this bit set to '0') for Channel 1. The bits FILTER1_COEFF_SET<2:0> is used to choose the required set of coefficients for Channel 1.

The passbands corresponding to of each of these filter coefficient sets is shown in Figure 50

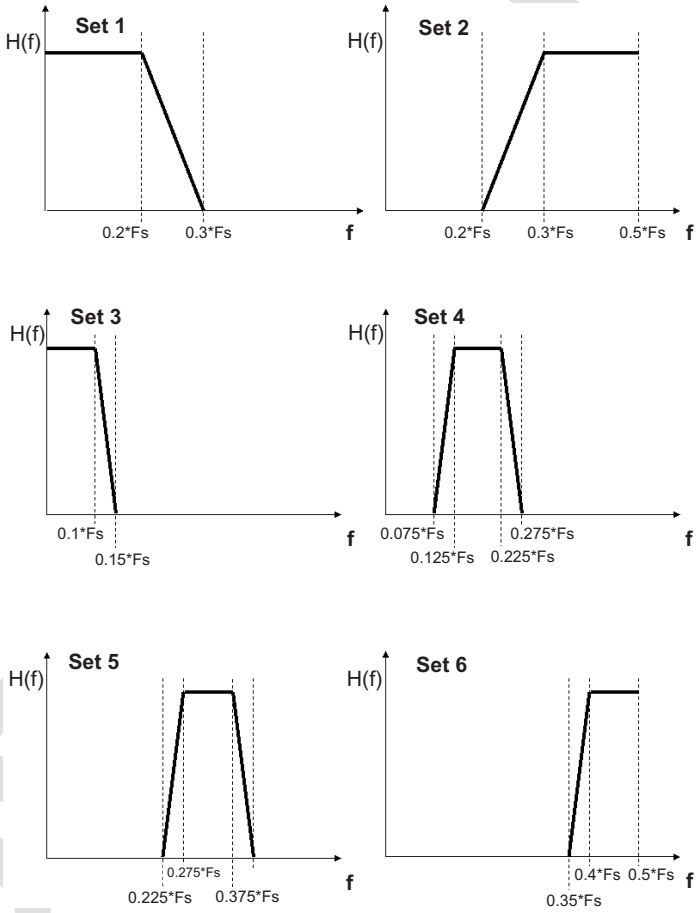


Figure 50. Filter Types

Coefficient Sets 1 and 2 are the most appropriate when decimation by a factor of 2 is required, whereas coefficient Sets 3, 4, 5, and 6 are appropriate when decimation by a factor of 4 is desired. The computation rate of the filter output is independently set using the bits FILTERn_RATE<2:0>. The settings are shown in Table 5.

Table 5. Digital Filters

DECIMATION	TYPE OF FILTER	<DATA RATE>	FILTERn RATE>	<FILTERn COEFF SET>	<ODD TAP>	<USE FILTER CHn>	<EN CUSTOM FILT>
Decimate by 2	Built-in **low-pass odd-tap** filter (pass band = 0 to f_S / 4)	001	000	000	1	1	0
	Built-in **high-pass odd-tap** filter (pass band = 0 to f_S / 4)	001	000	001	1	1	0
Decimate by 4	Built-in **low-pass even-tap** filter (pass band = 0 to f_S / 8)	010	001	010	0	1	0
	Built-in first **band pass even tap** filter(pass band = f_S / 8 to f_S / 4)	010	001	011	0	1	0
	Built-in second **band pass even tap** filter(pass band = f_S / 4 to 3 f_S / 8)	010	001	100	0	1	0
	Built-in **high pass odd tap** filter (pass band = 3 f_S / 8 to f_S / 2)	010	001	101	1	1	0
Decimate by 2	Custom filter (user-programmable coefficients)	001	000	000	0 and 1	1	1
Decimate by 4	Custom filter (user-programmable coefficients)	010	001	000	0 and 1	1	1
Decimate by 8	Custom filter (user-programmable coefficients)	011	100	000	0 and 1	1	1
Bypass decimation	Custom filter (user-programmable coefficients)				0 and 1	1	1
Note: EN_CUSTOM_FILT is the D15 of register 5A (Hex) to B9 (Hex).							

The choice of the odd or even tap setting, filter coefficient set, and the filter rate uniquely determines the filter to be used. In addition to the preset filter coefficients, the coefficients for each of the eight filter channels is programmed by the user. Each of the eight channels has 12 programmable coefficients, each 12-bit long. The 96 registers with addresses from 5A (Hex) to B9 (Hex) are used to program these 8 sets of 12 programmable coefficients. Registers 5A to 65 are used to program the first filter, with the first coefficient occupying the bits D11..D0 of register 5A, the second coefficient occupying the bits D11..D0 of register 5B, and so on. Similarly registers 66(Hex) to 71(Hex) are used to program the second filter, and so on.

When programming the filter coefficients, the D15 bit of each of the 12 registers corresponding to that filter should be set to '1'. If the D15 bit of these 12 registers is set to '0', then the preset coefficient (as programmed by FILTERn_COEFF_SET<2:0>) is used even if the bits D11..D0 are programmed. By setting or not setting the D15 bits of individual filter channels to '1', some filters operate with preset coefficient sets, and others simultaneously operate with programmed coefficient sets.

7.10 HIGH-PASS FILTER

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2E			X	X	X	X											HPF_corner_CH1
2E		X															HPF_EN_CH1
2F			X	X	X	X											HPF_corner_CH2
2F		X															HPF_EN_CH2
30			X	X	X	X											HPF_corner_CH3
30		X															HPF_EN_CH3
31			X	X	X	X											HPF_corner_CH4
31		X															HPF_EN_CH4
32			X	X	X	X											HPF_corner_CH5
32		X															HPF_EN_CH5
33			X	X	X	X											HPF_corner_CH6
33		X															HPF_EN_CH6
34			X	X	X	X											HPF_corner_CH7
34		X															HPF_EN_CH7
35			X	X	X	X											HPF_corner_CH8
35		X															HPF_EN_CH8

This group of registers controls the characteristics of a digital high pass transfer function applied to the output data, using Equation 3:

$$y(n) = \frac{2^k}{2^k+1}[x(n) - x(n-1) + y(n-1)] \quad (3)$$

Where k is set as described by the HPF_corner registers (one for each channel). Also the HPF_EN bit in each register must be set to enable the HPF feature for each channel.

7.11 BIT-CLOCK PROGRAMMABILITY

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
42										X	X						PHASE_DDR<1:0>
46	1											X					EN_SDR
46	1		X														FALL_SDR

The output interface of the ADS5292 is generally a DDR interface, with the LCLK rising edge and falling edge transitions in the middle of alternate data windows. This default phase is shown in Figure 51.

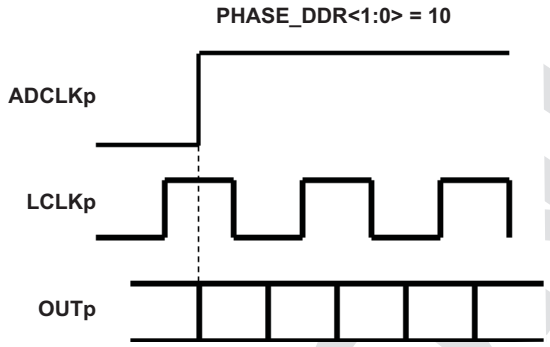


Figure 51. Default Phase of LCLK

The phase of LCLK is programmed relative to the output frame clock and data using bits PHASE_DDR<1:0>. The LCLK phase modes are shown in Figure 52.

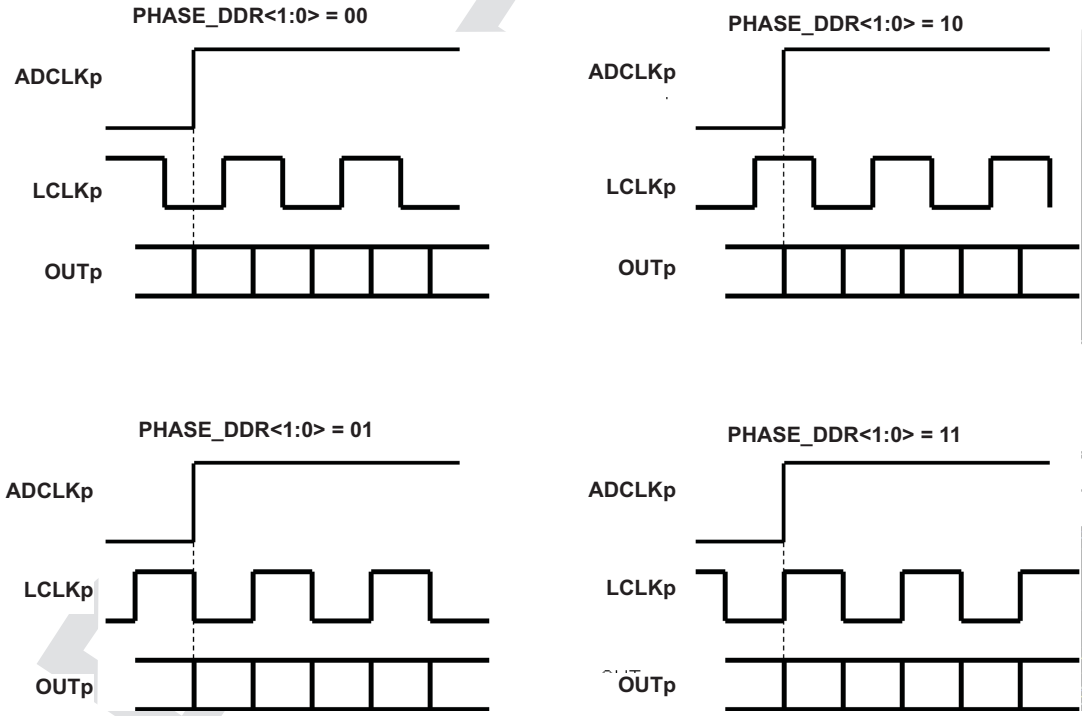


Figure 52. Phase Programmability Modes for LCLK

In addition to programming the phase of the LCLK in the DDR mode, the device also operates in SDR mode by setting bit EN_SDR to 1. In the mode, the bit clock (LCLK) is output at 14-times the input clock, or twice the rate as in DDR mode. Depending on the state of FALL_SDR, the LCLK outputs in either of the two manners shown in Figure 53. As seen in Figure 53, only the LCLK rising (or falling edge) is used to capture the output data in SDR mode. The SDR mode does not work well beyond 40 MSPS because the LCLK frequency becomes very high.

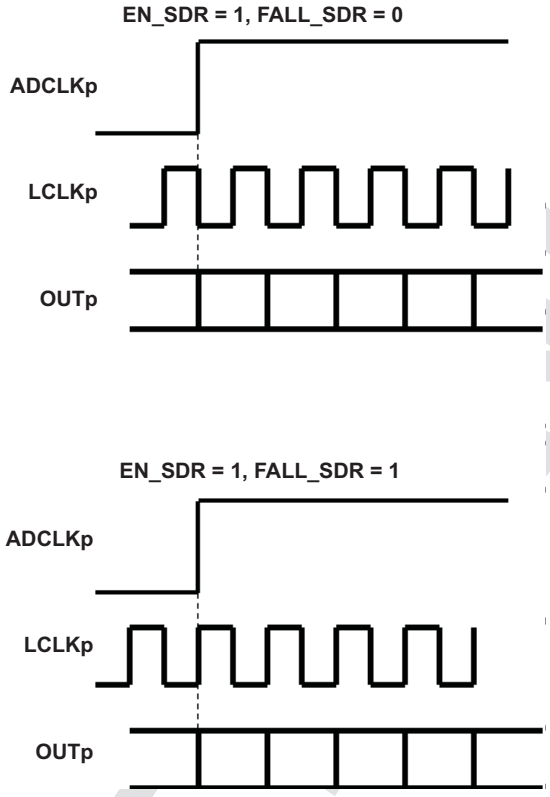


Figure 53. SDR Interface Modes

7.12 OUTPUT DATA-RATE CONTROL

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38															DATA_RATE<1>	DATA_RATE<0>

In the default mode of operation, the data rate at the output of the ADS5292 is at the sampling rate of the ADC which is true even when the custom pattern generator is enabled. In addition, both output data rate and sampling rate are also configured to a sub-multiple of the input clock rate.

With the DATA_RATE<1:0> control, the output data rate is programmed to be a sub-multiple of the ADC sampling rate. This feature lowers the output data rate, for example when the decimation filter is used. Without enabling the decimation filter, the sub-multiple ADC sampling rate feature still is used.

The different settings are listed in the following table.

DATA_RATE<1>	DATA_RATE<0>	Output data rate
0	0	Same as ADC sampling rate
0	1	1/2 of ADC sampling rate
1	0	1/4 of ADC sampling rate
1	1	1/8 of ADC sampling rate

7.13 SYNCHRONIZATION PULSE

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
25	TP_HARD_SYNC															
02			EN_SYNC													

The SYNC pin synchronizes the data output from channels within the same chip or from channels across chips when decimation filters are used with reduced output data rate.

When the decimation filters are used (for example, the decimate by two filter is enabled), then, effectively, the device outputs one digital code for every two analog input samples. If the SYNC function is not enabled, then the filters are not synchronized (even within a chip) which indicates that one channel is sending out codes corresponding to input samples N, N+1 and so on, while another is sending out code corresponding to N+1, N+2 and so on.

To achieve synchronization, the SYNC pulse must arrive at all the ADS529x chips at the same time instant (as shown in the timing diagram of Figure 54).

The ADS5292 generates an internal synchronization signal which is used to reset the internal clock dividers used by the decimation filter.

Using the SYNC signal in this way ensures that all channels output digital codes corresponding to the same set of input samples.

SYNC Timings:

Synchronizing the filters using the SYNC pin is enabled by default. No register bits are required to be written. Even the EN_SYNC bit is not required. For this mode to work, register bit TP_HARD_SYNC must be 0. As shown by Figure 54, the SYNC rising edge is positioned anywhere within the window. The width of the SYNC must be at least one clock cycle.

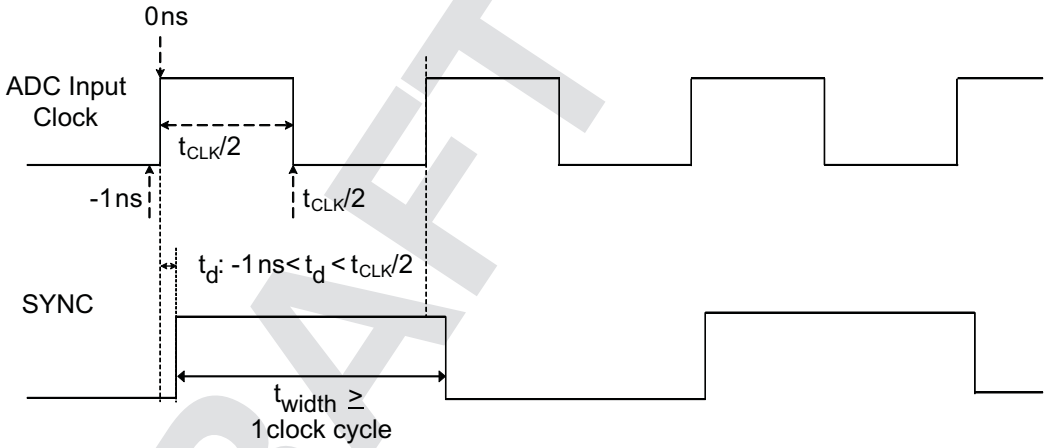


Figure 54. Synchronization Pulse Timing

Note that the SYNC DOES NOT synchronize the sampling instants of the ADC across chips. All channels within a single chip sample the analog inputs simultaneously. To ensure that channels across two chips sample the analog inputs simultaneously, the input clock must be routed to both chips with identical length which ensures that the input clocks arrive at both the chips at the same time. Both chips must be routed for the board design and routing. The SYNC pin cannot be used to synchronize the sampling instants.

In addition to the above, the SYNC also synchronizes the RAMP test patterns across channels. In order to synchronize the test patterns, TP_HARD_SYNC must be set as 1. Setting TP_HARD_SYNC =1 actually disables the sync of the filters.

7.14 External Reference Mode of Operation

The ADS5292 supports an external reference mode of operation in one of two ways:

a. By forcing the reference voltages on the REFT and REFB pins
b. By applying the reference voltage on VCM pin

This mode is used to operate multiple ADS5292 chips with the same (externally applied) reference voltage.

Using the REF pins:

For normal operation, the device requires two reference voltages, REFT and REFB. By default, the device generates these two voltages internally. To enable the external reference mode, set the register bits as shown in Table 6 which powers down the internal reference amplifier and forces the two reference voltages directly on the REFT and REFB pins as VREFT = 1.45 V ± 50 mV and VREFB = 0.45 V ±50 mV.

Note that the relation between the ADC full-scale input voltage and the applied reference voltages is

$$\text{Full-scale input voltage} = 2 \times (\text{VREFT} - \text{VREFB}) \quad (4)$$

Using the VCM pin:

In this mode, an external reference voltage VREFIN is applied to the VCM pin such that

$$\text{Full-scale input voltage} = 2 \times \text{VREFIN} \times (2/3) \quad (5)$$

To enable this mode, set the register bits as shown in Table 6 which changes the function of the VCM pin to an external reference input pin. The voltage applied on VCM must be 1.5 V ±50 mV.

Table 6. External reference function

Function	EN_HIGH_ADDRS(0x1[4])	EN_EXT_REF(0xF0[15])	EXT_REF_VCM(0x42[15, 3])
External reference using the REFT/REFB pins	1	1	00
External reference using the VCM pin	1	1	11

7.15 DATA OUTPUT FORMAT MODES

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
46	1													X			BTC_MODE
46	1												X				MSB_FIRST

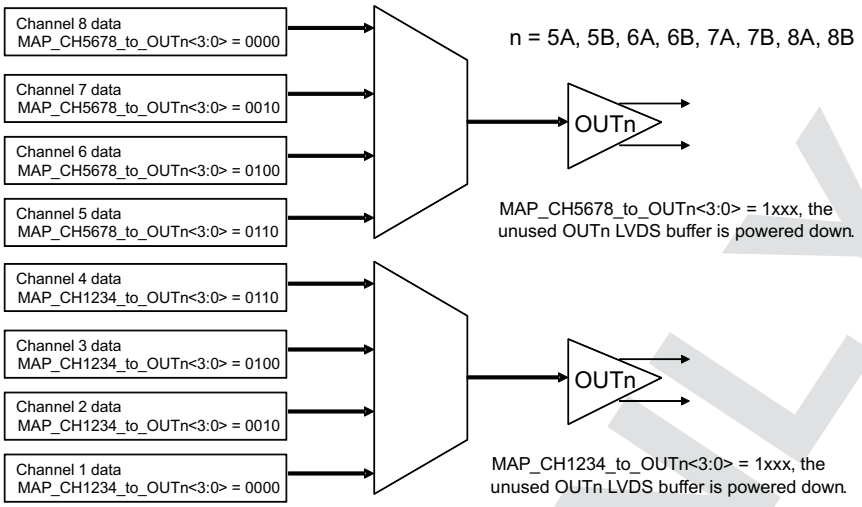
The ADC output, by default, is in straight-offset binary mode. Programming the BTC_MODE bit to '1' inverts the MSB, and the output becomes Binary 2s-complement mode. Also, by default, the first bit of the frame (following the rising edge of CLKP) is the LSB of the ADC output. Programming the MSB_FIRST mode inverts the bit order in the word, and the MSB is output as the first bit following CLKP rising edge.

7.16 PROGRAMMABLE MAPPING BETWEEN INPUT CHANNELS AND OUTPUT PINS

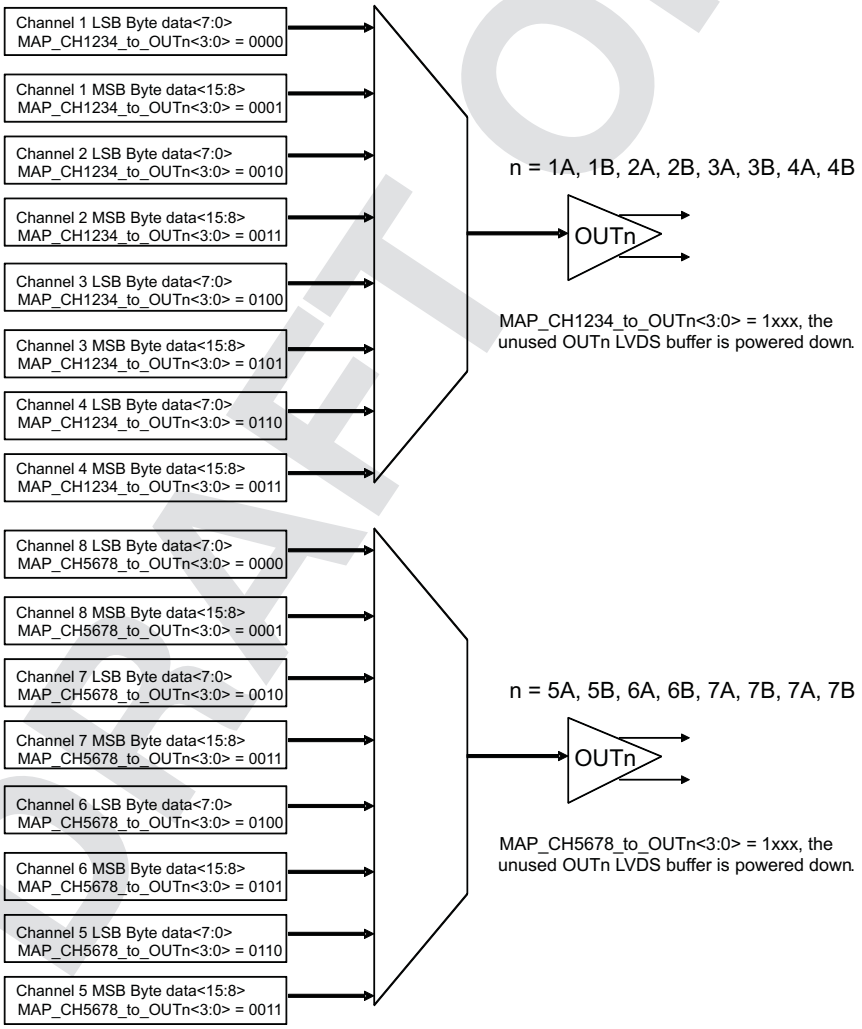
ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
50	1												X	X	X	X	MAP_CH1234_TO_OUT1A
	1								X	X	X	X					MAP_CH1234_TO_OUT1B
	1				X	X	X	X									MAP_CH1234_TO_OUT2A
51	1												X	X	X	X	MAP_CH1234_TO_OUT2B
	1								X	X	X	X					MAP_CH1234_TO_OUT3A
	1				X	X	X	X									MAP_CH1234_TO_OUT3B
52	1												X	X	X	X	MAP_CH1234_TO_OUT4A
	1								X	X	X	X					MAP_CH1234_TO_OUT4B
53	1												X	X	X	X	MAP_CH5678_TO_OUT5B
	1								X	X	X	X					MAP_CH5678_TO_OUT5A
	1				X	X	X	X									MAP_CH5678_TO_OUT6B
54	1												X	X	X	X	MAP_CH5678_TO_OUT6A
	1								X	X	X	X					MAP_CH5678_TO_OUT7B
	1				X	X	X	X									MAP_CH5678_TO_OUT7A
55	1												X	X	X	X	MAP_CH5678_TO_OUT8B
	1								X	X	X	X					MAP_CH5678_TO_OUT8A

The ADS5292 has 16 pairs of LVDS channel outputs. The mapping of ADC channels to LVDS output channels is programmable to allow for flexibility in board layout. The 16 LVDS channel outputs are split in to two groups of eight LVDS pairs. Within each group, four ADC input channels are multiplexed in to the eight LVDS pairs depending on the modes of operation (whether the device is in 1-wire mode or 2-wire mode).

Input channels 1 to 4 map to any of the LVDS outputs OUT1A or OUT1B to OUT4A or OUT4B (using the MAP_CH1234_TO_OUTnA or OUTnB). Similarly, input channels 5 to 8 map to any of the LVDS outputs OUT5A or OUT5B to OUT8A or OUT8B (using the MAP_CH5678_TO_OUTnA or OUTnB). The block diagram of the mapping is listed in Figure 55.



(a) 1-wire mode



(b) 2-wire mode

Figure 55. Input and Output Channel Mapping

Registers 0x50 to 0x55 control the multiplexing options as shown in the following tables.

MAP_CH1234_to_OUTn<3:0>	Mapping	Use in 1-wire mode?	Use in 2-wire mode?
0000	ADC input channel IN1 to OUTn	Y	Y, for LSB byte
0001	ADC input channel IN1 to OUTn (2-wire only)	N	Y, for MSB byte
0010	ADC input channel IN2 to OUTn	Y	Y, for LSB byte
0011	ADC input channel IN2 to OUTn (2-wire only)	N	Y, for MSB byte
0100	ADC input channel IN3 to OUTn	Y	Y, for LSB byte
0101	ADC input channel IN3 to OUTn (2-wire only)	N	Y, for MSB byte
0110	ADC input channel IN4 to OUTn	Y	Y, for LSB byte
0111	ADC input channel IN4 to OUTn (2-wire only)	N	Y, for MSB byte
1xxx	LVDS output buffer OUTn is powered down		

MAP_CH5678_to_OUTn<3:0>	Mapping	Use in 1-wire mode?	Use in 2-wire mode?
0000	ADC input channel IN8 to OUTn	Y	Y, for LSB byte
0001	ADC input channel IN8 to OUTn (2-wire only)	N	Y, for MSB byte
0010	ADC input channel IN7 to OUTn	Y	Y, for LSB byte
0011	ADC input channel IN7 to OUTn (2-wire only)	N	Y, for MSB byte
0100	ADC input channel IN6 to OUTn	Y	Y, for LSB byte
0101	ADC input channel IN6 to OUTn (2-wire only)	N	Y, for MSB byte
0110	ADC input channel IN5 to OUTn	Y	Y, for LSB byte
0111	ADC input channel IN5 to OUTn (2-wire only)	N	Y, for MSB byte
1xxx	LVDS output buffer OUTn is powered down		

The default mapping for 1-wire and 2-wire modes is shown in Table 7 and Table 8.

Table 7. Mapping for 1-wire Mode

Analog Input channel	LVDS Output
Channel IN1	OUT1A
Channel IN2	OUT2A
Channel IN3	OUT3A
Channel IN4	OUT4A
Channel IN5	OUT5A
Channel IN6	OUT6A
Channel IN7	OUT7A
Channel IN8	OUT8A
Note: In the single-wire mode, with default register settings, ADC data is available only on OUTnA.	

Table 8. Mapping for 2-wire Mode

Analog Input channel	LVDS Output
Channel IN1	OUT1A, OUT1B
Channel IN2	OUT2A, OUT2B
Channel IN3	OUT3A, OUT3B
Channel IN4	OUT4A, OUT4B
Channel IN5	OUT5A, OUT5B
Channel IN6	OUT6A, OUT6B
Channel IN7	OUT7A, OUT7B
Channel IN8	OUT8A, OUT8B
Note: In the 2-wire mode, the ADC data is available on both OUTnA and OUTnB.	

7.17 PLL Operation Versus LVDS Timing

The ADS5292 uses a PLL that automatically changes configuration to one of four states depending on the sampling clock frequency. The clock frequency detection is automatic and each time the sampling frequency crosses a threshold, the PLL changes the configuration to a new state. The PLL remains in the new state for a range of clock frequencies. To prevent unwanted toggling of the PLL state around a threshold, the circuit has an built-in hysteresis. The ADS5292 has three thresholds over the sampling clock frequency range from 10 MHz to 80 MHz and can therefore be in one of four states as shown by Figure 56.

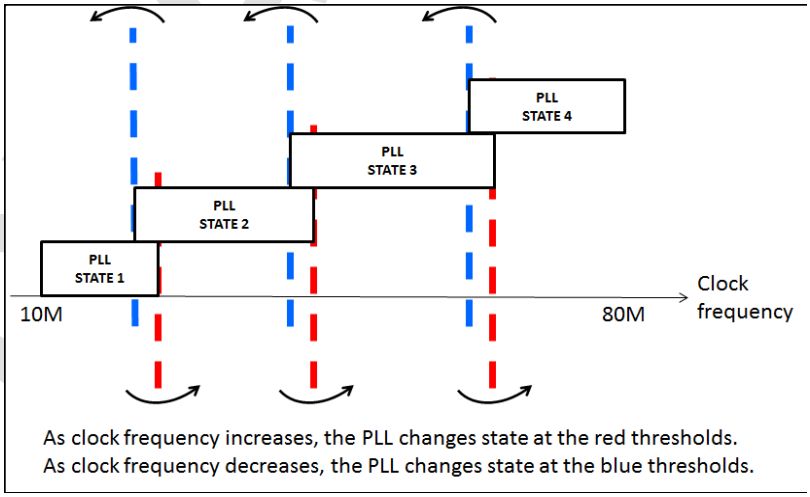


Figure 56. PLL States Versus ADC Fs

PLL Operation Versus LVDS Timing (continued)

Each threshold shifts by a small amount across temperature. On power-up, depending on the clock frequency, the PLL settles in one of the four states. Later, as the system warms up, the PLL changes state once due to the shift in the threshold across temperature.

7.17.1 Effect on Output Timings

The PLL state change affects the output LVDS timings. In some settings, the setup time decreases by 100 ps typical with a corresponding increase in the hold time.

In applications where a timing calibration occurs at the system level once after power up, this subsequent change of the PLL state is undesirable. The ADS5292 has register options to disable the automatic switch of the PLL state based on the detected frequency. To prevent this variation in output timing, disable the PLL from switching states.

In addition to disabling the auto-switching, setting the PLL to the correct state , depending on the sample clock frequency used in the system, is also required. The following sequence of register writes must be followed exactly:

- Step 1: Enable test-mode access by writing register data = 0x0010 in address 0x01 (for example: enable the access to registers with address higher than 0xF0).
- Step 2: Configure the PLL to the correct state depending on the clock frequency of operation and the decimation factor, as per below tables.

NOTE

For certain sampling frequencies, there two PLL states are possible, both of which are stable. In such cases, the higher PLL state results in a better setup time compared to a lower PLL state. For example, at 80 MSPS, with decimation by two enabled, the PLL may be in states 3 or 4. However, the setup time value specified in (0.43 ns minimum) is in PLL state 4. In state 3, the setup time is reduced further by 100 ps typical (with the hold time being correspondingly higher).

Table 9. PLL Configuration When Decimation is Disabled

ADC Fs (MSPS)	Function	Register Address	Register Data
Fs ≤ 12	Disable PLL auto state switch & put PLL in state 1	0xD1	0x0040
9 ≤ Fs ≤ 24	Disable PLL auto state switch & put PLL in state 2	0xD1	0x00C0
18 ≤ Fs ≤ 42	Disable PLL auto state switch & put PLL in state 3	0xD1	0x0140
Fs ≥ 28	Disable PLL auto state switch & put PLL in state 4	0xD1	0x0240

Table 10. PLL Configuration When Decimation by 2 is Used

ADC Fs	Function	Register Address	Register Data
Fs ≤ 24	Disable PLL auto state switch & put PLL in state 1	0xD1	0x0040
18 ≤ Fs ≤ 48	Disable PLL auto state switch & put PLL in state 2	0xD1	0x00C0
36 ≤ Fs ≤ 80	Disable PLL auto state switch & put PLL in state 3	0xD1	0x0140
Fs ≥ 56	Disable PLL auto state switch & put PLL in state 4	0xD1	0x0240

Table 11. PLL Configuration When Decimation by 4 is Used

ADC Fs	Function	Register Address	Register Data
Fs ≤ 48	Disable PLL auto state switch & put PLL in state 1	0xD1	0x0040
36 ≤ Fs ≤ 80	Disable PLL auto state switch & put PLL in state 2	0xD1	0x00C0
Fs ≥ 72	Disable PLL auto state switch & put PLL in state 3	0xD1	0x0140

Table 12. PLL Configuration When Decimation by 8 is Used

ADC Fs	Function	Register Address	Register Data
Fs ≤ 80	Disable PLL auto state switch & put PLL in state 1	0xD1	0x0040
72 ≤ Fs ≤ 80	Disable PLL auto state switch & put PLL in state 2	0xD1	0x00C0

8 APPLICATION INFORMATION

8.1 THEORY OF OPERATION

The ADS5292 is an octal-channel high-speed ADC with sample rate up to 80 MSPS that runs off a single 1.8-V supply. The output resolution is configured as 14-bit,12-bit, and 10-bit if necessary. At 12-bit output resolution, this ADC achieves 70-dBFS SNR at 80 MSPS. When the output resolution of the ADS5292 is 14 bit and 10 bit, SNR of 72 dBFS and 61 dBFS (respectively) is achieved.

All eight channels of the ADS5292 simultaneously sample the analog inputs at the rising edge of the input clock. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock, edge the sample propagates through the pipeline resulting in a data latency of 11 clock cycles.

The 14/12/10 data bits of each channel are serialized and sent out in either 1-wire (one pair of LVDS pins are used) or 2-wire (two pairs of LVDS pins are used) mode, depending on the LVDS output rate. When the data is output in the 2-wire mode, it reduces the serial data rate of the outputs, especially at higher sampling rates. Hence, low-cost FPGAs are used to capture 80-MSPS/12-bit data. Alternately, at lower sample rates, the 12-bit data is output as a single data stream over one pair of LVDS pins (1-wire mode), for example Fs<=65MSPS. The device outputs a bit clock at 7x and frame clock at 1x times the sample frequency in the 14-bit mode.

8.2 ANALOG INPUT

The analog inputs consist of a switched-capacitor-based differential sample-and-hold architecture. This differential topology results in very good AC performance even for high input frequencies at high sampling rates. The INP and INM pins are internally biased around a common-mode voltage of Vcm (0.95 V). For a full-scale differential input, each input pin (INP and INM) must swing symmetrically between Vcm + 0.5 V and Vcm – 0.5 V, resulting in a 2 V_{PP} differential input swing. Figure 57 illustrates the equivalent circuit of the input sampling circuit.

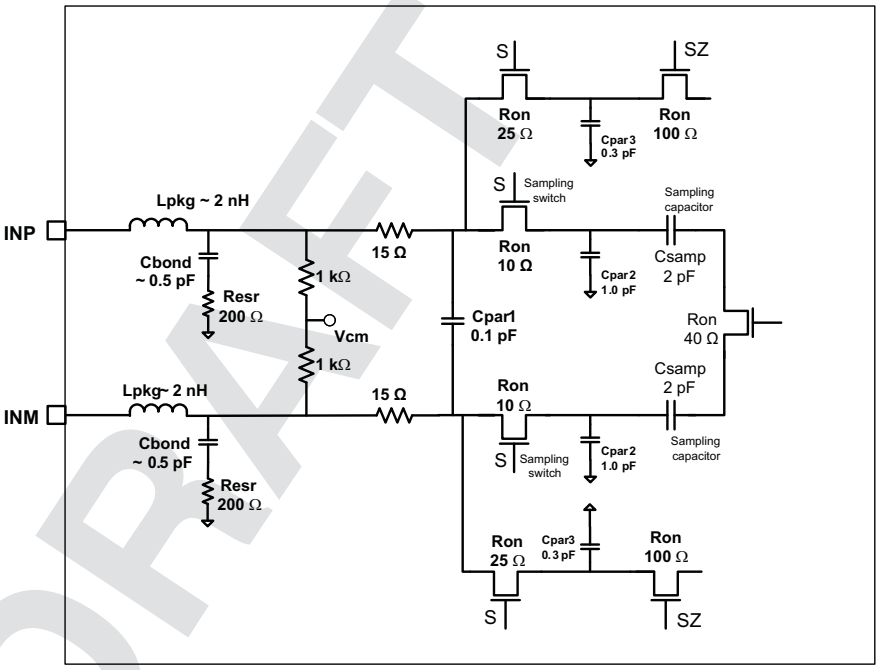


Figure 57. Analog Input Circuit Model

8.3 DRIVE CIRCUIT

For optimum performance, the analog inputs must be driven differentially which improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp-out ringing caused by package parasitic.

DRIVE CIRCUIT (continued)

The drive circuit shows an R-C filter across the analog input pins. The purpose of the filter is to absorb the glitches caused by the opening and closing of the sampling capacitors.

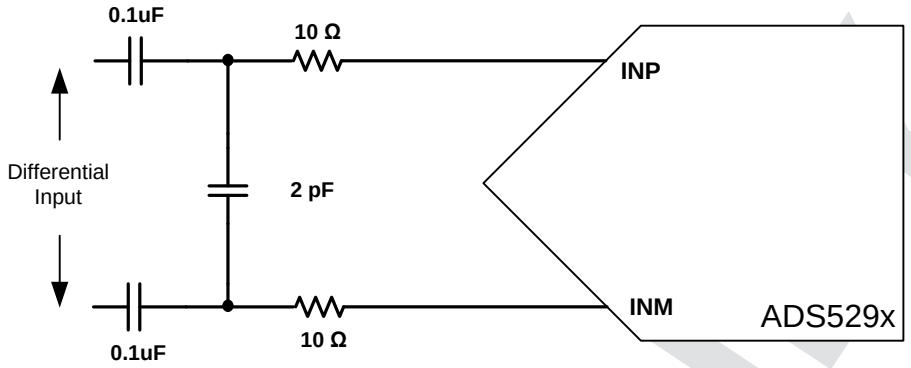


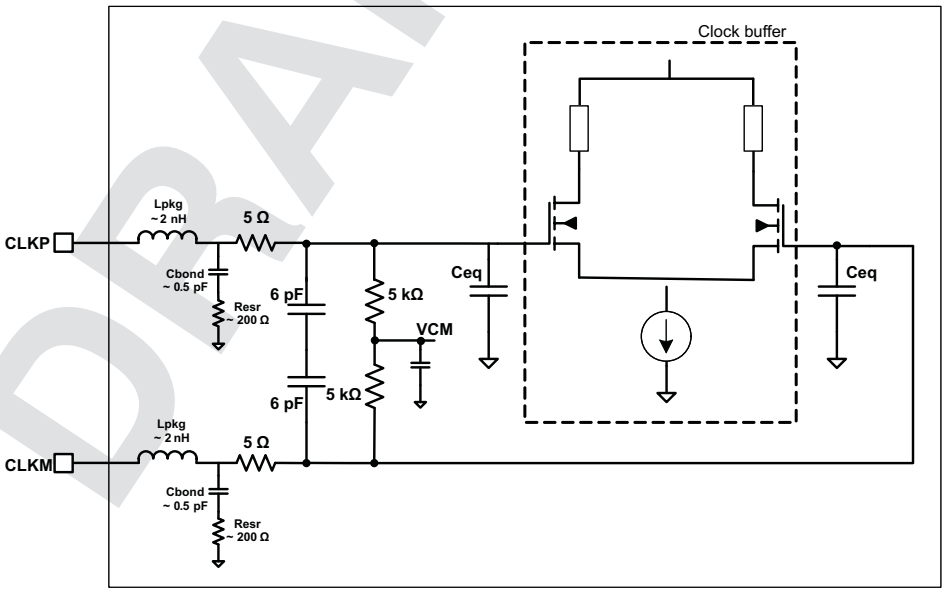
Figure 58. Drive Circuit

8.4 Large and Small Signal Input Bandwidth

The small signal bandwidth of the analog input circuit is high, around 550 MHz. When using an amplifier to drive the ADS5292, the total noise of the amplifier up to the small signal bandwidth must be considered. The large signal bandwidth of the device depends on the amplitude of the input signal. The ADS5292 supports 2 VPP amplitude for input signal frequency up to 80 MHz. For higher frequencies (80 MHz), the amplitude of the input signal must be decreased proportionally. For example, at 160 MHz, the device supports a maximum of 1-VPP signal.

8.5 INPUT CLOCK

The ADS5292 is configured by default to operate with a single-ended input clock. CLKP is driven by a CMOS clock and CLKM is tied to GND. The device automatically detects a single-ended or differential clock. If CLKM is grounded, the device treats the clock as a single-ended clock. Operating with a low-jitter differential clock usually gives better SNR performance, especially at input frequencies greater than 30 MHz. Typical clock termination structures are listed in Figure 59 and Figure 60. Please note the location of LVDS Rterm depends on the LVDS clock driver as well. Some clock devices require the Rterm at the left side of AC-coupling capacitors.



Ceq is approximately 1 to 3 pF, equivalent input capacitance of clock buffer.

Figure 59. Equivalent Circut of the Input Clock Circuit

INPUT CLOCK (continued)

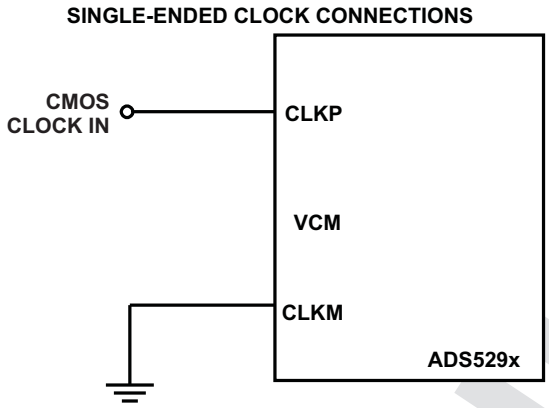
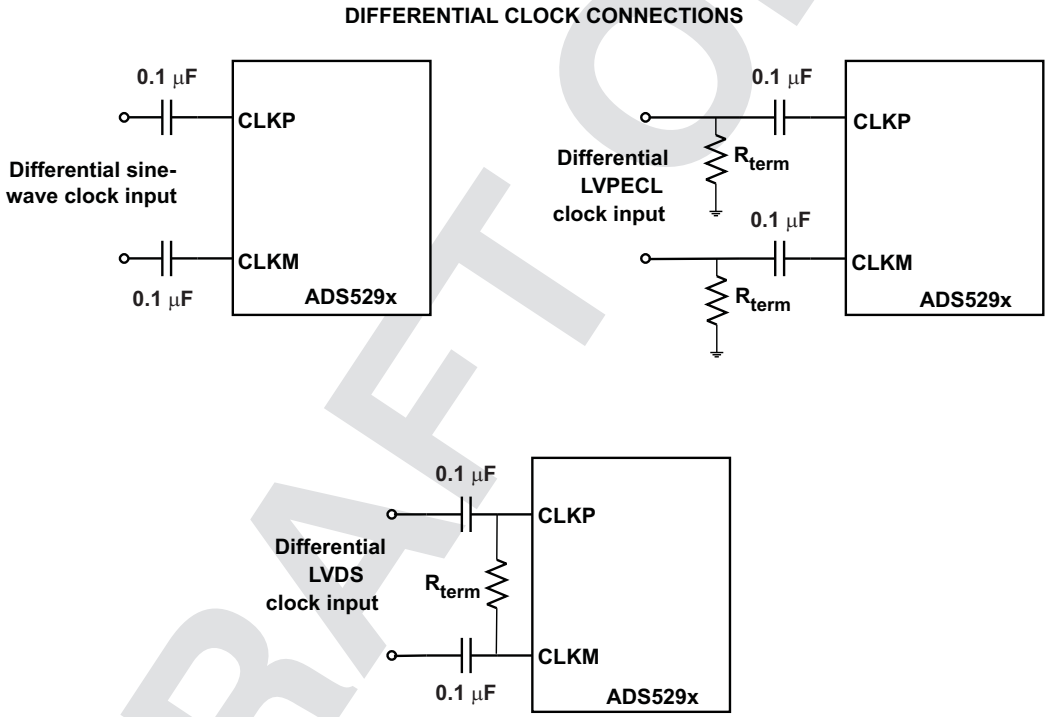


Figure 60. Drive Circuit

8.6 DIFFERENTIAL CLOCK CONNECTIONS



8.7 DIGITAL HIGH-PASS IIR FILTER

DC offset is often observed at ADC input signals. For example, in ultrasound applications, the DC offset from variable Gain amplifier (VGA) varies at different gains. Such a variable offset can introduce artifacts in ultrasound images especially in Doppler modes. Analog filter between ADC and VGA can be used with added noise and power. Digital filter achieves the same performance as analog filters and has more flexibility in fine tuning multiple characteristics.

The ADS5292 includes optional first-order digital high-pass (HP) IIR filter. Figure 61 shows the device block diagram and transfer function.

$$y(n) = \frac{2^k}{2^k+1}[x(n) - x(n-1) + y(n-1)] \quad (6)$$

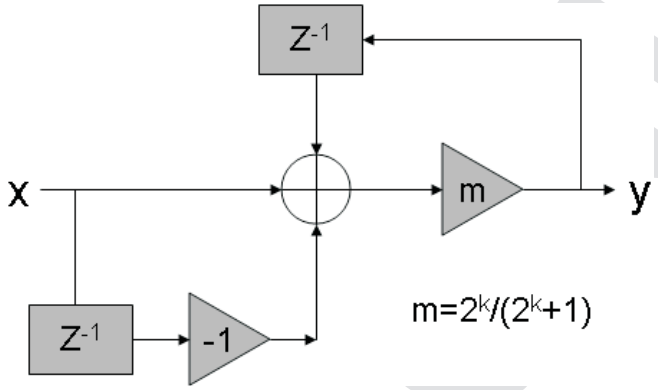


Figure 61. HP Filter Block Diagram

Figure 62 shows the characteristics at K = 2 to 10.

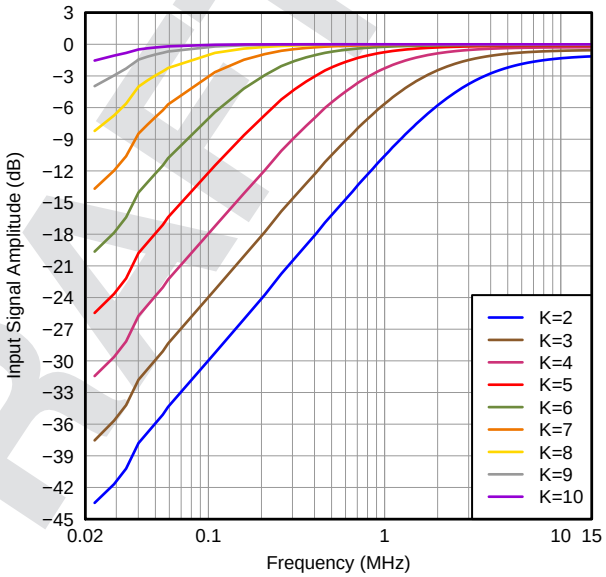


Figure 62. HP Filter Amplitude Response at K = 2 to 10

8.8 DECIMATION FILTER

The ADS5292 includes an option to decimate the ADC output data using filters. Once the decimation is enabled, the decimation rate and frequency band of the filter can be programmed. In addition, the user can select either the pre-defined or custom coefficients.

Table 13. Digital Filters

DECIMATION	TYPE OF FILTER	<DATA RATE>	FILTERn RATE>	<FILTERn COEFF SET>	<ODD TAP>	<USE FILTER CHn>	<EN CUSTOM FILT>
Decimate by 2	Built-in **low-pass odd-tap** filter (pass band = 0 to f_S / 4)	001	000	000	1	1	0
	Built-in **high-pass odd-tap** filter (pass band = 0 to f_S / 4)	001	000	001	1	1	0
Decimate by 4	Built-in **low-pass even-tap** filter (pass band = 0 to f_S / 8)	010	001	010	0	1	0
	Built-in first **band pass even tap** filter(pass band = f_S / 8 to f_S / 4)	010	001	011	0	1	0
	Built-in second **band pass even tap** filter(pass band = f_S / 4 to 3 f_S / 8)	010	001	100	0	1	0
	Built-in **high pass odd tap** filter (pass band = 3 f_S / 8 to f_S / 2)	010	001	101	1	1	0
Decimate by 2	Custom filter (user-programmable coefficients)	001	000	000	0 and 1	1	1
Decimate by 4	Custom filter (user-programmable coefficients)	010	001	000	0 and 1	1	1
Decimate by 8	Custom filter (user-programmable coefficients)	011	100	000	0 and 1	1	1
Bypass decimation	Custom filter (user-programmable coefficients)				0 and 1	1	1
Note: EN_CUSTOM_FILT is the D15 of register 5A (Hex) to B9 (Hex).							

8.9 DECIMATION FILTER EQUATION

In the default setting, the decimation filter is implemented as a 24-tap FIR filter with symmetrical coefficients (each coefficient is 12-bit signed). By setting the register bit **<ODD TAPn>** = 1, a 23-tap FIR is implemented

8.9.1 Predefined Coefficients

The built-in filters (low-pass, high-pass, and band-pass) use predefined coefficients. The frequency responses of the built-in decimation filters with different decimation factors are shown in Figure 63 and Figure 64.

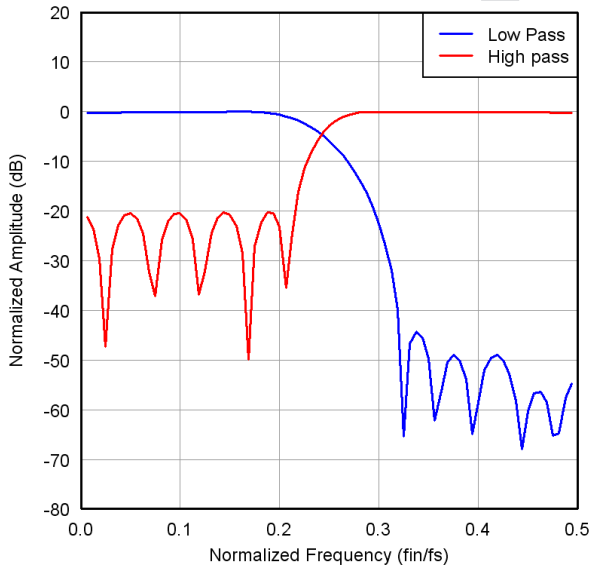


Figure 63. Filter Response, Decimate by 2

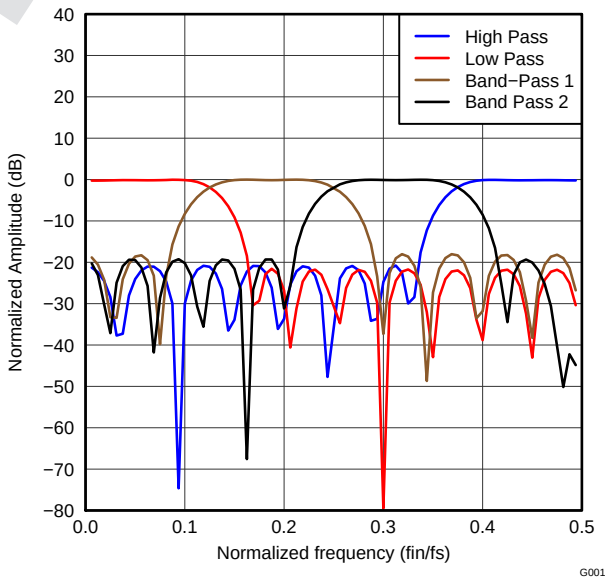


Figure 64. Filter Response, Decimate by 4

DECIMATION FILTER EQUATION (continued)

8.9.2 Custom Filter Coefficients

The filter coefficients are also programmed, or customized, by the user. For custom coefficients, set the register bit **<FILTER COEFF SELECT>** and load the coefficients (h_0 to h_{11}) in registers 0x5A to 0xB9, using the serial interface as:

Register content = real coefficient value x 211 (such as a 12-bit signed representation of real coefficient).

8.10 Board Design Considerations

8.10.1 Grounding

A single ground plane is sufficient to give good performance, provided that the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS5292EVM Evaluation Module* (SLAU355) for placement of components, routing, and grounding.

8.10.2 Supply Decoupling

Because the ADS5292 already includes internal decoupling, minimal external decoupling can be used without loss in performance. For example, the ADS5292EVM uses a single 0.1-µF decoupling capacitor for each supply which is placed close to the device supply pins.

8.11 Packaging

8.11.1 Exposed Pad

The exposed pad at the bottom of the package is the main path for heat dissipation. Therefore, the pad must be soldered to a ground plane on the PCB for best thermal performance. The pad must be connected to the ground plane through the optimum number of vias.

See TI's thermal Web site at www.ti.com/thermal for additional information.

8.12 DEFINITION OF SPECIFICATIONS

Analog Bandwidth The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay Aperture delay is the delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) Aperture uncertainty is the sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) The INL is the deviation of the ADC transfer function from a best-fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}.
To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.
For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5 / 100) \times FS_{ideal}$ to $(1 + 0.5 / 100) \times FS_{ideal}$.

Offset Error The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. Temperature drift is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (7)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding DC.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (8)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB) ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

DEFINITION OF SPECIFICATIONS (continued)

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (9)$$

Total Harmonic Distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10} \frac{P_S}{P_N} \quad (10)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (11)$$

Voltage Overload Recovery Voltage overload recovery is the number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. Voltage over load recovery is tested by separately applying a sine-wave signal with 6-dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (12)$$

Crosstalk (only for multi-channel ADCs) Crosstalk is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. Crosstalk is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). Crosstalk is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. Crosstalk is typically expressed in dBc.

9 REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2011) to Revision A **Page**

- Changed the document From: Product Preview To: Production 1

Changes from Original (November 2011) to Revision B **Page**

- Changed the description of the SYNC pin 4
- Changed the location of OUT A and OUT B in Figure 5 and Figure 6 14
- Added EN_HIGH_ADDRS to Table 3 29
- Moved EN_EXT_REF From: 0x0F To: 0xF0 in Table 3 34
- Added the section BIT-BYTE-WORD WISE OUTPUT. Added Figure 47 and Figure 48. 37
- Added section DIGITAL PROCESSING BLOCKS 38
- Replaced Table 5 and Table 6 with new Table 5 - Digital Filters 44
- Changed the SYNCHRONIZATION PULSE section 47
- Added the External Reference Mode of Operation section 48
- Added Figure 59 56
- Replaced Table 9 (Decimation Filter Modes) with new Table 13 - Digital Filters 59
- Deleted section: Synchronization Pulse 60

Changes from Revision B (July 2012) to Revision C **Page**

- Updated Figure 1 to 14-Bit ADC 2
- Added note for REFB pin under INT/EXT reference modes. 4
- Added note for REFT pin under INT/EXT reference modes. 4
- Added cross-reference link for VCM pin. 4
- Changed maximum rating of digital input pins RESET, SCLK, SDATA, SYNC, PD,CSZ to 3.6 V. 5
- Changed maximum "MSPS" to "MBPS" 6
- Added a note "14-bit SNR is ensured by design and characterization and not tested in production." 7
- Added Corrected typo "5X" to "6X" and added " (12-bit Output Resolution), Digital Filter Disabled" in the title of Table 1 11
- Added Changed "LVDS output rate" to "ADC CLK Frequency" in Table 1. 11
- Added Added "(12-bit Output Resolution) and Digital Filter Disabled" in the title of Table 2 11
- Added Changed "LVDS output rate" to "ADC CLK Frequency" in Table 2. 11
- Added note after Table 2 : *The above LVDS timing spec is only valid when digital filters are disabled*... 11
- Added reference in Table 3 for Register 38 to *OUTPUT DATA RATE CONTROL* section 33
- Changed the Reg.0x46[11:8] formatting. 33
- Changed the EN_RAMP address from 0x24 to 0x25 in the section of LVDS test patterns. 36
- Changed *Note that these bits are functional only when the GLOBAL_EN_FILTER gets set to 1* in DECIMATION FILTER to *Note that these bits are functional only when the GLOBAL_EN_FILTER gets set to 1 and USE_FILTERn bit is set to 1" in the section of Decimation Filter,*. 43
- Added a note related to EN_CUSTOM_FILT and changed formats in theTable 5 44
- Added × (2/3) to Equation 5 48
- Added register address in Table 6. 48
- Added before *APPLICATION INFORMATION* section 52
- Reworded to "The ADS5292 is an octal-channel high-speed ADC with sample rate up to 80 MSPS that runs off a single 1.8-V supply. The output resolution is configured as 14-bit,12-bit, and 10-bit if necessary. At 12-bit output

resolution, this ADC achieves 70-dBFS SNR at 80 MSPS. When the output resolution of the ADS5292 is 14 bit and 10 bit, SNR of 72 dBFS and 61 dBFS (respectively) is achieved." in THEORY OF OPERATION 55

- Changed " The 14 data bits..." to "The 14/12/10 data bits" in THEORY OF OPERATION 55
- Added " , for example Fs<=65MSPS " in THEORY OF OPERATION 55
- Changed " The device outputs a bit clock at 7x and frame clock at 1x times the sample frequency in the 12-bit mode." to "...14-bit" in THEORY OF OPERATION 55
- Changed Figure 58 and moved the 2-pF cap to the left-hand side of the resistors. 56
- Added a note regarding the location of LVDS Rterm in the section of Input clock. 56
- Added note related to EN_CUSTOM_FILT and changed formats in Table 13 59

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