

LP2980,LP2982,LP2985

Engineers note: Capacitors are key to voltage regulator design



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Engineers note: Capacitors are key to voltage regulator design

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Some 99 percent of the "design" problems associated with linear and switching regulators can be traced directly to the improper use of capacitors: wrong type, wrong value, or incorrect physical placement. Regulator designs sometimes diagnosed as "unstable" are often simply victims of bad layout or inadequate bypassing. Excessive EMI is frequently caused by poor bypassing and failing to snub high-frequency noise generators at the source. This article will cover some of the most common mistakes made and provide solutions.

Switching regulators

The switching regulator is inherently vulnerable to poor capacitor design methodology for the simple reason that all switching regulators draw high peak currents when they switch on. The fundamental question is: Where will that current come from? The answer is a capacitor, and that capacitor had better be a very good one with a minimum amount of inductance between itself and the switch or all kinds of problems will result.

Local bypassing

The basic buck regulator circuit in Figure 1 will be used to illustrate the single most common design mistake made in switching converters: inadequate input support capacitance (sometimes called "local bypassing" because the input capacitor C_{IN} keeps the switch currents confined to a local area on the board). If the input support capacitor is either too small, too far away, or simply not good enough in high frequency performance to provide the switch peak current, there will be serious problems.

When the main switch Q1 turns ON, current must flow along the path shown by the arrows. For the regulator to operate efficiently, there must be a minimum of switching losses which requires a very fast rise time for the current. This current can only be provided by C_{IN} , and that requires that it be a very good high-frequency capacitor with low impedance. Because a fairly large amount of capacitance would be required, this cap would likely be a Tantalum or Aluminum electrolytic designed for HF switching. Of course, the best capacitor in the world is useless if the trace inductance between it and the switch FET is large enough to cause limitations of the rise time of the current. For this reason, all of the power components in a switching converter must be kept physically close and trace inductance kept to a minimum.

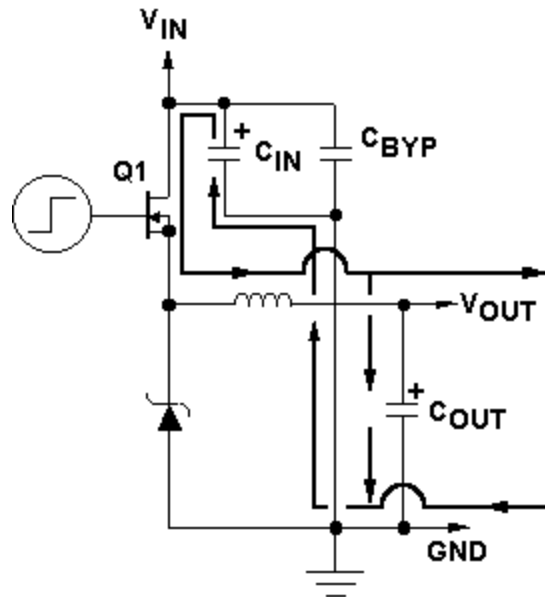


FIGURE 1. BASIC BUCK REGULATOR

RF noise bypassing

When a switch is used to chop a voltage provided by a DC source, a significant amount of noise will be put onto that DC line by the switching converter. To minimize the noise conducted back to the rest of the circuitry through this line, good bypass caps are essential. In Figure 1, it was shown that C_{IN} was used to supply the high peak currents to the FET switch.

The Tantalums and aluminum electrolytics typically used for C_{IN} become fairly reactive at higher frequencies (above a few MHz) because of relatively high ESR (equivalent series resistance) and ESL (equivalent series inductance), and are therefore poor RF bypass capacitors. As shown in Figure 1, C_{IN} must be paralleled by a good ceramic capacitor C_{BY} for RF bypassing to reduce the amount of hash that will be conducted back on the DC source line to other circuitry. Amount and type of capacitor(s) used on the input line of the switching converter is basically application dependent. In some higher current converters, the amount of RF noise on the V_{IN} line at the switching converter input is so high that simply bypassing to ground does not provide enough noise reduction. Then it becomes necessary to add an L-C filter as shown in Figure 2 to prevent this RF from causing problems in other circuitry powered from the same source. It is not always necessary to add a physical inductor to achieve noise reduction, sometimes trace inductance can be used effectively to reduce high frequency noise in conjunction with good ceramic bypass caps placed near the V_{IN} pins of the devices which require clean power.

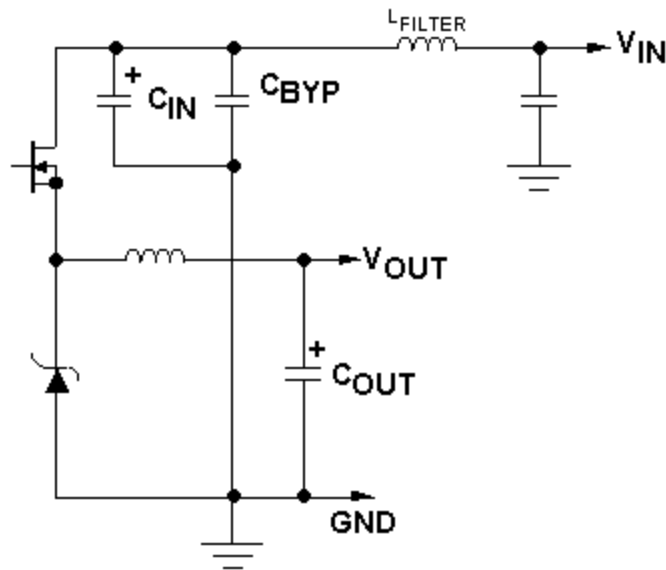


FIGURE 2. EMI FILTER ON V_{IN}

Snubbers

Without question, the best way to handle the problem of RF EMI is to minimize or reduce it at the source. In switching converters, the source of the nastiest EMI is usually the power switch (FET) and the worst EMI is usually when it turns OFF. To understand why, simply refer to figure 1: when Q1 is ON, current flows through the inductor. When Q1 is turned OFF, the voltage on the FET end of the inductor is forced to swing negative until the diode turns ON to hold the current through the inductor constant. A silicon ultra-fast diode can not turn ON in zero time, so the voltage can shoot negative beyond a diode drop and then ring as the diode turns ON.

Even if a Schottky diode is used, parasitic trace inductance will still cause some ringing to occur. This ringing is usually in the 20 MHz to 100 MHz range and generally seems to appear on every circuit node in the lab within ten feet of the board under test. It is "seen" everywhere because the EMI induces a signal directly into the scope probe's ground lead. A good way to reduce this EMI is to add an R-C snubber as shown in Figure 3 (typically a ceramic capacitor and carbon film resistor). It works because when the FET stops sourcing current, the capacitor will source enough current so that the di/dt rate of current fall through the inductor is not as fast. The R-C also damps out the ringing if the component values are appropriately selected. Snubbers have the disadvantage that they reduce overall efficiency by a few percentage points. The loss of efficiency shows up most at light loads because the power they burn is basically constant and relatively independent of output load current, which means the percent of total converter input power consumed by the snubber increases at lighter loads.

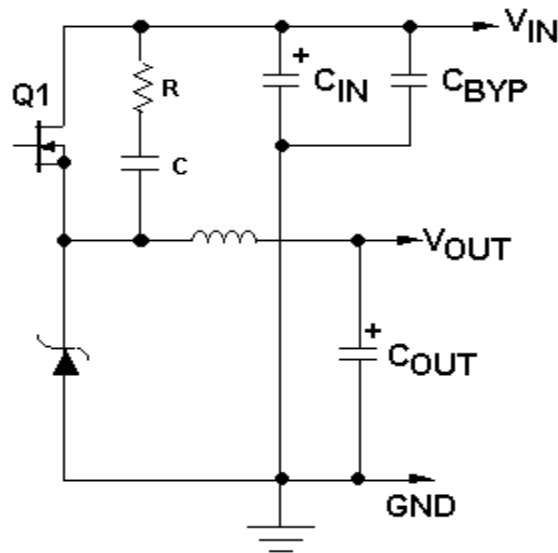


FIGURE 3: R-C SNUBBER REDUCES RF NOISE

Ripple current

The single most commonly made mistake in component selection for capacitors in switching regulators may be in the ripple current specification. Ripple current is the RMS value of the current flowing into and out of the capacitor each time the switch turns ON and OFF. Referring to Figure 1, there is a ripple current flowing in both CIN and COUT. Current flows into and out of CIN as the FET turns on and off, and current flows into and out of COUT as the inductor current charges it and then the capacitor discharges into the load. What must be understood is that the ripple current flows through the ESR (equivalent series resistance) of the capacitor and dissipates power as given by the well known term for power which is:

$$P = I(\text{squared}) * \text{ESR}.$$

Ripple current derivations are not trivial in many switching converters and some designers have been known to solder a 10 milli-Ohm resistor on the ground side of the capacitor in question and snap a scope photo to see what the ripple current actually looks like. Then, a graphical estimate of the RMS value gives a good approximation. The only definitive test of the capacitor selected is to check the temperature rise when operated at full output load current. What is most important to realize is that if you replace a good, high-frequency low-ESR switching cap with a generic aluminum electrolytic it will likely overheat and fail due to the increased power dissipation caused by the ripple current.

Linear regulators

A dangerous precedent was established by the first linear regulator semiconductors sold commercially like the LM7805 type devices: they require no input or output capacitor and are completely stable under virtually any operating conditions. Some of the newer LDO regulators require careful attention to external capacitors to operate in a stable mode. The main reason the 7805 is unconditionally stable is because the power pass transistor was made up of an NPN Darlington as shown in Figure 4. They are usually referred to as “NPN regulators” for this reason, and are comprised of an error amplifier, voltage reference, and NPN Darlington power transistor.

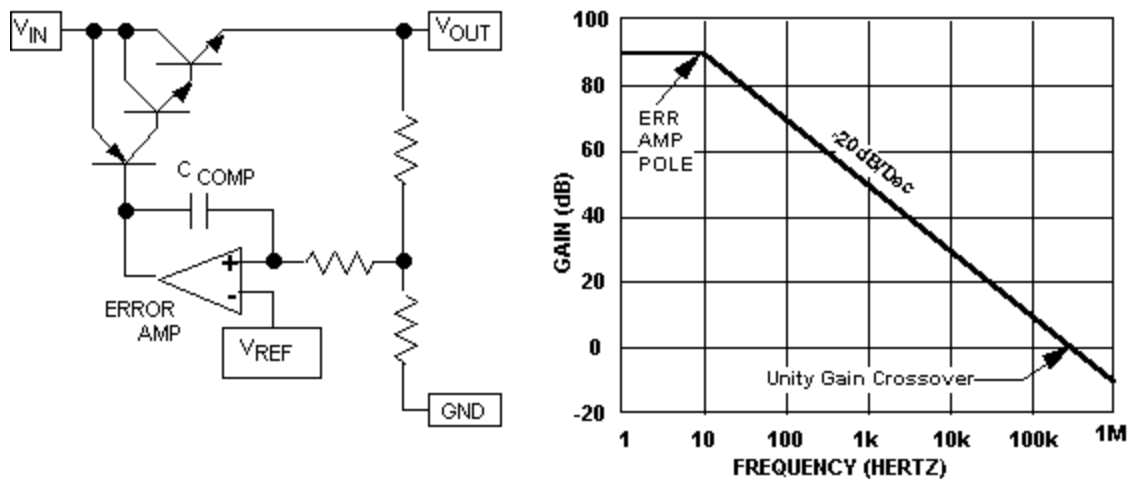


FIGURE 4. NPN REGULATOR AND LOOP GAIN

The NPN regulator drives the load off of the emitter of an NPN transistor in a configuration sometimes called “emitter follower” because the voltage gain from base to emitter is nearly unity, but the current gain is very high. The critical characteristic of the emitter follower is that it is very wide-band and does not introduce low-frequency poles into the loop gain. This makes compensation very easy: “dominant pole” compensation is used by putting a pole into the loop created by the capacitor around the error amplifier. The result is a very low frequency pole (typically around 10 - 100 Hz) causing a 20 dB/decade roll-off out to the unity gain crossover frequency which is typically between about 100kHz and 1 MHz. This shows why no external compensation is required for stability in an NPN regulator.

LDO regulators

NPN regulators are a great product, but as the voltages used in circuits have dropped lower, they have become less attractive because of one reason: dropout voltage. This is defined as the minimum voltage (input-to-output) which must be maintained for the regulator to hold the output in regulation. The standard NPN regulator requires about 2 - 2.5V minimum because of the 2 VBE's + 1 SAT required to operate the NPN Darlington power transistor and PNP driver. The power dissipation caused by the voltage drop across the regulator becomes more and more significant as the regulated output voltage drops. This led directly to the development of the LDO (low dropout) regulator which can operate with as little as a few hundred millivolts across it (see Figure 5).

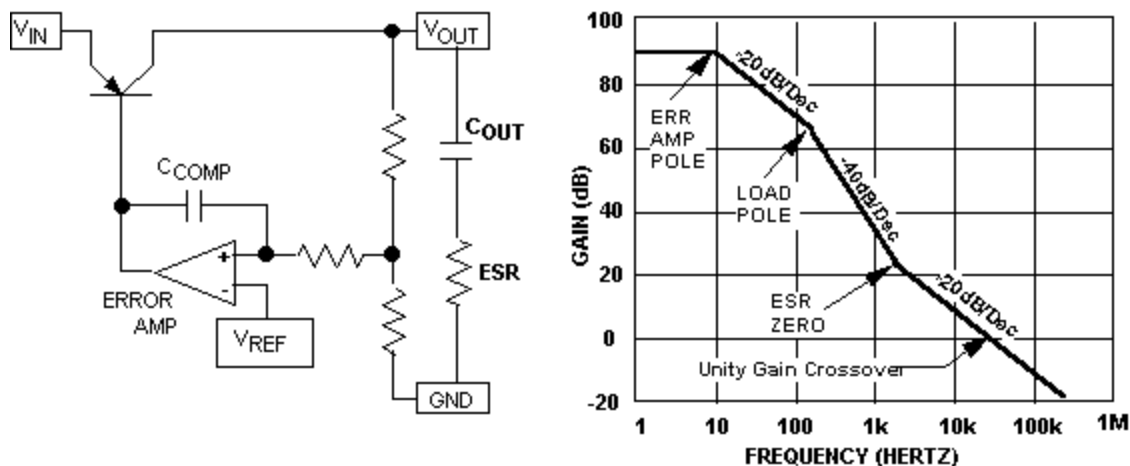


FIGURE 5. LDO REGULATOR AND LOOP GAIN

The LDO regulator (sometimes called a “PNP” regulator) differs from the NPN regulator because the power transistor is a single PNP: the good news is that dropout voltage can be as low as the saturation voltage of the PNP (a few hundred millivolts). However, the single PNP has lower beta compared to the NPN Darlington, so the ground pin current of the LDO regulator is approximately equal to the load current divided by the beta of the PNP. To reduce this current, very good PNP devices have to be fabricated on the IC which have high current gain. The VIP devices used on our LP298X line have typical betas > 100 so the ground pin current is kept very low.

The major difference between the LDO and the NPN regulator is that the LDO must be compensated differently from an NPN regulator. The LDO requires an output capacitor, and the ESR (equivalent series resistance) of that capacitor is integral to stability. The reason for this is because the PNP drives the output off the collector (in a configuration called common-emitter) and has a fairly high output impedance. Because of this, the loop gain has a pole in it (I will refer to as the Load Pole) formed by the output capacitor and the load resistance. The load pole frequency is closely approximated by:

$$f_{LP} = 1 / (2 * \pi * R_L * C_{OUT}).$$

The presence of a second low-frequency pole poses a problem: two poles can result in 180 degree phase shift which will cause oscillations. The solution is to introduce some positive phase lead to cancel out some of the shift from the two poles. This is accomplished using the ESR of the output capacitor. A zero is created by the ESR whose frequency is given by:

$$f_z = 1 / (2 * \pi * ESR * C_{OUT})$$

If the ESR is in the correct range, stable operation will result because it will provide enough phase lead to get sufficient phase margin at the unity gain frequency. If the ESR is too low, the zero doesn't kick in until well past the unity-gain frequency so it does no good. If the ESR is too high, the zero comes in at too low of a frequency and the loop bandwidth will get too wide (and that allows other high-frequency poles to add phase shift and cause oscillations). So, it has to be in the right range. The way we determine the range is to bench test the regulator using a capacitor which has pretty close to zero ESR (surface mount ceramic) and add series resistance values and plot ESR stability curves (Figure 6).

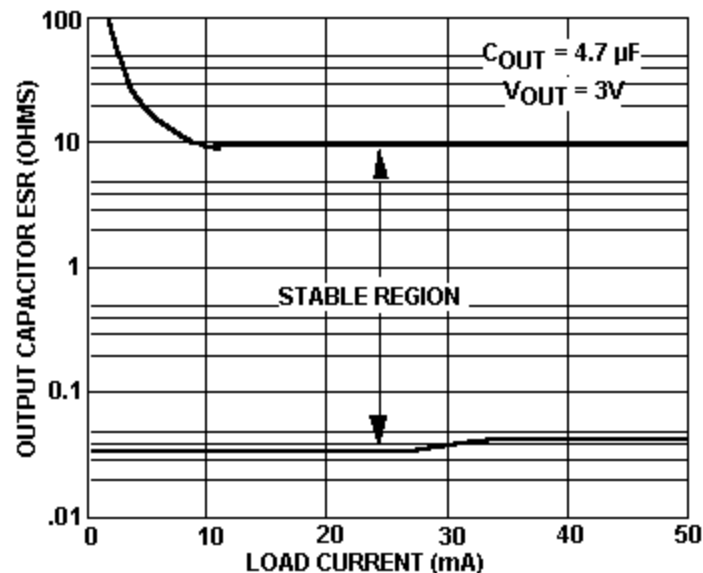


FIGURE 6: STABLE ESR RANGE OF COUT FOR TYPICAL LDO

Figure 6 shows the stable ESR range of the LP2982, which is a low-noise, high-performance LDO regulator. The first thing to notice is that it is a pretty wide range, with greater than 100X from minimum to maximum range value of stable boundaries. The stable zone is centered at around 1 Ohm, which matches very closely with the typical ESR of a Tantalum capacitor of this capacitance value. It would seem the stability limits for the output capacitor are pretty easy to meet, but users sometimes find ways to miss it.

The biggest reasons many LDO's oscillate are:

- a) Using an aluminum electrolytic output capacitor in a design that operates at cold temperatures. Aluminum capacitors may have an ESR in the "stable" range at room temperature, but their ESR increases exponentially as the temperature goes below about 10 degrees Centigrade. These capacitors must never be used with LDO's if cold temperatures can occur in the application.
- b) Using a ceramic output capacitor on an LDO not designed for it. The typical 2.2 - 4.7 uF ceramic capacitor will have an ESR of about 5 milli Ohms. This puts the ESR zero somewhere around 6 MHz where it clearly won't help compensate the loop. Using ceramics on the output of LDO's which are not designed to work with them is presently the #1 reason for unstable LDO operation.

Why most LDO's hate ceramic bypass capacitors

The last section explained why most LDO regulators will not operate in a stable mode with a ceramic output capacitor. Their loop requires the ESR of the output capacitor to supply a zero which gives the phase lead necessary to cancel out the effects of one of the low-frequency poles.... and ceramic capacitors have almost no ESR, so they won't provide any phase lead. Most LDO's designed in the late 1980's and early 1990's were made assuming a Tantalum capacitor would be used for the output capacitor, and so they don't tolerate ceramics very well.

But, there is another "ceramic" oscillation mode so sneaky it deserves it's own section: suppose the LDO has a perfectly suitable output capacitor (say a 2.2 uF Tantalum with a one Ohm ESR) which should be perfectly stable..... and then somebody adds a few 0.01 uF ceramic bypass capacitors on the output rail to help reduce noise. Common sense tells us there should be no problem, after all a few 0.01 uF caps in parallel with a 2.2 uF cap should have no effect. The larger Tantalum should swamp out the effects of a smaller capacitor... or would it?

Unfortunately, most LDO's can tolerate only a small amount of ceramic capacitance (like a few thousand pico Farads) placed directly on the output even when a good Tantalum capacitor is already there. To understand why this is true, it must be remembered that the PNP pass transistor has a relatively high output impedance and looks like a current source driving the output capacitors. This means that two capacitors in parallel with very different ESR values will form a distinct pole/zero set for each individual capacitor. Recalling that the frequency of the pole and zero for EACH capacitor connected to the output can be closely approximated by:

$$f_p = 1 / (2 * \pi * R_L * C_{OUT})$$

$$f_z = 1 / (2 * \pi * ESR * C_{OUT})$$

We can now examine a real-time example of how the small ceramic caps can cause oscillation using the LP2980 which is a 50 mA LDO built on a high-performance bipolar process. Open loop gain is assumed to be about 80dB and the fixed-frequency pole provided by the error amplifier is set at about 200 Hz. An output cap of 2.2uF Tantalum will be used and an ESR value of 1 Ohm will be assumed. Operating at 2.5V out with 50mA load current, that means $R_L = 50$ Ohms. From the above equations, the Tantalum capacitor's load pole will be at 1.4 kHz and the ESR zero will be at 72 kHz. Figure 7 shows the gain and phase plot of this regulator.

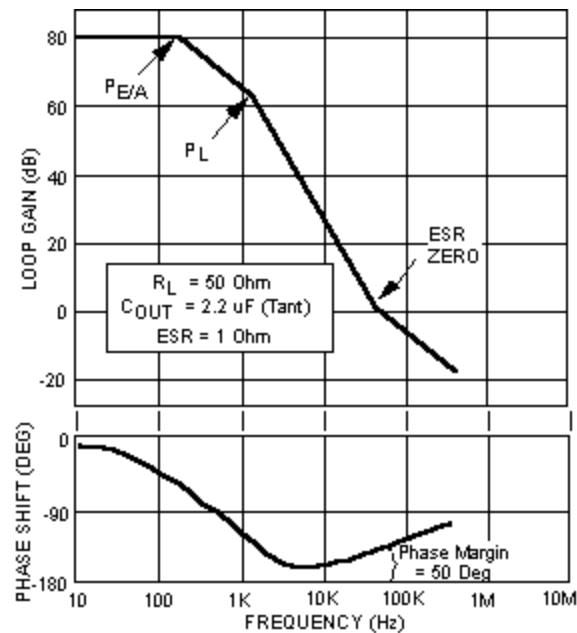


FIGURE 7. STABLE LDO GAIN-PHASE PLOT (WITHOUT CERAMIC CAPS)

Clearly, without ceramic capacitors the circuit is quite stable because it has a phase margin of about 50 degrees. Next, we will study what happens if we add four ceramic bypass capacitors with a value of 0.01 uF each. We will assume an ESR of about 5 milli Ohms for the ceramic capacitors. Since all four of the ceramic capacitors are electrically equivalent, we will model them as a single ceramic capacitor of 0.04 uF. This will form a pole at 79 kHz and a zero at about 300 MHz. Most engineers can see what's coming at this point: the pole from the ceramic capacitors almost exactly cancels out the zero of the Tantalum ESR which is providing the phase lead required to make the loop stable (Figure 8 shows the effects of adding the ceramic capacitors).

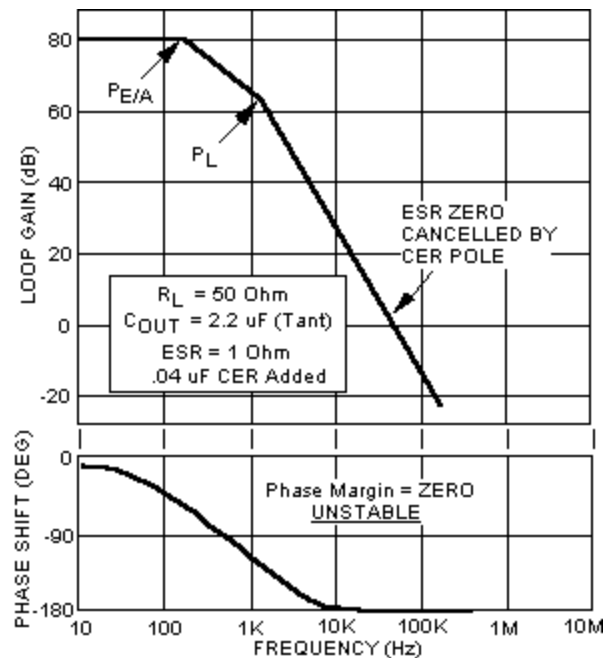


FIGURE 8. LDO MADE UNSTABLE BY CERAMIC BYPASS CAPS

Since the pole from the ceramics wipes out the Tantalum's ESR zero, the two lower frequency poles from the error amplifier and the Tantalum output capacitor will cause a negative 180 degree phase shift and the loop will be completely unstable. It should be noted that in bench testing, this particular device could be made to oscillate with values of ceramic bypass capacitance between 0.002 and 0.003 μF , so it is not necessary to drop the pole exactly on top of the zero to get the phase margin low enough to make the loop oscillate (just getting close can do it).

That explains why we generally recommend against putting ceramics on the output of "Tantalum-only" LDO regulators. If you must use ceramics, keep the amount of capacitance to a minimum and move them physically as far as possible from the output of the LDO, since trace inductance will help to decouple the effect of the ceramic capacitors. This particular susceptibility to small ceramic capacitors is not unique to National Semiconductor's LDO regulators, as nearly all PNP (or P-FET) LDO regulators have similar control loops and similar characteristics in regards to loop gain and phase. They are generally only stable with ceramic capacitors if specifically designed to be (see next section).

LDO's Which Are Stable With Ceramic Output Capacitors

In the late 1990's, ceramic capacitors passed Tantalums as the most optimum choice for capacitor values in the 1 μF to 5 μF range in terms of size, cost, availability, and overall electrical performance. This was due primarily to the development of new ceramic materials which made it possible to fabricate low-voltage ceramics which were extremely small and cheap in values as high as 10 μF .

Because of this, customers demanded LDO regulators be made which were stable using ceramic output capacitors. About 4 years ago, National Semiconductor brought out a low-noise, high performance LDO called the LP2985 which met these requirements. The method used to make the part ceramic-stable was to alter the error amplifier compensation so that it had both the dominant (fixed) pole traditionally used, and also a zero to take the place of the ESR zero which was formerly provided by the Tantalum output capacitor (see Figure 9). A resistor is placed in series with the compensation capacitor in the feedback loop of the error amplifier which adds a zero to the loop gain. Using this technique, the control loop is stable with output capacitance ESR values down to zero Ohms.

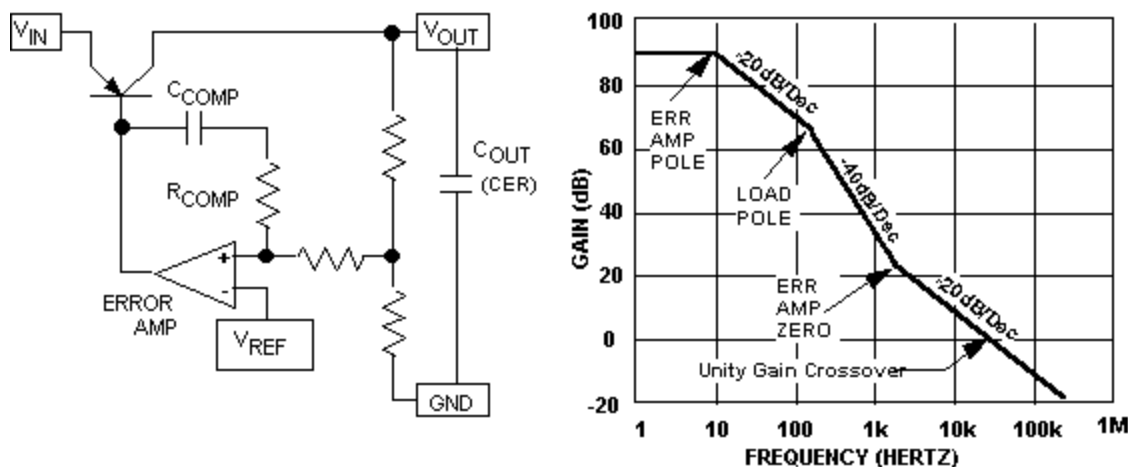


FIGURE 9: CERAMIC-STABLE LDO AND GAIN PLOT

Transient response

An article about the usage of capacitors in the design of linear and switching regulators would not be complete without some information on transient response, defined as the regulator's ability to hold its output in regulation when the load current changes abruptly. Transient response became a very important aspect of design about seven or eight years back as the operating speeds of microprocessor chips increased, demanding both higher current from their supplies and also requiring rails that would stay solid when hit with demands for high peak currents that were virtually instantaneous in time. One particular power supply specification I read required the output to stay within 3 percent of nominal when the load current changed from zero to 15A in 100 nano seconds.

That was pretty scary, but the demands made on the CPU power supply today (and in the near future) will make that look like the good old days.

A few years back, I attended a presentation from another semiconductor manufacturer who was explaining about how their new regulator was going to solve the transient response problem: “The response time of this part is so fast you won't even need capacitors!” The truth is that capacitors were, are and always will be required to provide power in systems with very fast changing load currents. Faster responding regulators (or converters) do provide a way to reduce the total amount of capacitance by shifting more of the energy load from the regulator's output capacitors to the input capacitors. The following information should give the designer a better understanding of the various elements of the transient response design parameters.

The basics of a load transient

The equivalent circuit to understand a load transient is shown in Figure 10. The circuit elements labeled “Lp” represent parasitic inductances in either the PCB traces, component leads, or inductance internal to the capacitors. CBYP is shown without any value of ESR because it is assumed it will be a ceramic capacitor and the ESR will be negligible. It will also be assumed that the load is drawing zero or negligible current, then at time $t = 0$, the load current steps to full load in a very fast rise time. This will result in an output voltage excursion as shown.

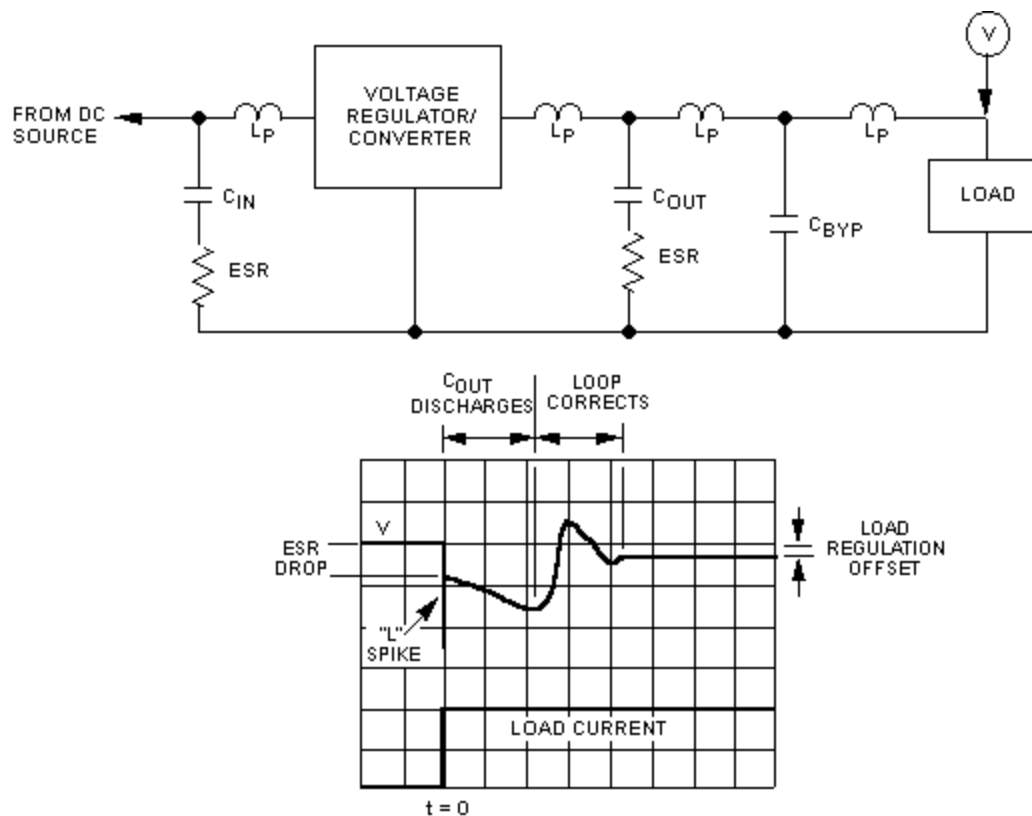


FIGURE 10: TRANSIENT RESPONSE CIRCUIT AND SCOPE PHOTO

Inductance effects

In the initial part of the load transient where the load current is increasing very rapidly, most of the current will be provided by the capacitor shown as CBYP (which may actually be a lot of capacitors in parallel). These are typically ceramic capacitors because they must have absolute minimum ESR (equivalent series resistance) and ESL (equivalent series inductance). To see why inductance must be minimized, it should be understood that a current changing in an inductor forces a voltage drop across it given by:

$$V = L * (di/dt)$$

For this example we will assume that the current rises from zero to 15A in 100 ns. We will assume the output rail voltage to the load is 2.5V, with an allowable worst-case deviation specification of --3 percent. Given these parameters, the maximum inductance between the CBYP and load terminal (including internal ESL and PCB trace inductance) is a maximum of 0.5 nH (or 500 pH).

Board designers minimize inductance through layout. A good example is the CPU on a typical mother board. The CPU chip is plugged into a “cavity” socket which has an air gap under the CPU chip. This space is usually filled with dozens of ceramic capacitors which supply current to the load during very fast transients. Of course since these are ceramics, the total capacitance which can be practically mounted in this small space is limited. The main current to support the load transient must be provided by the output capacitor COUT.

Bulk capacitance

Before the regulator loop registers the need for increased current and starts supplying it, the majority of the current supplied to the load must be provided by COUT, sometimes called bulk capacitance. These are normally aluminum electrolytic capacitors, which are optimized for low ESR and very low high-frequency impedance (which means they are more expensive than standard AL caps). On a motherboard, these caps are usually sitting right next to the CPU socket. Note that as the current begins to flow out of COUT, the voltage at the terminal of COUT will be decreased by the value of:

$$V_{ESR} = I_L * ESR.$$

This is the reason the output voltage shows a “step” down in voltage right after the “L” spike occurs. As COUT continues to supply current, the voltage across COUT discharges at a rate given by:

$$I_L = C * (dV/dt)$$

We can estimate how much bulk capacitance would be needed in this particular example if we assume the loop will kick the power converter or regulator “ON” in about 20 us. Further, we will assume that the output may only discharge 3% of the 2.5V rail in those 20 us (the ESR drop will be neglected for this calculation). If the 15A current is to be delivered for 20 us and the voltage drop not more than 75 mV, then a capacitance of at least 4000 uF must be provided.

Designing in this much capacitance using very good Al capacitors is fairly costly, and highlights the reason faster regulators and converters are so important in designs that must maintain regulation when hit by fast-rising, high-current transients. The amount of bulk capacitance required at COUT is directly proportional to how long it takes the regulator or power converter to turn on the power device and supply load current from CIN. By transferring more of the load support back to CIN, the total amount of bulk capacitance required by the system is reduced since a larger voltage change at CIN can be allowed because the regulator will correct for it.

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