Sean Grotle
Aaron Paxton
Mike Hartshorne

TI Precision Designs: Verified Design
6A Current-Sharing Dual LDO

TI Precision Designs

TI Precision Designs are analog solutions created by TI's analog experts. Verified Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

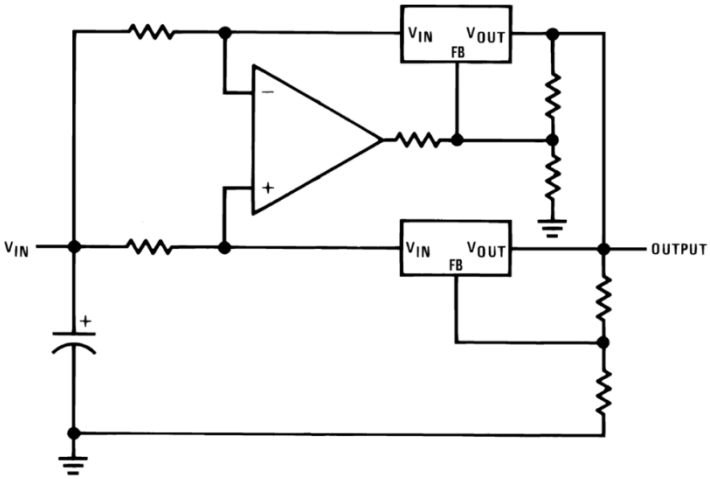
Design Archive	All Design files
TINA-TI™	SPICE Simulator
TPS74401	Product Folder
OPA333	Product Folder

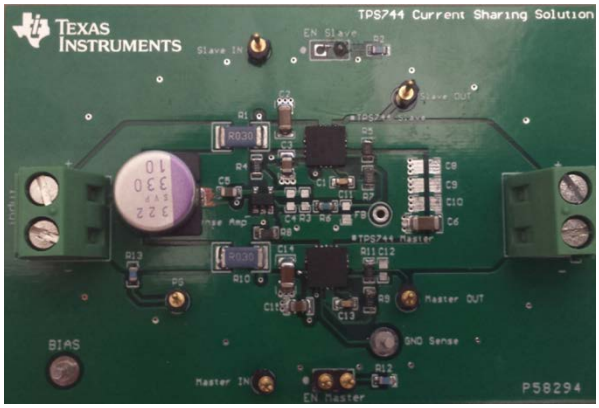
Circuit Description

This power supply topology is capable of sourcing 6A via two LDOs operating in parallel. The solution sources current evenly between the two TPS74401's, each capable of supplying 3A. This design allows for higher currents to be supplied than is typically possible with a single LDO. It also allows for additional heat syncing not available with an individual LDO.

TI E2E™ Community

Ask The Analog Experts
WEBENCH® Design Center
TI Precision Designs Library





1 Design Summary

The design requirements are as follows:

- Input Voltage: 0.9V - 5.5V
- Bias Voltage: 2.375 – 5.25V
- Output Current: up to 6A

The design goals and measured performance are summarized in Table 1.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Current Mismatch	0%	0%	<2%
Low Noise (100Hz – 100kHz)	(16 x V_{OUT}) μV_{RMS}	-	(17 x V_{OUT}) μV_{RMS}
PSRR @ 100kHz, 6A	30dB	-	40dB

Figure 1 depicts the measured startup.

Output = 3.3V
Input = 0V to 5V
Bias = Vin
I_{LOAD} = 6A
C_{SS} = 10nF
C_{IN} = 330µF and10µF
C_{OUT} = 100µF
C_{BIAS} = 1µF

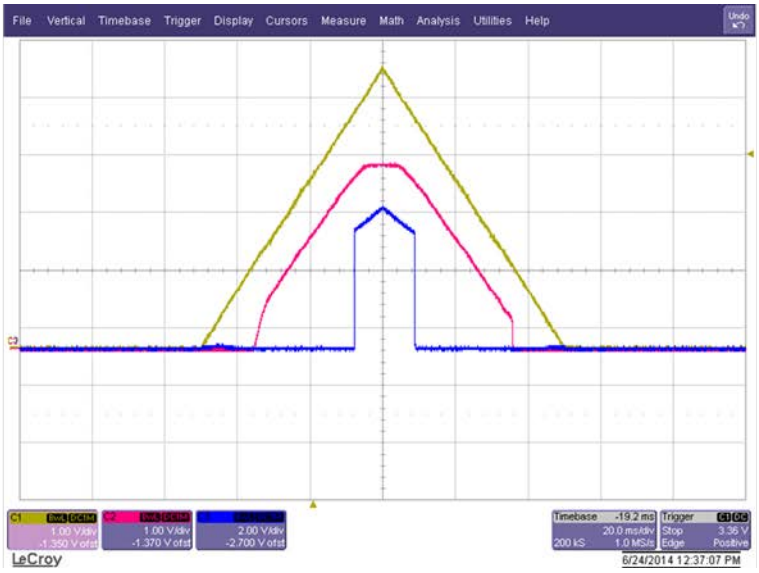


Figure 1: Measured Startup

2 Theory of Operation

A Current-Sharing Dual LDO power supply is desirable when the current sourced by a single LDO is inadequate or the heat dissipated from a single LDO will exceed maximum die temperature. A current-sharing configuration allows two LDOs to regulate the same voltage in parallel, thereby splitting the current being sourced equally between the two regulators. Consequently, this allows the supply to source twice the current than would be possible with a single LDO. The thermal dissipation resulting from regulation will also be more spread out than the same thermal dissipation occurring in a single LDO. This property can be important in closed environments where air flow is restricted.

This method is a preferable solution over a switched-mode power supply when the noise resulting from switching is unacceptable. A Current-Sharing Dual LDO power supply retains the noise characteristics of its individual LDOs. This allows it to generate a low-noise rail without the need for additional filtering by means of passive components. Its low-noise properties also make it a good candidate to follow switched-mode power supplies as a means of filtering undesirable ripple.

2.1 The Ideal, but Flawed, Approach

Before the theory of operation is explained, it is helpful to take a look at why it is not possible to put two LDOs in parallel with one another by simply tying their inputs and outputs. This configuration is depicted in Figure 2.

There are several reasons why this simple approach does not work: Although the two LDOs are the same model, there are slight variations when it comes to their internal components. State-of-the-art manufacturing seeks to minimize these variations but cannot eliminate them entirely. As a result, the internal bandgap, FET, and error amplifier have subtle differences across devices. Although the two LDOs use the same resistor feedback network in this configuration, these differences in internal components will cause the two LDOs to regulate slightly different output voltages. As such, the LDO with the higher output voltage will become dominant over the other. This leads to the dominant LDO sourcing the majority of the current to the load. Since the distribution of current between the two LDOs is no longer equal, this can potentially cause the dominant LDO to reach current limit, thermal shutdown, or both.

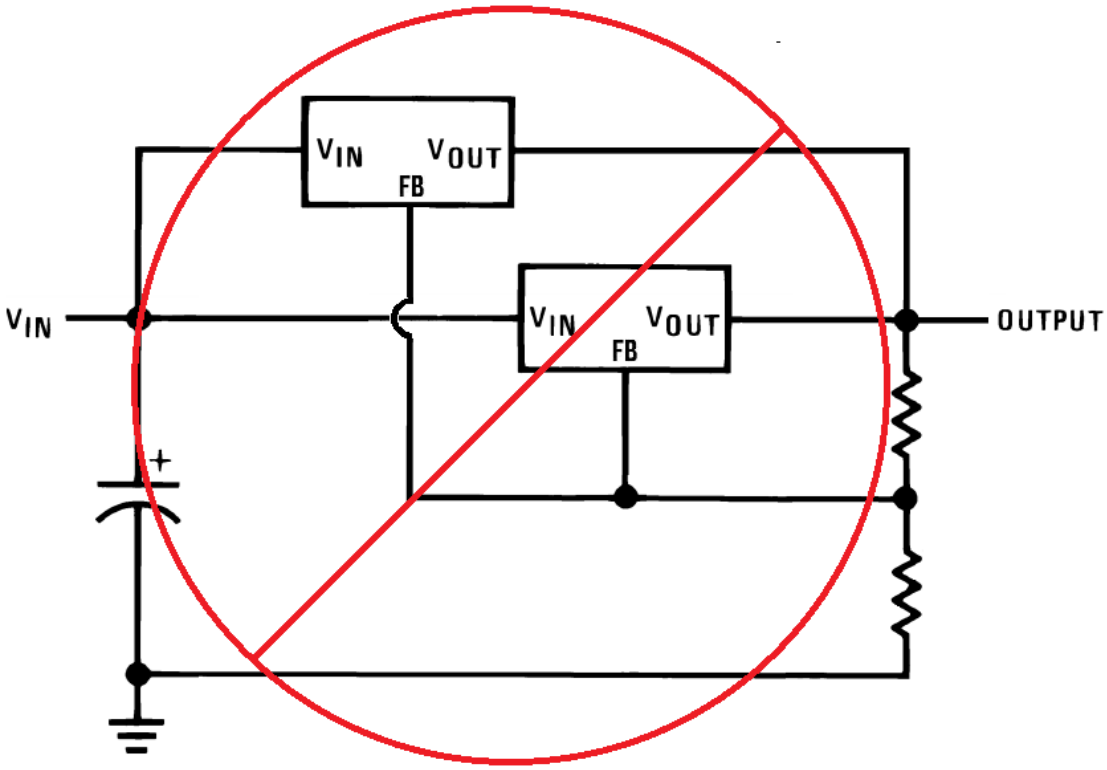


Figure 2: An Ideal Current-Sharing Supply

2.2 Control Loop

In order to account for the variations in the reference and offset voltage between each LDO, an external control loop must be added to ensure equal distribution of current between the two LDOs. This loop is created by the introduction of an op amp and sense resistors, as shown in Figure 3. The voltage drop across each of the sense resistors is proportional to the current being sourced through the particular LDO. Ideally, the voltage across these resistors should be equal. These voltages are fed into the inputs of a low offset, op amp in an open loop configuration. Depending on the voltage differential between the two sense resistors, the op amp will correspondingly drive the feedback node of the upper LDO, known as the slave LDO. It will continue to drive this node until the slave LDO outputs the same voltage as the bottom LDO, known as the master LDO. In this steady state, current distribution through the two LDOs will be nearly equal.

Notice that, unlike the ideal configuration, both LDOs each have a resistor network to set their output voltage. The reason for this is because the master LDO needs its own network as it will essentially be the point of reference for the slave LDO. As the op amp measures the differential between the negative and positive terminal, it will drive the slave accordingly. At steady state, the slave LDO's output voltage will match that of the master LDO.

A resistor between the op amp output and the feedback node is necessary to separate the voltage loop from the current loop. The size of this resistor determines the voltage range seen by the feedback node. If the resistor is too small, the voltage range will be too large and can potentially cause instability. If the resistor is too large, the voltage range will be too small to account for variations in outputs between the two LDOs. A resistor of 15kΩ was used to allow for a maximum of 4% mismatch between the output voltages of the master and slave LDOs.

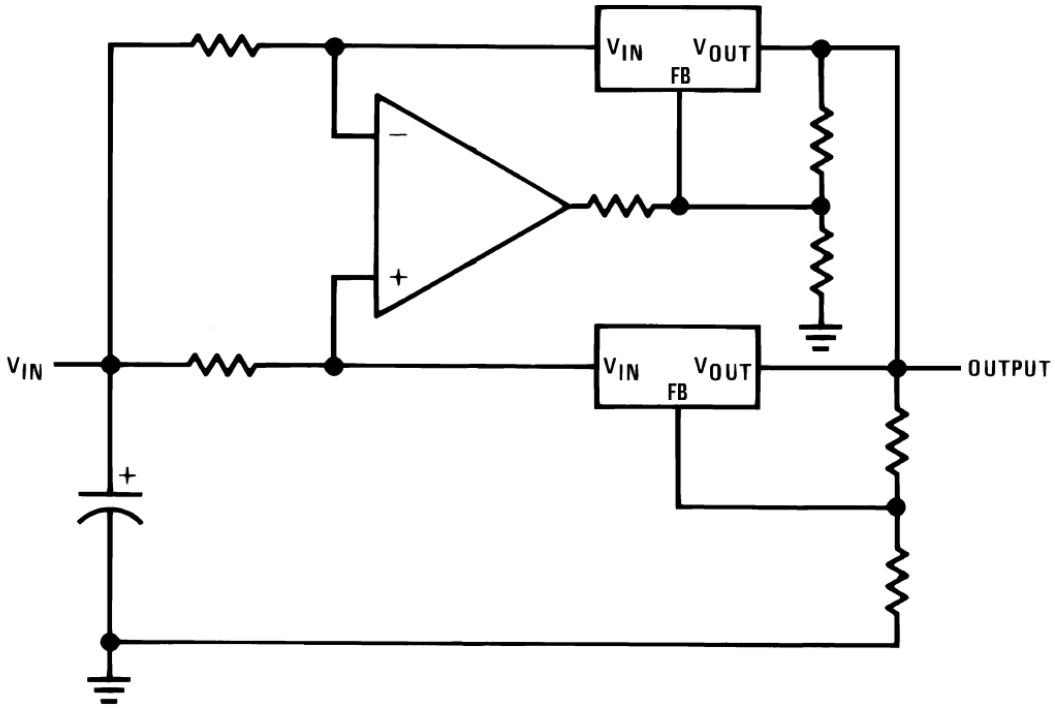


Figure 3: Basic Current-Sharing Operation

3 Component Selection

3.1 LDOs

Dropout

As this power supply is intended for supplying higher currents than are feasible with an individual LDO, thermal dissipation will inevitably become a concern. The power dissipation of an individual LDO is succinctly expressed as:

$$P_{LOSS} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Therefore, as current increases, it's important to keep the V_{IN}-V_{OUT} differential as small as possible to limit dissipation. Of course, the minimum possible differential is contingent upon the dropout properties of the LDO. An LDO with low dropout is necessary to achieve efficient operation. More information on dropout and efficiency can be found in the Technical Review of Dropout Voltage Regulator Operation and Performance application report.

This is one of the reasons why TPS74401 was chosen for this design. When operating individually, TPS74401 has a max dropout of 195mV when sourcing 3A.

Package

Despite efforts to minimize power dissipation, some heat will be generated as a byproduct of regulation. The thermal properties of the LDO must be accounted for in order to ensure the LDO will not go into thermal shutdown. Thermal metrics can be found in device datasheets. Additional information on the various metrics can be found in the IC Package Thermal Metrics application report.

The TPS74401 was selected because it is available in the RGW package, a 5x5mm QFN with a large thermal pad and superb thermal characteristics. Coupled with proper board layout, this package allows the LDO to continue to operate in spite of large power dissipation.

Output Noise/PSRR

Another benefit of using an LDO as a power supply is its ability to filter noise. The components necessary to create an equivalent low-pass filter can be bulky and expensive. When attempting to filter upstream noise, an LDO is much more compact solution than using discrete elements.

When using an LDO as a filter, the key specifications to pay attention to are PSRR and output noise. PSRR dictates the LDO's ability to attenuate input ripple across a wide frequency band. Output Noise refers to the intrinsic noise generated by the LDO by virtue of being an electronic device. Output Noise is also characterized across a wide frequency band. For more information on the subject, see the LDO Noise Demystified application report.

TPS74401 was chosen for this design because it has high PSRR (over 30dB through 700kHz) and low noise (as low as 14uV_{RMS}).

3.2 Amplifier

Single Supply

As the LDO does not require a negative rail, a single-supply op amp is preferred for this design. The positive power supply (V^+) should be connected to the input (V_{IN}) or bias (V_{BIAS}) rail. The negative power supply (V^-) should be connected to ground.

Care must also be taken to choose an op amp with an appropriate CMRR voltage range.

Low offset

In order to properly respond to small differences in voltage across the sense resistors, the input offset should be as small as possible. If the offset is not small enough, the op amp will be unable to detect subtle voltage differences across its inputs and will fail to drive the reference voltage of the slave LDO to a state of equilibrium with the master LDO. This will result in unequal sharing of current between the two regulators.

3.3 External Resistor Network

Since this design is intended to share current between two adjustable LDOs, the output voltage must be set via an external resistor divider. The master LDO and the slave LDO should each have their own resistor network. These two networks should be nominally identical. The desired output voltage should be set according to the formula specified in the datasheet of the given LDO being used.

In the case of TPS74401:

$V_{OUT} = 0.8 \times (1 + \frac{R_1}{R_2})$, where R_2 is the resistor from FB to GND.

The variance of the voltage reference and the tolerance of the resistors can contribute to an output voltage that is slightly off from the nominal value. To minimize this inaccuracy, an LDO with a small voltage reference variance and resistors with small tolerances should be chosen. More information on this topic is available in the AN-1378 Method for Calculating Output Voltage Tolerances in Adjustable Regulators application report.

In this design, TPS74401 is a 1% accurate LDO over line, load, and temperature. The resistor network features 1% tolerance resistors.

Note that although the two resistor dividers will not have the same exact resistor values, the supply will still operate properly.

3.4 Sense Resistors

The sense resistors are the means by which the op amp measures how evenly current is being distributed between master and slave LDOs.

These resistors should have a nominal value of 30mΩ or less to avoid unnecessary dissipation. Since large amounts of current will pass through these resistors, a corresponding drop in voltage will occur before the input, V_{IN}, of the LDOs. If the voltage drop is too large, it can cause one or both of the LDOs to go into premature dropout.

These resistors should also have a tolerance of 1% or better. Since the voltage drops across the resistors are the inputs to the op amp, it is imperative that these resistor values be as close as possible. After all, the output of the op amp will only be driven so far as there is there is a difference between the inputs.

See the following example:

- The slave sense resistor has a value of 29mΩ
- The master sense resistor has a value of 31mΩ
- Although 3A is being sourced through each LDO, the op amp does not see it that way. Instead, it sees a voltage of 0.087V across the slave sense resistor and 0.093V across the master sense resistor. It will then drive the output until the two sense voltages reach equilibrium.
- In ‘equilibrium’, the slave LDO will source 3.1A and the master LDO will only source 2.9A. This results in 96.6% sharing, which is less than ideal.

The last consideration when choosing sense resistors is the power rating. In this design, the resistors are rated at 1W to withstand a maximum dissipation of 0.27W.

3.5 Input Capacitor

It is generally considered best practice to use an input capacitor with an LDO. Although not always required for stability, an input capacitor counteracts reactive input sources, improves transient response and aids ripple rejection. As a result, an input capacitor can often be forgone in proper circumstances.

However, this design *does* require the use of an input capacitor. This is because of the large amount of current being sourced.

Whenever the LDO is abruptly loaded, large amounts of inrush current can temporarily drop the input voltage to the current-sharing supply due to both the large impedance on the line and the load transient of upstream power supplies. This input voltage drop can subsequently send one or both LDOs into dropout as they attempt to respond to the transient. As a result, the output voltage will ring for an extended period before stabilizing.

In order to avoid this oscillatory ringing, an input capacitor must be added. Since this particular design can have an inrush current of 6A, the input capacitance must be greater than is required for an individual LDO. A 330µF input capacitor is recommended for this design to stabilize the input voltage and avoid having the LDOs going into dropout unnecessarily.

4 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

4.1 PCB Layout

PCB design must account for thermal dissipation and large current draw. Therefore, the following steps should be taken:

- Allow large traces to be used for input and output paths (>120mil in width).
- Try to keep the two input and output traces for slave and master the same length to allow for higher accuracy.
- Have a large ground plane directly below the top layer.
- Use multiple vias to connect the ground planes together.

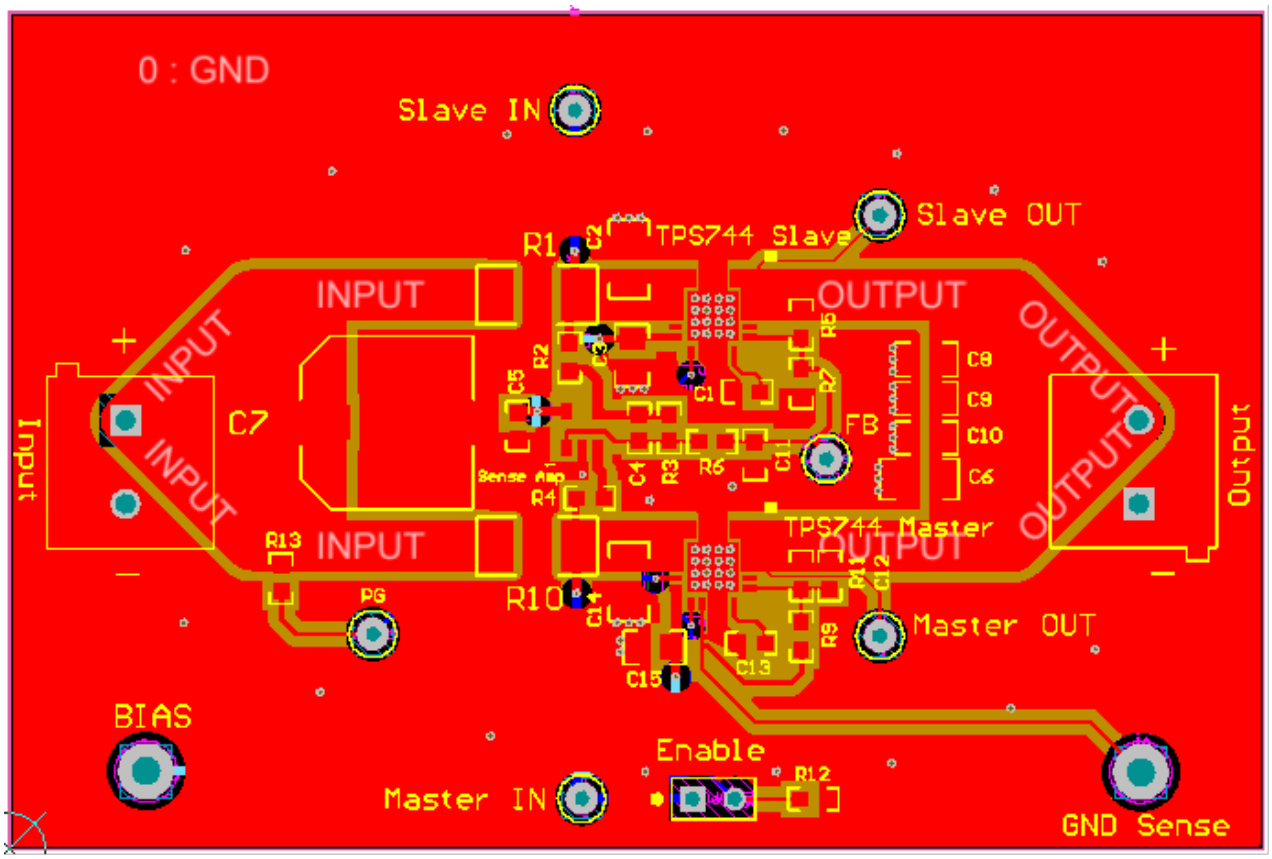


Figure 4: Top View of the PCB Layout

5 Simulation

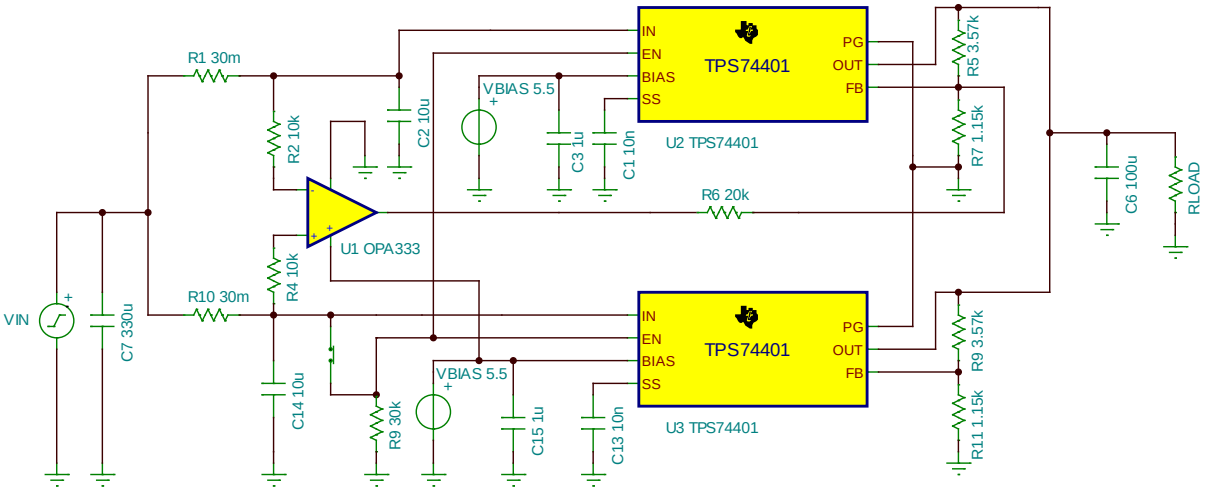


Figure 5: TINA-TI™ Simulation Circuit

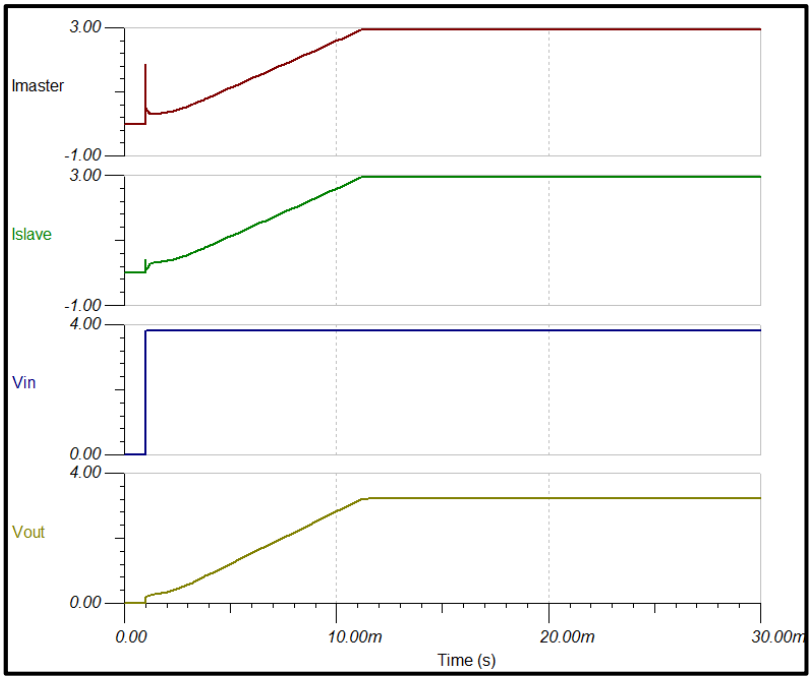


Figure 6: Simulated Startup

6 Verification & Measured Performance

6.1 Current Sharing Error

Figure 7 depicts the current sharing error, excluding the error arising from the sense resistors. This is because it does not take into account the tolerance of the resistors. To find the worst-case, overall error, add the tolerance of the resistors to the error found below.

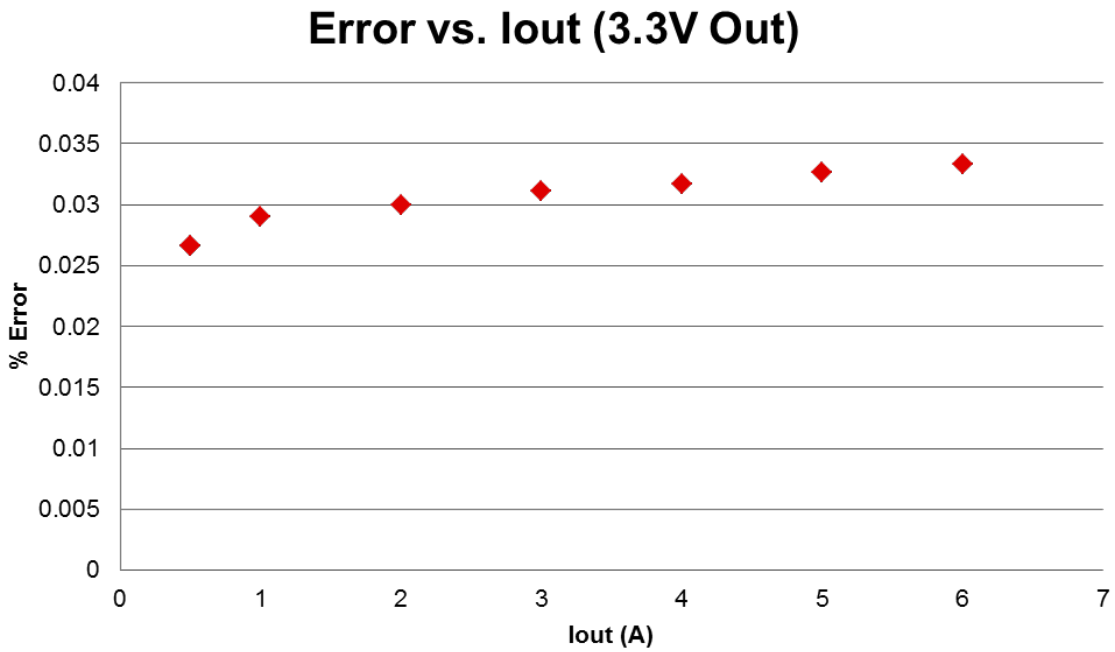


Figure 7: Current Sharing Error vs. I_{OUT}

6.2 Startup

Like individual LDOs, the startup of the Current-Sharing Dual LDO power supply can be modified with the introduction of a soft-start capacitor. A programmable soft-start is advantageous for powering many processors and FPGAs that need a specifically-timed, monotonic startup.

The maximum recommended soft-start capacitor value for the TPS74401 is 0.015µF.

Note that the soft-start capacitor also serves as a noise-reduction capacitor as discussed in section 6.7.

Output = 0.8V
Input = 0V to 5V
Bias = Vin
I_{LOAD} = 6A
C_{SS} = 10nF
C_{IN} = 330µF and10µF
C_{OUT} = 100µF
C_{BIAS} = 1µF

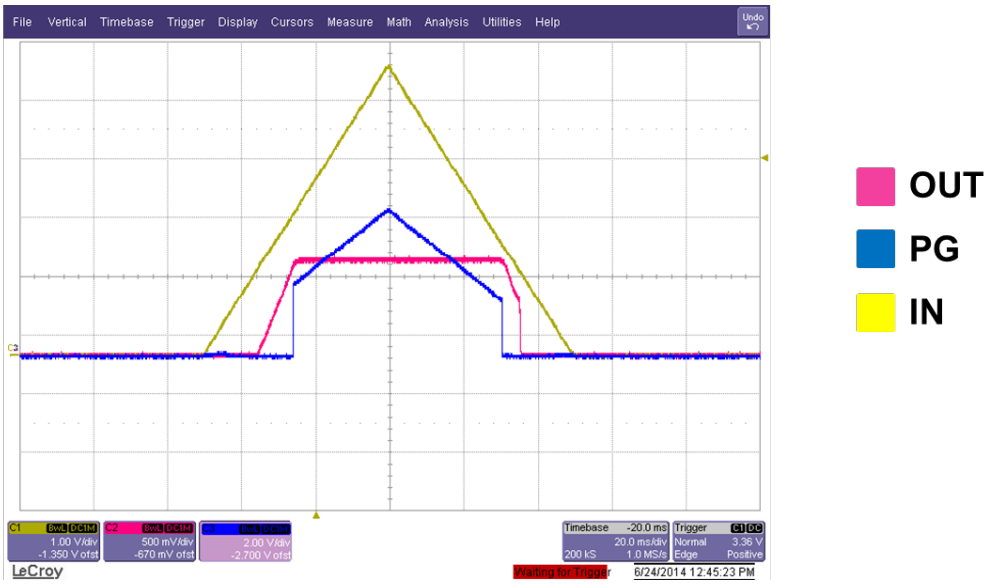


Figure 8: Power-Up/Power-Down (V_{OUT}: 0.8V)

Output = 3.3V
Input = 0V to 5V
Bias = Vin
I_{LOAD} = 6A
C_{SS} = 10nF
C_{IN} = 330µF and10µF
C_{OUT} = 100µF
C_{BIAS} = 1µF

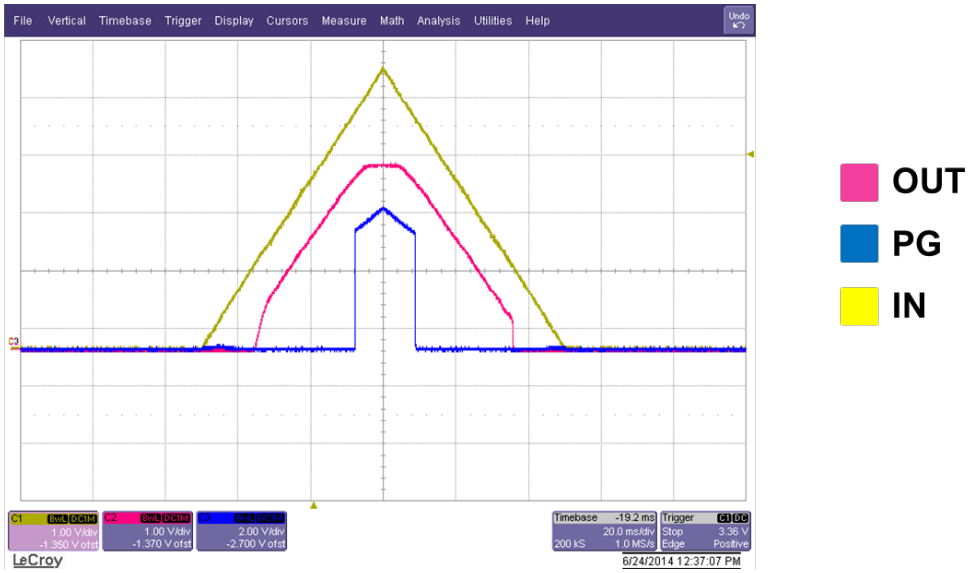


Figure 9: Power-Up/Power-Down (V_{OUT}: 3.3V)

6.3 Load Transient Response

The load transient response is largely determined by the load transient, the input capacitor, and the output capacitor. A large input capacitor (330µF) prevents the output from going into dropout. A large output capacitor (100µF) helps reduce undershoot and overshoot on the output rail.

Output = 0.8V
Input = 1.3V
Bias = 5.0V
I_{LOAD} = 100mA to 6A
C_{SS} = 10nF
C_{IN} = 330µF and10µF
C_{OUT} = 100µF
C_{BIAS} = 1µF

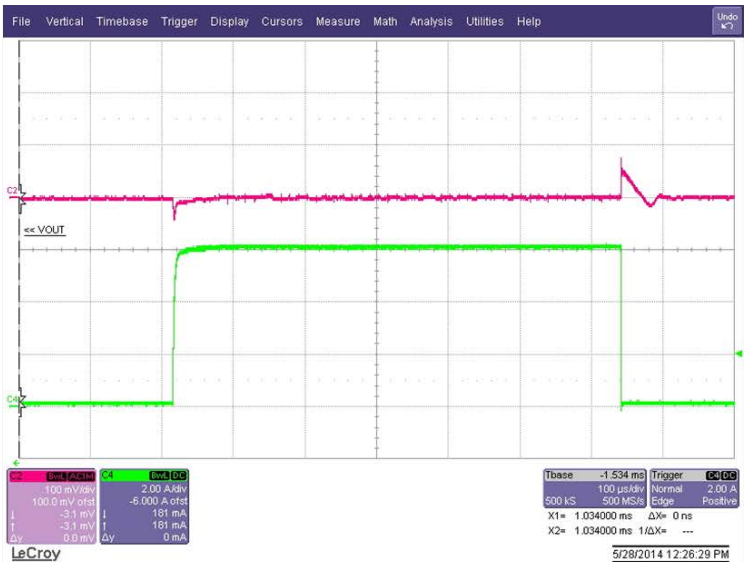


Figure 10: Load Transient Response (V_{OUT}: 0.8V)

Output = 3.3V
Input = 3.8V
Bias = 5.0V
I_{LOAD} = 100mA to 6A
C_{SS} = 10nF
C_{IN} = 330µF and10µF
C_{OUT} = 100µF
C_{BIAS} = 1µF

Figure 11: Load Transient Response (V_{OUT}: 3.3V)

6.4 Short Circuit Recovery

Output = 0.8V
Input = 1.3V
Bias = 5.0V
I_{LOAD} = Shorted
C_{SS} = 10nF
C_{IN} = 330µF and10µF
C_{OUT} = 100µF
C_{BIAS} = 1µF

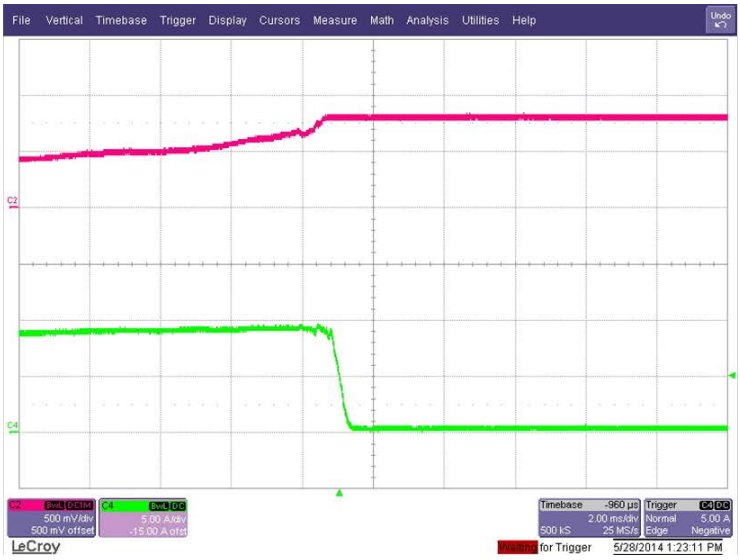


Figure 12: Output Short-Circuit Recovery (V_{OUT}: 0.8V)

Output = 3.3V
Input = 3.8V
Bias = 5.0V
I_{LOAD} = Shorted
C_{SS} = 10nF
C_{IN} = 330µF and10µF
C_{OUT} = 100µF
C_{BIAS} = 1µF

Figure 13: Output Short-Circuit Recovery (V_{OUT}: 3.3V)

6.5 Dropout

The following figures depict the typical overall dropout of the Current-Sharing Dual LDO supply. In this design, the overall dropout is composed of two parts: the dropout of the individual LDOs and the voltage drop across the sense resistors. These measurements were taken at 25C.

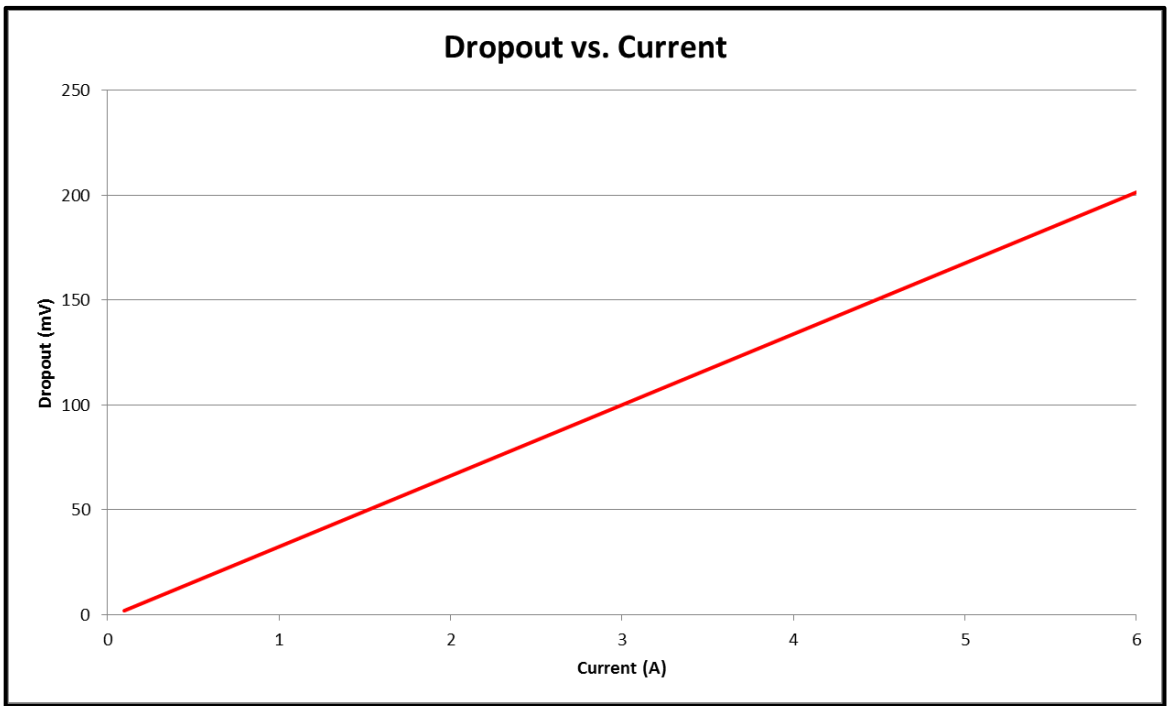


Figure 14: V_{IN} Dropout Voltage vs I_{OUT}

6.6 PSRR

Power Supply Rejection Ratio is important for attenuating ripple generated upstream of the Current-Sharing Dual LDO power supply. This ripple, if left alone, has the potential to cause a loss in fidelity for noise-sensitive applications. An LDO with high PSRR over a wide frequency band is necessary to filter switching noise occurring at high frequencies.

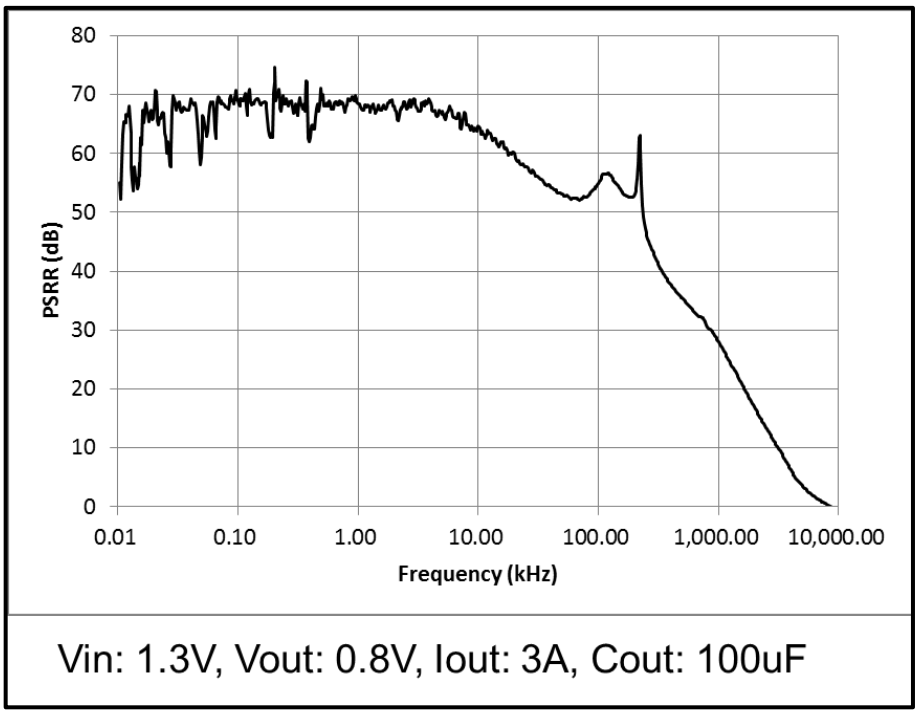


Figure 15: V_{IN} PSRR vs Frequency (V_{OUT}: 0.8V, I_{OUT}: 3A)

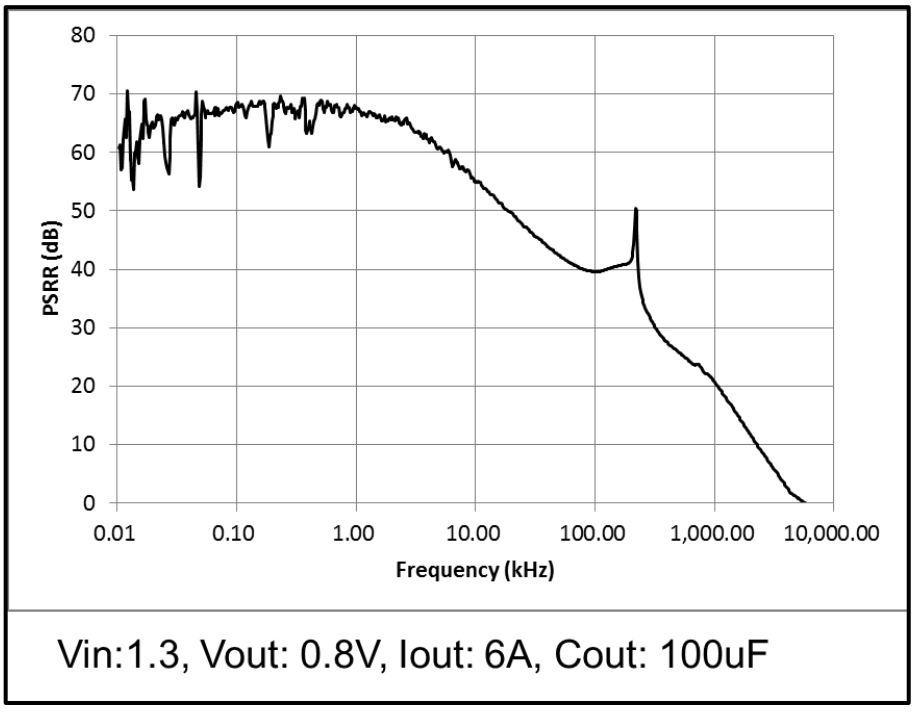


Figure 16: V_{IN} PSRR vs Frequency (V_{OUT}: 0.8V, I_{OUT}: 6A)

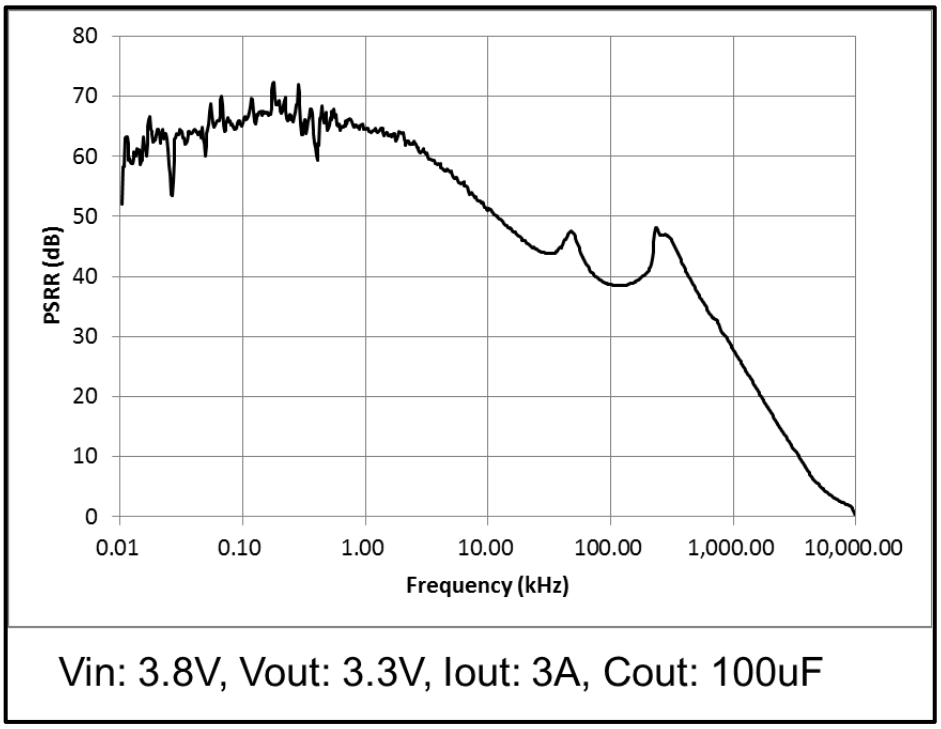


Figure 17: V_{IN} PSRR vs Frequency (V_{OUT}: 3.3V, I_{OUT}: 3A)

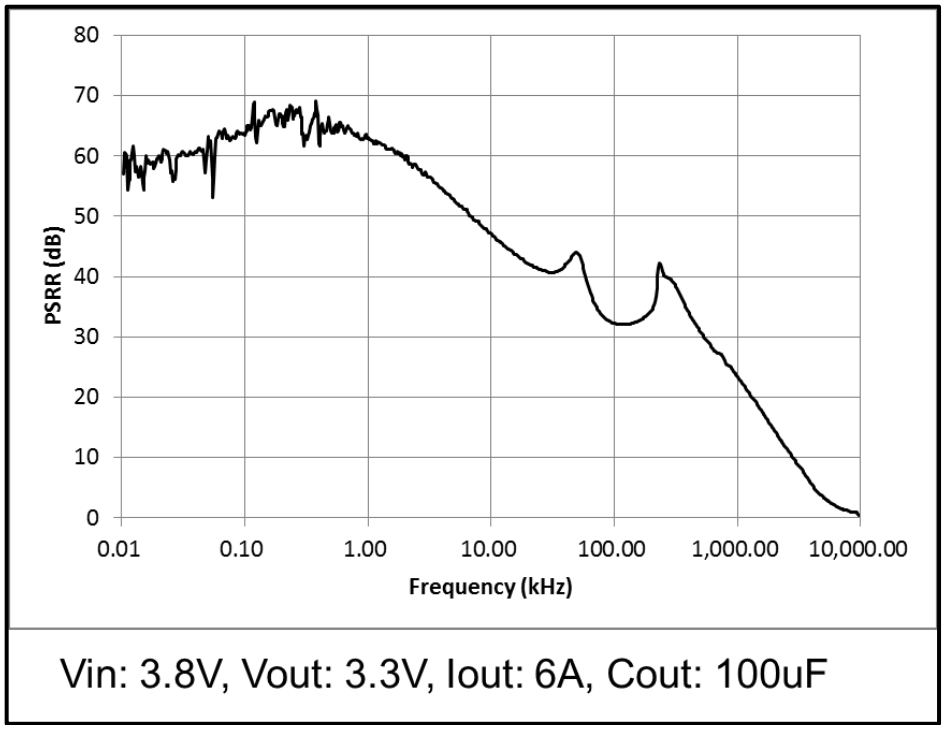


Figure 18: V_{IN} PSRR vs Frequency (V_{OUT}: 3.3V, I_{OUT}: 6A)

6.7 Noise

Along with PSRR, Output Noise is also an important characteristic to consider. Output noise will be generated by the LDOs themselves by virtue of their being electronic devices. Output noise should be as low as possible across a wide frequency band to ensure a clean rail.

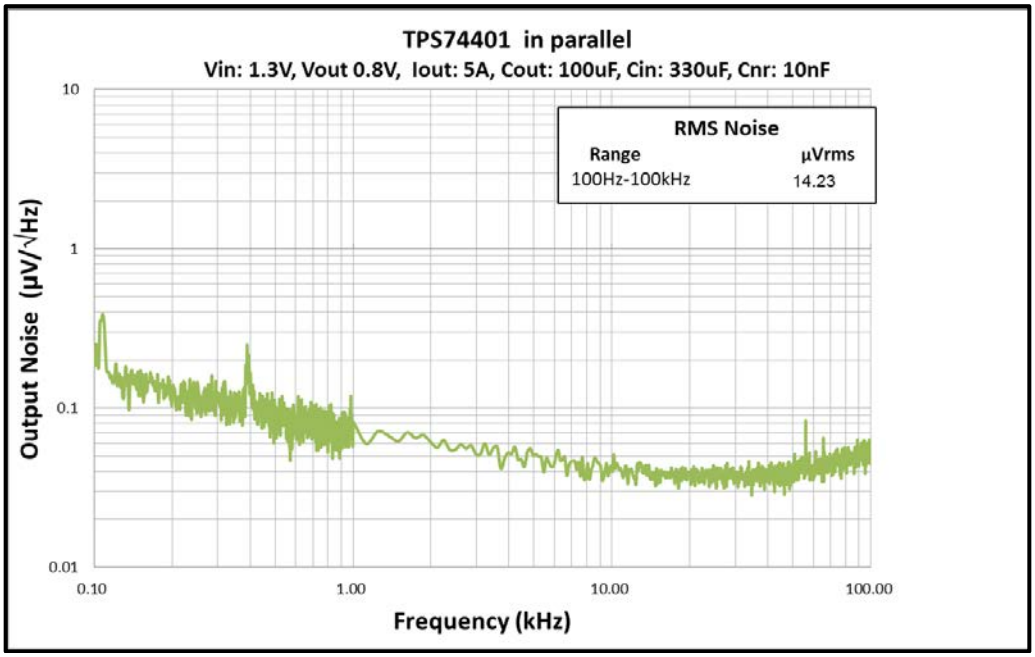


Figure 19: Noise Spectral Density (V_{OUT}: 0.8V)

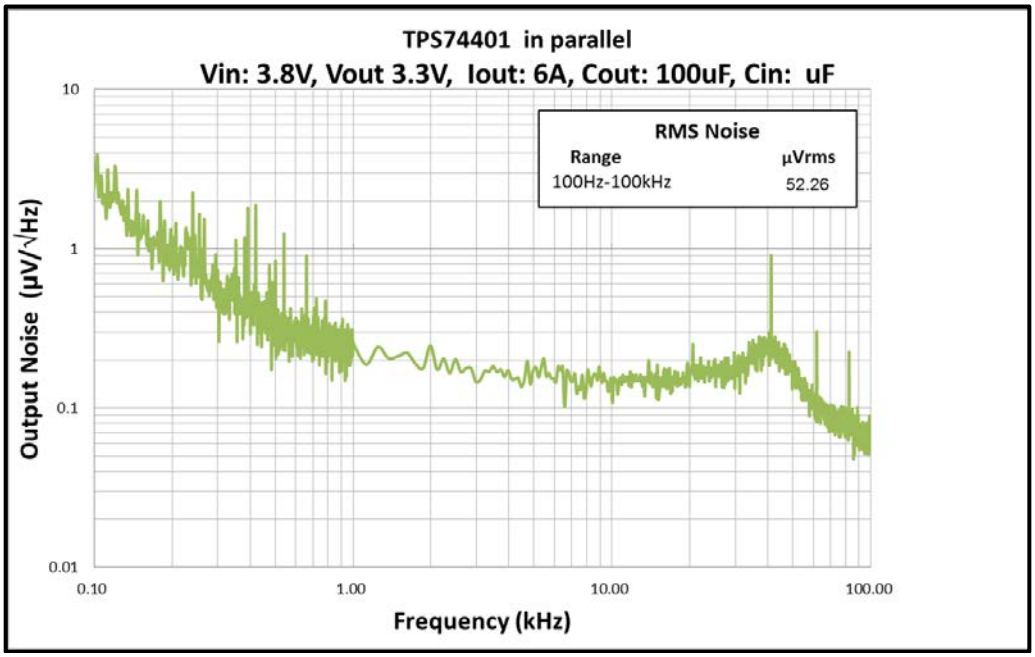


Figure 20: Noise Spectral Density (V_{OUT}: 3.3V)

6.8 Thermal Image

Figure 21 displays the thermal distribution of the Current-Sharing Dual LDOs board at full load. The placement of the LDOs prevents them from heating each other inadvertently. Additionally, the large ground plane serves to spread the heat across the entire board.

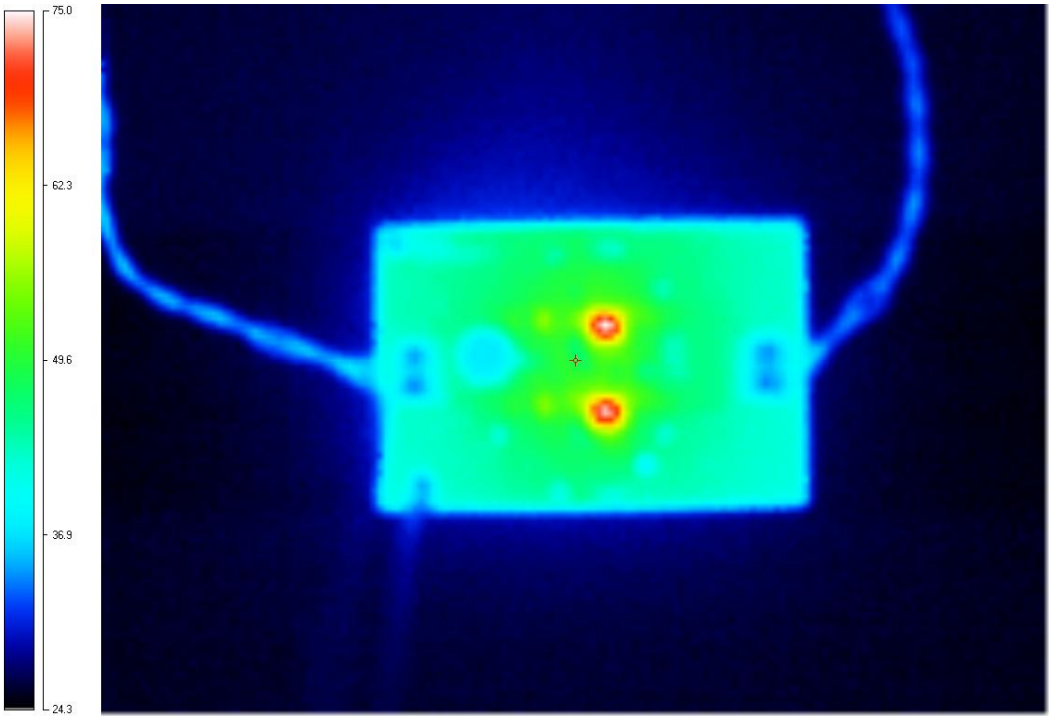


Figure 21: Thermal Image of the Current Sharing Supply sourcing 6A

7 About the Author

Mike Hartshorne is an applications engineer in the Linear Power business unit. He has worked as an applications engineer in various power product lines, and previously in ADC product lines. Mike received a BSEE from the University of San Diego and an M. Eng. from the University of Arizona.

Sean Grotle is a test engineer in the Linear Power business unit. He received his BSEE from the University of Arizona in 2012. He joined TI in 2013.

Aaron Paxton is a product marketing engineer in the Linear Power business unit. He received a BAEE/BSEE from the University of San Diego in 2012. He joined TI in 2012.

8 Acknowledgements & References

1. *Technical Review of Low Dropout Voltage Regulator Operation and Performance (SLVA072)*
2. *Semiconductor and IC Package Thermal Metrics (SPRA953B)*
3. *LDO Noise Demystified (SLAA412)*
4. *AN-1378 Method for Calculating Output Voltage Tolerances in Adjustable Regulators (SNVA112A)*

Appendix A.

A.1 Electrical Schematic

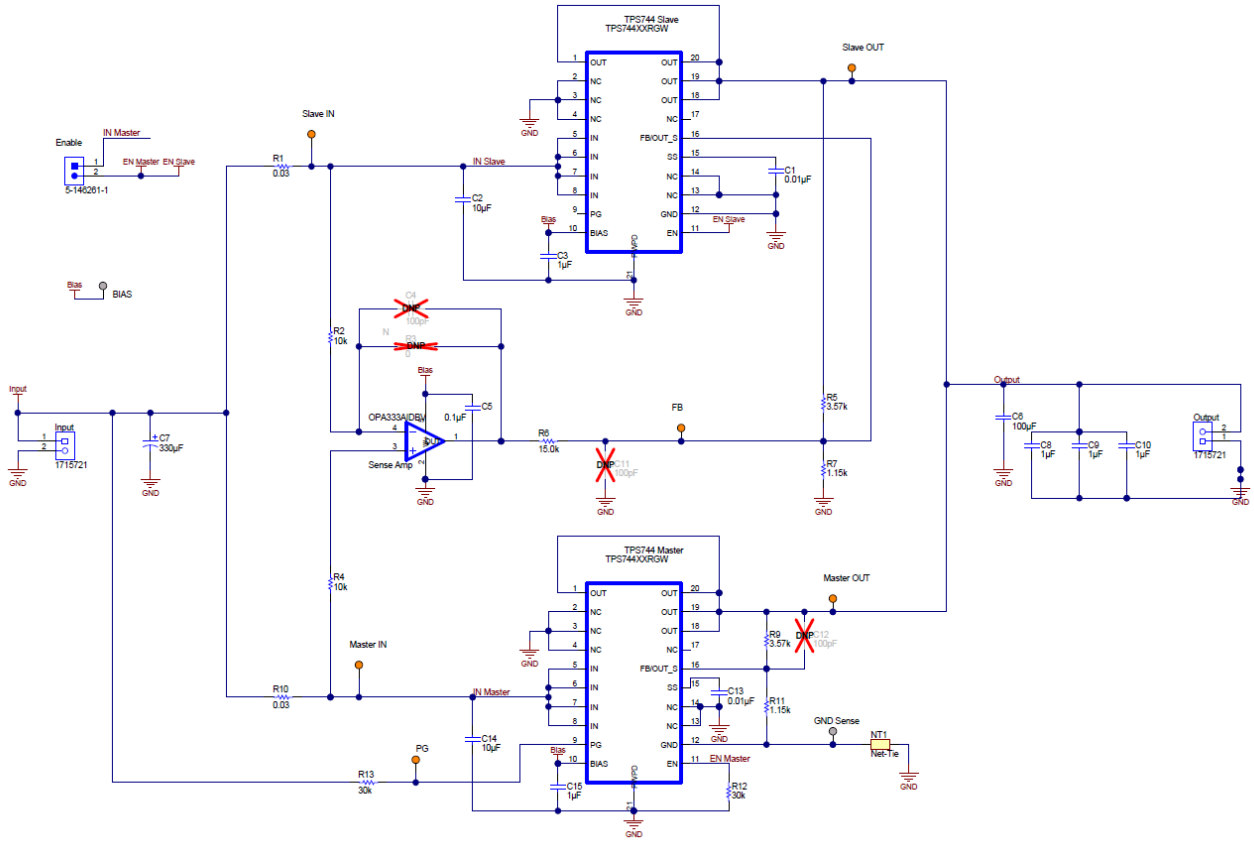


Figure A-1: Electrical Schematic

A.2 Bill of Materials

Bill of Materials

TI DESIGNS

TEXAS INSTRUMENTS

Quantity	Designator	Value	Description	Manufacturer	Manufacturer Part Numbe	Supplier Part Number 1
2	BIAS, GND Sense	Single	Terminal, Turret, TH, Hollow, Single	Keystone	1562-2	1562-2K-ND
2	C1, C13	0.01uF	CAP, CERM, 0.01uF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E103KA01D	490-1520-1-ND
2	C2, C14	10uF	CAP, CERM, 10uF, 10V, +/-20%, X5R, 1206	TDK	C3216X5R1A106M160AB	445-1387-1-ND
5	C3, C8, C9, C10, C15	1uF	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0805	MuRata	GRM21BR71C105KA01L	490-1691-1-ND
1	C5	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X5R, 0603	MuRata	GRM188R61C104KA01D	GRM188R61C104KA01D-ND
1	C6	100uF	CAP, CERM, 100uF, 6.3V, +/-20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	490-4539-1-ND
1	C7	330uF	CAP, AL, 330uF, 10V, +/-20%, 0.024 ohm, SMD	Nippon Chemi-Con	APXA100ARA331MJ80G	565-3071-1-ND
6	FB, Master IN, Master OUT, PG, Slave IN, Slave OUT	Orange	Test Point, Miniature, Orange, TH	Keystone	5003	5003K-ND
2	Input, Output	2x1	Conn Term Block, 2POS, 5.08mm, TH	Phoenix Contact	1715721	277-1263-ND
2	R1, R10	0.03	RES, 0.03 ohm, 1%, 0.75W, 2010	Ohmite	LVK20R030FER	588-LVK20R030FER
2	R2, R4	10k	RES, 10k ohm, 5%, 0.1W, 0603	Yageo America	RC0603JR-0710KL	311-10KGRCT-ND
2	R5, R9	3.57k	RES, 3.57k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-073K57L	311-3.57KHRCT-ND
1	R6	15.0k	RES, 15.0k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0715KL	311-15.0KHRCT-ND
2	R7, R11	1.15k	RES, 1.15k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031K15FKEA	541-1.15KHCT-ND
2	R12, R13	30k	RES, 30k ohm, 5%, 0.1W, 0603	Yageo America	RC0603JR-0730KL	311-30KGRCT-ND
1	Sense Amp	OPA333AIDBV	IC, 1.8V, microPower, CMOS Op Amp, Zerø-Drift Series	TI	OPA333AIDBV	
2	TPS744 Master, TPS744 Slave	TPS74401RGW	IC, 3A LDO With Programmable Soft-Start	TI	TPS74401RGW	

Figure A-2: Bill of Materials