SPECIFICATIONS No. 10TLM078	Issue: Oct. 28, 2010

Specifications for

TFT-LCD Monitor (TENTATIVE)

Version 0.1

MODEL COM20T2M57XSB

Customer's Approval
Signature:
Name:
Section:
Title:
Date:

ORTUSTECH

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Version History

Ver.	Date	Page	Description	
0.0	Sep. 8, 2010	-	-	Tentative issue
0.1	Oct. 28,2010	P.11		7. Recommended Operating Conditions
			Change	VDDIO TYP: 3.3V → (1.8)V
	△A ×4	P.12		8.1.1 Display Module
			Change	VDD=VDDIO=3.3V → VDD=3.3V,VDDIO=1.8V
		P.13		8.2.1 RGB Interface Block
			Change	VDD=VDDIO=3.3V → VDD=3.3V,VDDIO=1.8V
		P.14		8.2.2 Serial Communication Block
			Change	VDD=VDDIO=3.3V → VDD=3.3V,VDDIO=1.8V

Contents

1. Application

This Specification is applicable to 5.12cm (2.0 inch) TFT-LCD monitor for non-military use.

◎ ORTUS TECHNOLOGY makes no warranty or assume no liability that use of this Product and/or any information including drawings in this Specification by Purchaser is not infringing any patent or other intellectual property rights owned by third parties, and ORTUS TECHNOLOGY shall not grant to Purchaser any right to use any patent or other intellectual property rights owned by third parties. Since this Specification contains ORTUS TECHNOLOGY's confidential information and copy right, Purchaser shall use them with high degree of care to prevent any unauthorized use, disclosure, duplication, publication or dissemination of ORTUS TECHNOLOGY'S confidential information and copy right.

◎ If Purchaser intends to use this Products for an application which requires higher level of reliability and/or safety in functionality and/or accuracy such as transport equipment (aircraft, train, automobile, etc.), disaster-prevention/security equipment or various safety equipment, Purchaser shall consult ORTUS TECHNOLOGY on such use in advance.

◎ This Product shall not be used for application which requires extremely higher level of reliability and/or safety such as aerospace equipment, telecommunication equipment for trunk lines, control equipment for nuclear facilities or life-support medical equipment.

◎ ORTUS TECHNOLOGY assumes no liability for any damage resulting from misuse, abuse, and/or miss-operation of the Product deviating from the operating conditions and precautions described in the Specification.

◎ If any issue arises as to information provided in this Specification or any other information, ORTUS TECHNOLOGY and Purchaser shall discuss them in good faith and seek solution.

◎ ORTUS TECHNOLOGY assumes no liability for defects such as electrostatic discharge failure occurred during peeling off the protective film or Purchaser's assembly process.

◎ This Product is compatible for RoHS directive.

Object substance	Maximum content [ppm]
Cadmium and its compound	100
Hexavalent Chromium Compound	1000
Lead & Lead compound	1000
Mercury & Mercury compound	1000
Polybrominated biphenyl series（PBB series）	1000
Polybrominated biphenyl ether series（PBDE series）	1000

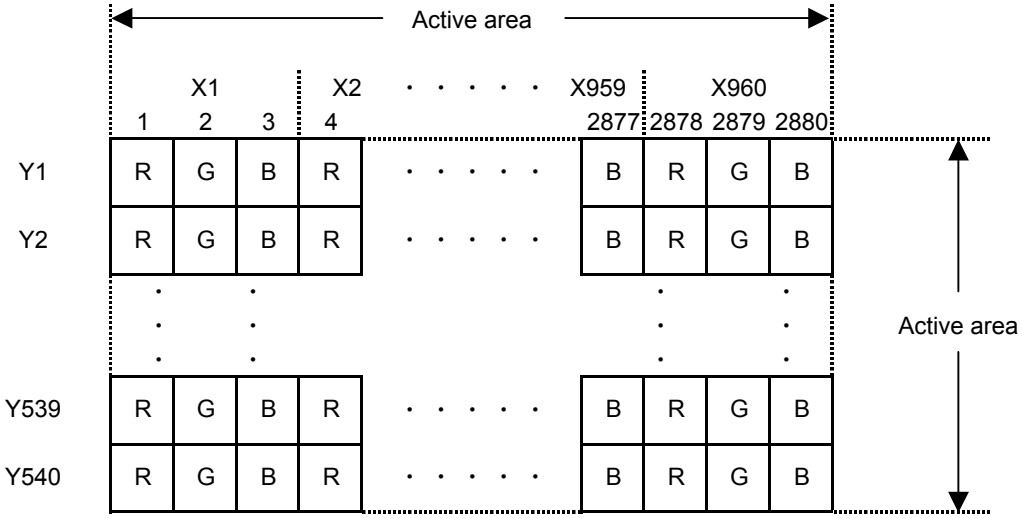
2. Outline Specifications

2.1 Features of the Product

- 2.0 inch diagonal display, 2,880 [H] x 540 [V] dots.
- RGB 8-bit 16,777,216 colors display capability.
- Built in Timing generator (TG), Built-in power supply circuit, Counter-electrode driving circuit.
- Long life & high brightness LED back-light

2.2 Display Method

Items	Specifications	Remarks
Display type	TN type 16,777,216 colors. Transmissive type, Normally white	
Driving method	a-Si TFT Active matrix Line-scanning, Non-interlace	
Dot arrangement	RGB stripe arrangement	Refer to "Dot arrangement"
Signal input method	8-bit RGB, parallel input.	
Backlight type	Long life & High bright white LED.	



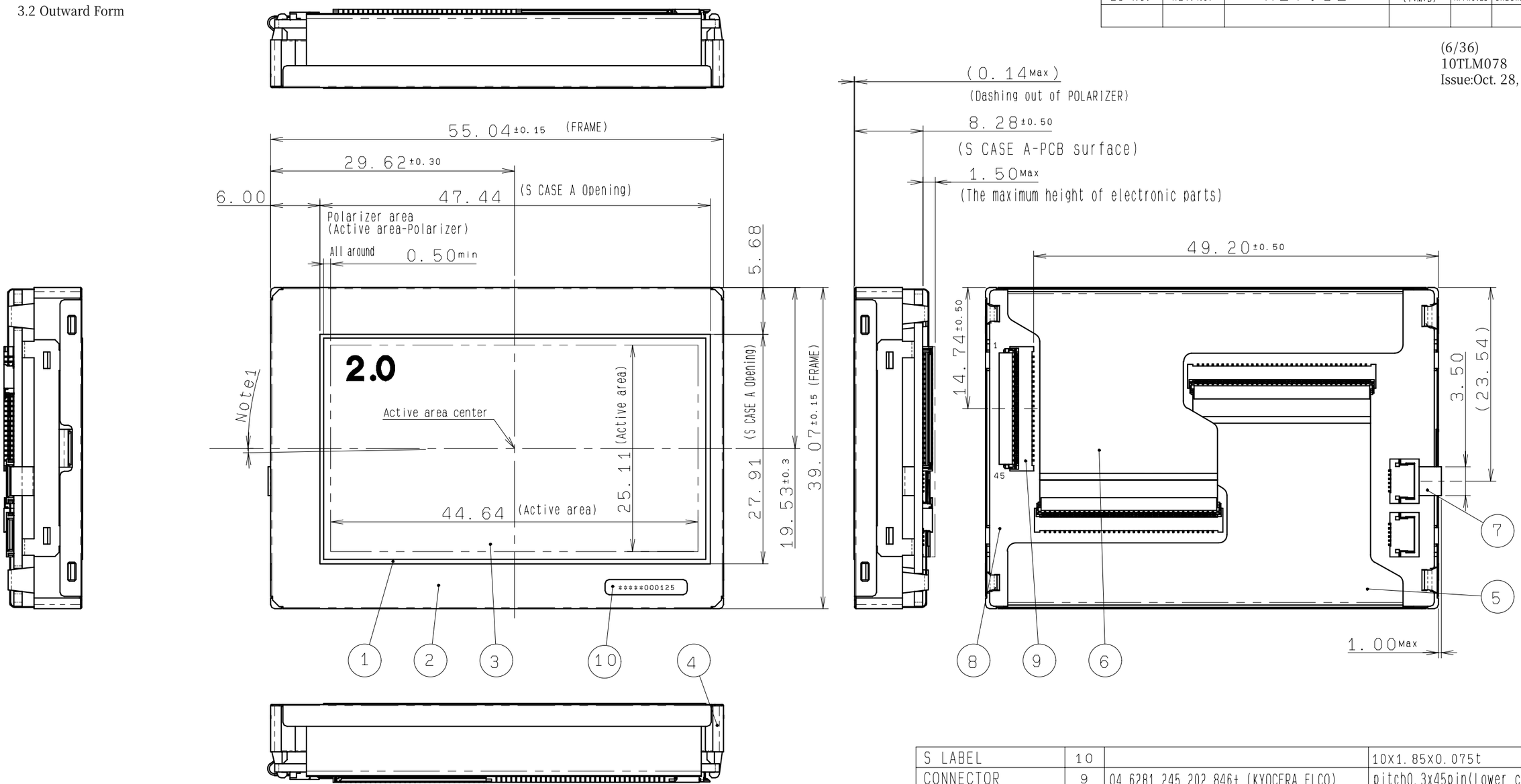
Dot arrangement
(When "S LABEL" on the front case is placed at the lower right)

3. Dimensions and Shape

3.1 Dimensions

Items	Specifications	Unit	Remarks
Outline dimensions	(55.04)[H] × (39.07)[V] × (9.78)[D]	mm	
Active area	44.64[H] × 25.11[V]	mm	5.12cm diagonal
Number of dots	2,880[H] × 540[V]	dot	
Dot pitch	15.5[H] × 46.5[V]	μm	
Surface hardness of the polarizer	3	H	Load:(2.0)N
Weight	(TBD)	g	

EC NO.	REV. No.	REVISE	DATE (Y:M:D)	APPROVED	CHECKED	PREPARED



S LABEL	10		10x1.85x0.075t
CONNECTOR	9	04 6281 245 202 846+ (KYOCERA ELCO)	pitch0.3x45pin(Lower contact)
PCB	8		1.0t
LED-FPC	7		
FPC B	6		
FPC A	5		
Frame	4		
Polarizer	3		with protection sheet
S CASE A	2	SUS (t=0.15)	
TFT-LCD	1	Glass substrate thickness=0.5t	
PART NAME	ITEM	MATERIAL GRADE	REMARK

Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than [±40°].

Note 2. S LABEL is affixed the area shown in the drawing.
The thickness of the S label will be added to that of S CASE's surface.

Note 3. Protective film is affixed on front surface of the screen.
Location tolerance of the protective film shall be ±1.5 mm to the polarizing film.

Note 4. Refer to "11. CRITERIA OF JUDGMENT" about the appearance specification of a polarizer.

APPROVED 橋爪	GENERAL TOLERANCE ±0.3	SCALE 2/1	UNIT mm
CHECKED 平信	ISSUE (Y:M:D) 10:07:29	MODEL COM20T2M57X**	
CHECKED	NAME		
DESIGN 大橋貴文	OUTLINE-D2M57		
DRAW 大橋貴文			

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RJD520657D301			

PART

3.3 SERIAL LABEL (S-LABEL)

1) Display Items

S-label indicates the least significant digit of manufacture year (1digit), manufacture month with below alphabet (1letter), model code (5characters), serial number (6digits).

* Contents of Display

*	*	*****	******
a	b	c	d

	Contents of display			
a	The least significant digit of manufacture year			
b	Manufacture month	Jan-A	May-E	Sep-I
		Feb-B	Jun-F	Oct-J
		Mar-C	Jul-G	Nov-K
		Apr-D	Aug-H	Dec-L
c	Model code	20FTB (Made in Japan)		
		20FVB (Made in Malaysia)		
		20FWB (Made in China)		
d	Serial number			

* Example of indication of Serial label (S-label)

・Made in Japan

0L20FTB000125

means "manufactured in December 2010, 2.0" FT type, B specifications, serial number 000125"

・Made in Malaysia

0L20FVB000125

means "manufactured in December 2010, 2.0" FV type, B specifications, serial number 000125"

・Made in China

0L20FWB000125

means "manufactured in December 2010, 2.0" FW type, B specifications, serial number 000125"

2) Location of Serial Label (S-label)

Refer to 3.2 "Outward Form".

4. Pin Assignment

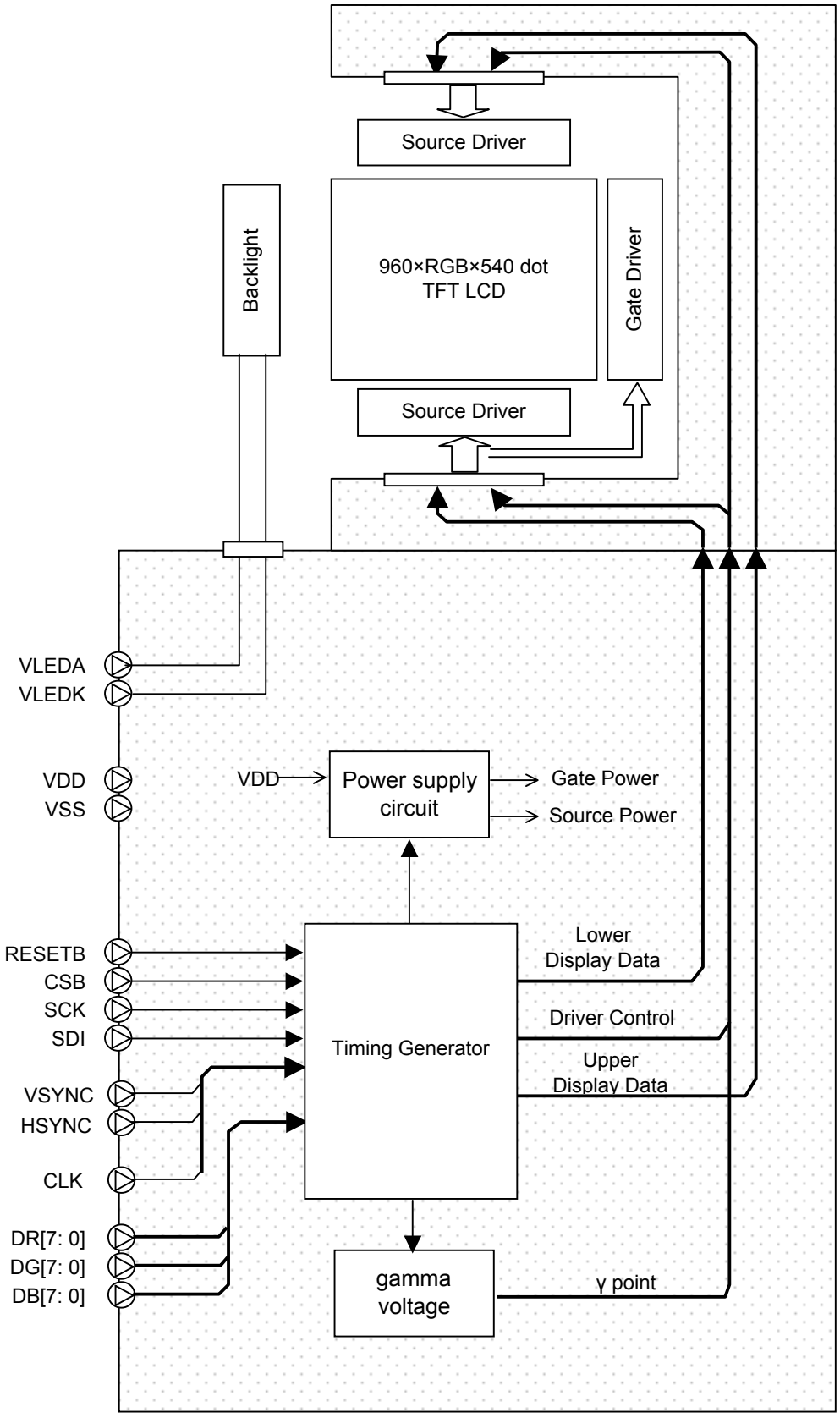
No.	Symbol	Function	Signal voltage
1	VLEDA	Backlight power supply input.(anode side)	
2	VLEDA	Backlight power supply input.(anode side)	
3	VLEDK	Backlight power supply input.(cathode side)	
4	VLEDK	Backlight power supply input.(cathode side)	
5	VSS	GND.	
6	DR7	Display data(R).	VDDIO
7	DR6	00h: Black	
8	DR5	DR0:LSB DR7:MSB	
9	DR4		
10	DR3		
11	DR2		
12	DR1		
13	DR0		
14	VSS	GND.	
15	DG7	Display data(G).	VDDIO
16	DG6	00h: Black	
17	DG5	DG0:LSB DG7:MSB	
18	DG4		
19	DG3		
20	DG2		
21	DG1		
22	DG0		
23	VSS	GND.	
24	DB7	Display data(B).	VDDIO
25	DB6	00h: Black	
26	DB5	DB0:LSB DB7:MSB	
27	DB4		
28	DB3		
29	DB2		
30	DB1		
31	DB0		
32	VSS	GND.	
33	CLK	Clock signal.	VDDIO
34	VSS	GND.	
35	HSYNC	Horizontal sync signal	VDDIO
36	VSYNC	Vertical sync signal.	VDDIO
37	RESETB	Reset signal.(Low : reset、Hi : normal)	VDD
38	SCK	Clock input for serial communication. Latching data at the rising edge.	VDD
39	SDI	Data input for serial communication.	VDD
40	CSB	Chip select input for serial communication.. (Low active)	VDD
41	VSS	GND.	
42	VDDIO	Power supply for IO input.	VDDIO
43	VDD	Power supply input.	VDD
44	VDD	Power supply input.	VDD
45	VDD	Power supply input.	VDD

- Used connector: KYOCERA ELCO CO., LTD. 6281 series [04 6281 2452 02 846+]
- Please refer to the section "3.2 Outward Form" for pin terminal order.
- The corrosion phenomenon by the different kind metal uniting is generated according to the system requirements, and there is a possibility of becoming a loose connection.
  Please select very carefully, and design the FPC cable used.

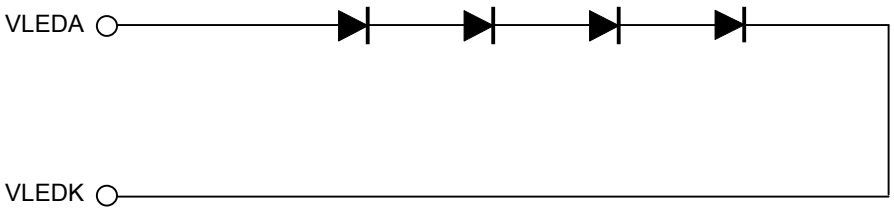
5. Circuit

5.1 Block Diagram

Each arrow shows signal flow.



5.2 LED Circuit



6. Absolute Maximum Rating

VSS=0V

Item	Symbol	Condition	Rating		Unit	Applicable terminal
			MIN	MAX		
Supply voltage 1	VDD		-0.3	3.7	V	VDD
Supply voltage 2	VDDIO		-0.3	3.7	V	VDDIO
Input voltage for logic 1	VI1		-0.3	VDD+0.3	V	RESETB,CSB,SCK, SDI
Input voltage for logic 2	VI2		-0.3	VDDIO+0.3	V	VSYNC,HSYNC,CLK DR[7:0],DG[7:0],DB[7:0]
LED forward current	IL		―	TBD	mA	VLEDA-VLEDK
Storage temperature range	Tstg		-30	80	˚C	

A

7. Recommended Operating Conditions

VSS=0V

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Supply voltage 1	VDD		(3.1)	3.3	3.4	V	VDD
Supply voltage 2	VDDIO		1.7	(1.8)	3.4	V	VDDIO
Input voltage for logic 1	VI1		0	―	VDD	V	RESETB,CSB,SCK, SDI
Input voltage for logic 2	VI2		0	―	VDDIO	V	VSYNC,HSYNC,CLK DR[7:0],DG[7:0],DB[7:0]
Operating temperature range	Top		-20	25	70	˚C	Panel surface temperature

8. Characteristics

8.1 DC Characteristics

A 8.1.1 Display Module

(Unless otherwise noted, Ta=25°C,VDD=3.3V,VDDIO=1.8V,VSS=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Input voltage for logic 1	VIH 1		0.8VDD	–	VDD	V	RESETB,CSB,SCK,SDI
	VIL 1		0	–	0.2VDD	V	
Input voltage for logic 2	VIH 2		0.8VDDIO	–	VDDIO	V	VSYNC,HSYNC,CLK DR[7:0],DG[7:0],DB[7:0]
	VIL 2		0	–	0.2VDDIO	V	
Operating Current	IDD	fCLK=37.1MHz Color bar display	–	(270)	TBD	mA	VDD
	IDDIO		–	(7)	TBD	mA	VDDIO
Standby Current	IDDs	Input signal : const R02h PSAVE=0	–	TBD	TBD	mA	VDD
	IDDIOs		–	TBD	TBD	mA	VDDIO

8.1.2 Backlight

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
LED forward current	IL		–	(25)	TBD	mA	VLEDA-VLEDK
LED forward voltage	VL	Ta=25°C, IL=(25)mA	–	(11.3)	TBD	V	
Estimated Life of LED	LL	Ta=25°C, IL=(25)mA Note	–	(15000)	–	hr	

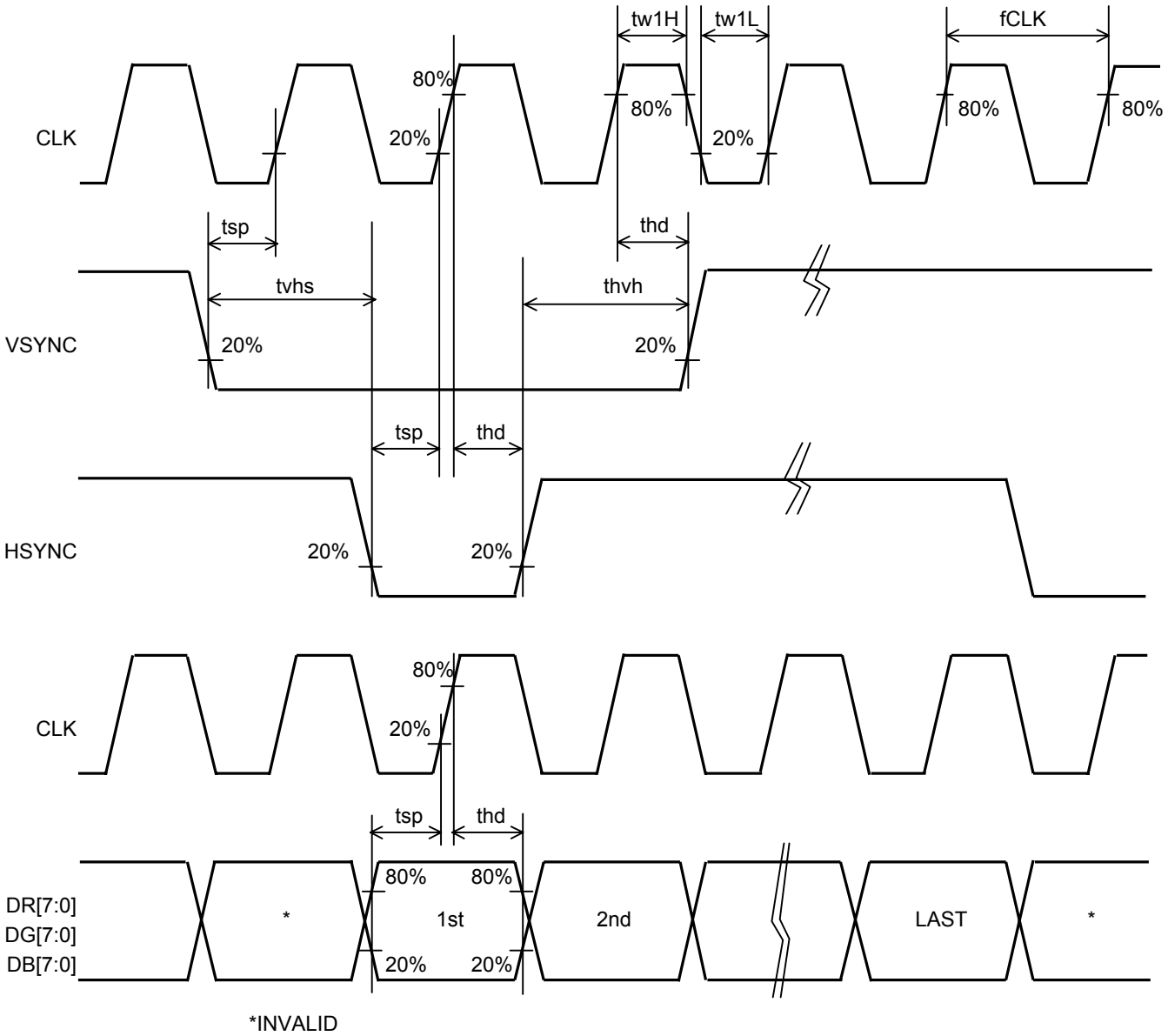
Note: - The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not as a guarantee.
- This figure is estimated for an LED operating alone. As the performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

8.2 AC Characteristics

A 8.2.1 RGB Interface Block

(Unless otherwise noted, Ta=25°C,VDD=3.3V,VDDIO=1.8V,VSS=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
CLK frequency	fCLK		—	37.1	(45)	MHz	CLK
CLK Low period	tw1L		(3)	—	—	ns	CLK
CLK High period	tw1H		(3)	—	—	ns	CLK
Setup time	tsp		(7)	—	—	ns	CLK, DR[7:0],DG[7:0],DB[7:0] HSYNC,VSYNC
Hold time	thd		(7)	—	—	ns	
Falling phase lag VSYNC/HSYNC	tvhs		(0)	—	—	CLK	HSYNC,VSYNC
Rising phase lag HSYNC/VSYNC	thvh		(0)	—	—	CLK	

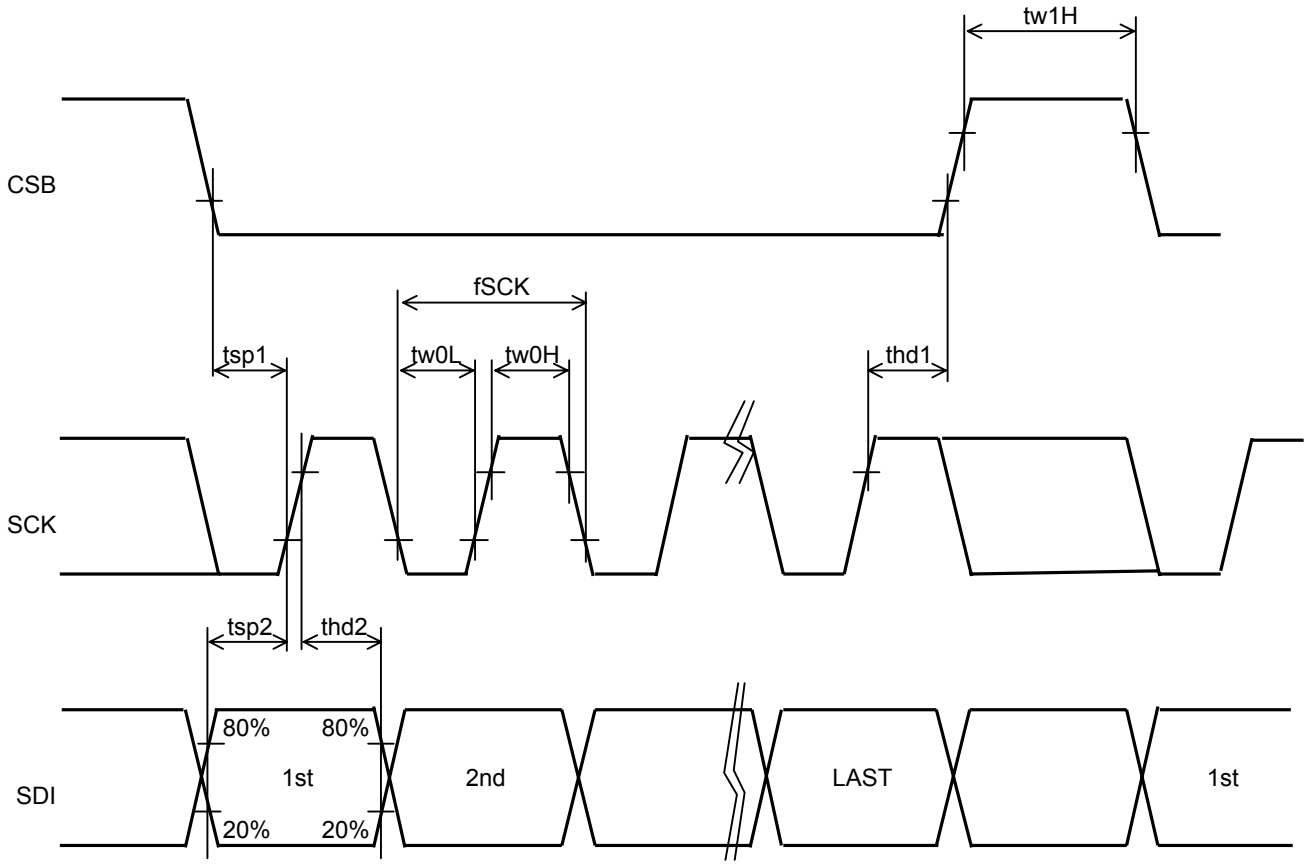


*INVALID

A 8.2.2 Serial Communication Block

(Unless otherwise noted, Ta=25°C,VDD=3.3V,VDDIO=1.8V,VSS=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
SCK pulse frequency	fSCK		(1)	(5)	(10)	MHz	SCK
SCK pulse Low period	tw0L		(20)	–	–	ns	SCK
SCK pulse High period	tw0H		(20)	–	–	ns	SCK
CSB pulse High period	tw1H		(20)	–	–	ns	CSB
CSB setup time	tsp1		(20)	–	–	ns	CSB,SCK
CSB hold time	thd1		(20)	–	–	ns	CSB,SCK
SDI setup time	tsp2		(20)	–	–	ns	SDI,SCK
SDI hold time	thd2		(20)	–	–	ns	SDI,SCK



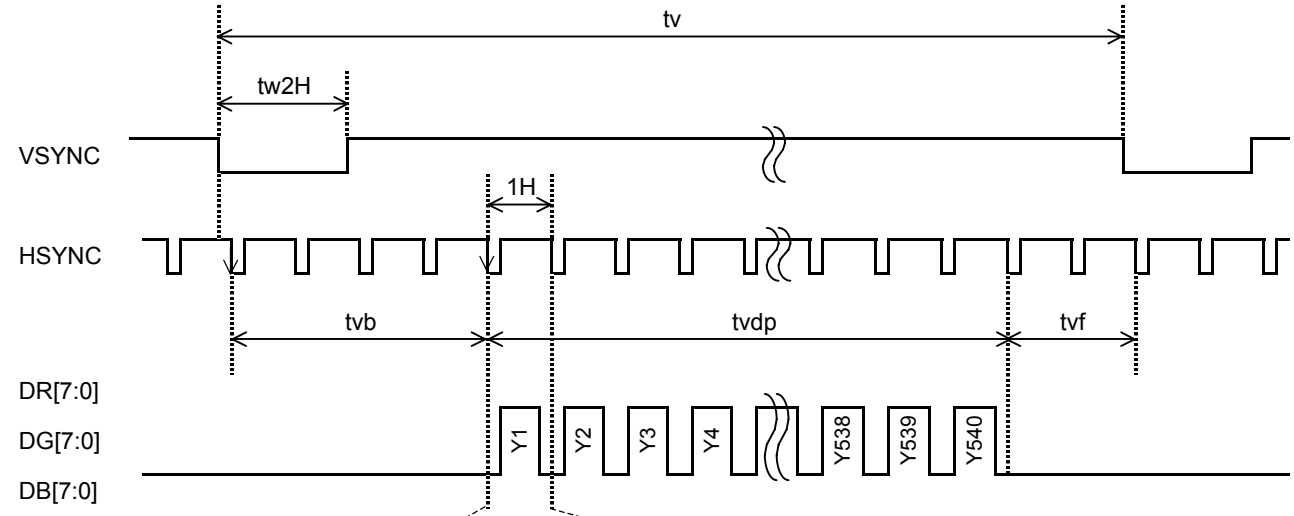
8.3 Input Timing Characteristics

Item	Symbol	Rating			Unit	Applicable terminal
		MIN	TYP	MAX		
CLK frequency	fCLK		37.1	(45)	MHz	CLK
VSYNC Frequency Note	fVSYNC	48	59.9	(66)	Hz	VSYNC
Number of Frame Line	tv	(559)	563		H	VSYNC,HSYNC
VSYNC Pulse Width	tw2H	2	3		H	
Vertical Back Porch	tvb	(17)	18		H	VSYNC,HSYNC
Vertical front Porch	tvf	(2)	5		H	DR[7:0],DG[7:0],DB[7:0]
Vertical Display Period	tvdp	—	540	—	H	
HSYNC frequency	fHSYNC	—	33.8	35.0	KHz	HSYNC
HSYNC Cycle	th	(1044)	1100		CLK	HSYNC,CLK
HSYNC Pulse Width	tw3H	5	20		CLK	
Horizontal Back Porch	thb	(56)	106		CLK	HSYNC,CLK
Horizontal front Porch	thf	(28)	34		CLK	DR[7:0],DG[7:0],DB[7:0]
Horizontal Display Period	thdp	—	960	—	CLK	

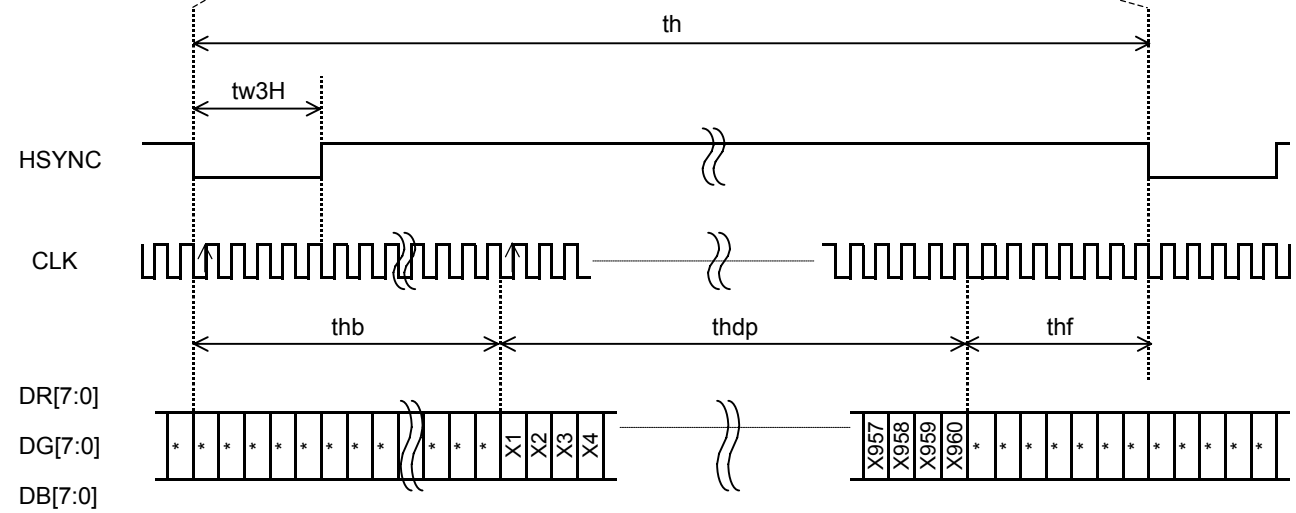
Note: The characteristic of this item is recommended standard.
Please use it after it confirms it enough like the display fineness etc.
When it comes off from this characteristic and it is used.

8.4 Driving Timing Chart

-Vertical Timing

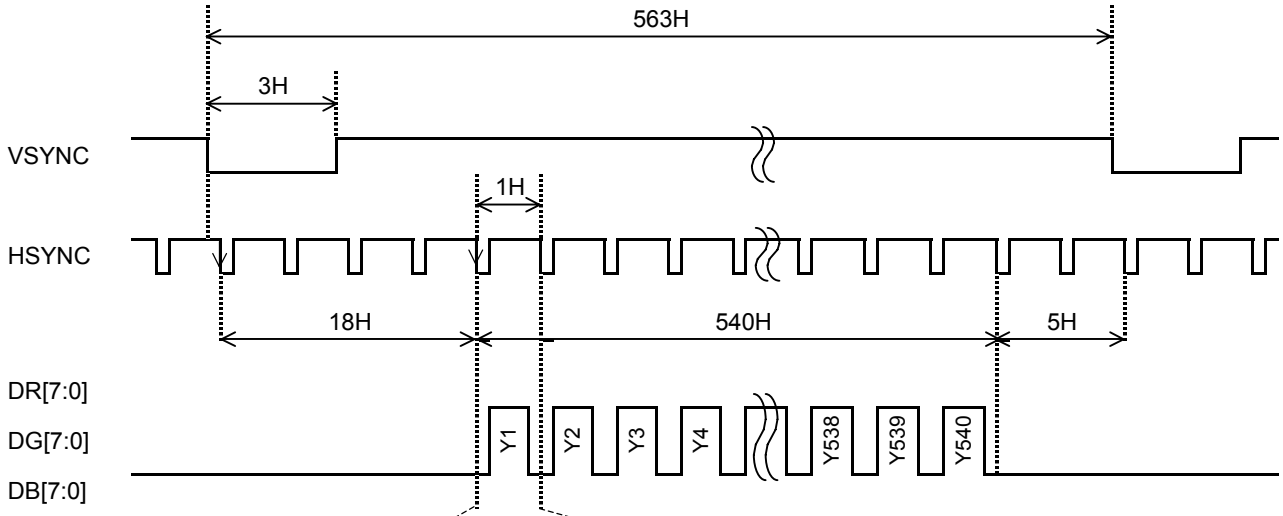


-Horizontal Timing

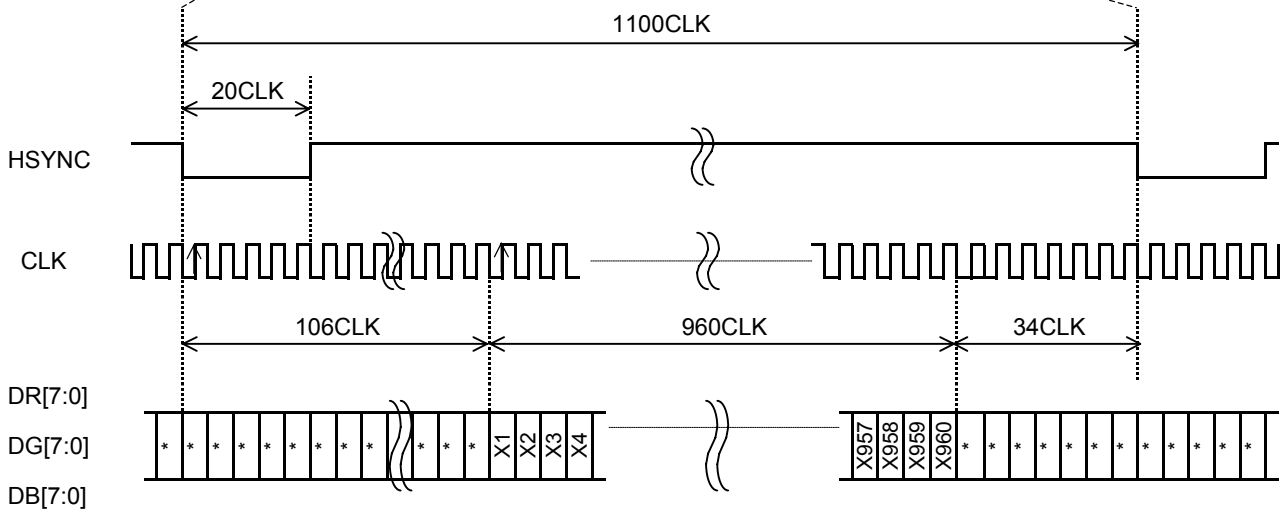


8.5 Example of Driving Timing Chart

-Vertical Timing



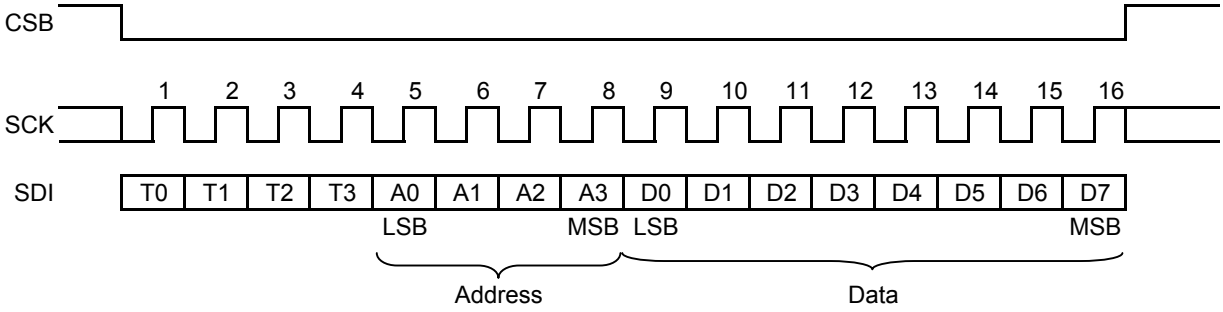
-Horizontal Timing



9. Description of Operation

9.1 Serial Communication Timing

After input signal of CSB drops from Hi to Lo, the Shift Resister loads 16 bits of serial data from SDI at the rising edge of the input signal of SCK.
When loaded SDI data during the low period of CSB is less than 16 bits, all loaded data are discarded .
When loaded SDI data during the low period of CSB is 16 bits or more, the last read of 16 bits is used .
Serial Communication Control Block is configurable at any time during display and standby mode as it is completely independent from other circuit run by CLK in the monitor.



9.2 Serial Communication Data

	T0-T3	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
R00h	0000	0	0	0	0	VBP0	VBP1	VBP2	VBP3	VBP4	VBP5	VBP6	VBP7
		initial				0	1	1	1	1	0	0	0
R01h		1	0	0	0	HBP0	HBP1	HBP2	HBP3	HBP4	HBP5	HBP6	HBP7
		initial				0	1	1	1	1	0	0	0
R02h		0	1	0	0	UDB	LRB	-	PSAVE	HPOL	VPOL	CKEG	TEST
		initial				0	0	0	0	1	1	0	0
R03h		1	1	0	0	HCKNMB0	HCKNMB1	HCKNMB2	HCKNMB3	HCKNMB4	HCKNMB5	HCKNMB6	HCKNMB7
		initial				1	1	0	0	1	0	0	0
R04h		0	0	1	0								
		initial											
R05h		1	0	1	0								
		initial											
R06h		0	1	1	0								
		initial											
R07h		1	1	1	0								
		initial											
R08h		0	0	0	1								
		initial											
R09h		1	0	0	1								
		initial											
R0Ah		0	1	0	1								
		initial											
R0Bh		1	1	0	1	TDR0	TDR1	TDR2	TDR3	TDR4	TDR5	TDR6	TDR7
		initial				0	0	0	0	0	0	0	0
R0Ch		0	0	1	1	TDG0	TDG1	TDG2	TDG3	TDG4	TDG5	TDG6	TDG7
		initial				0	0	0	0	0	0	0	0
R0Dh		1	0	1	1	TDB0	TDB1	TDB2	TDB3	TDB4	TDB5	TDB6	TDB7
		initial				0	0	0	0	0	0	0	0
R0Eh		0	1	1	1	TLINE	TPIX	TNINE	TCENT	TWAK	TRON	TGON	TBON
		initial				0	0	0	0	0	0	0	0
R0Fh		1	1	1	1								
		initial											

(1) R00h : Vertical Back Porch Period

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	0	VBP0	VBP1	VBP2	VBP3	VBP4	VBP5	VBP6	VBP7
				0	1	1	1	1	0	0	0

VBP[7:0] Setting numbers of HSYNC from the falling edge of VSYNC to valid RGB data (When VPOL=1).
When VPOL=0 , it becomes a count from the rising edge of VSYNC.
This command is executed by VSYNC immediately after the rising the edge of CSB.

(2) R01h : Horizontal Back Porch Period

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
1	0	0	0	HBP0	HBP1	HBP2	HBP3	HBP4	HBP5	HBP6	HBP7
				0	1	1	1	1	0	0	0

HBP[7:0] Setting numbers of CLK from the falling edge of HSYNC to valid RGB data (When HPOL=1).
When HPOL=0 , it becomes a count from the rising edge of HSYNC.
This command is executed by VSYNC immediately after the rising the edge of CSB.

(3) R02h : Interface Mode

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
0	1	0	0	UDB	LRB	GAMS	PSAVE	HPOL	VPOL	CKEG	TEST
				0	0	0	0	1	1	0	0

UDB Setting for vertical flip display. The selected display mode is carried out by VSYNC.
0 : Normal Display
1 : Vertical Flip Display (Up/Down)

LRB Setting for horizontal flip display. The selected display mode is carried out by VSYNC.
0 : Normal Display
1 : Horizontal Flip Display (Right/Left)

PSAVE Setting into Standby mode. It is carried out by the rising edge of CSB.
0 : Standby mode
Power consumption is significantly reduced in standby mode .
Serial data can be received by serial communication block even in standby mode.
1 : Normal operation

HPOL Setting the polarity of HSYNC. It is carried out by the rising edge of CSB.
0 : HSYNC is High active (Normally Low)
1 : HSYNC is Low active (Normally High)

VPOL Setting the polarity of VSYNC. It is carried out by the rising edge of CSB.
0 : VSYNC is High active (Normally Low)
1 : VSYNC is Low active (Normally High)

CKEG Setting the timing of data read. It is carried out by the rising edge of CSB.
0 : The data is read on the rising edge of CLK
1 : The data is read on the falling edge of CLK

TEST The TEST pattern is inserted in the display image. It is carried out by VSYNC.
0 : Normal Display
1 : The TEST pattern is inserted
The inserted TEST pattern is specified by register R0Bh-R0Eh.

(4) R03h : Setting 1H period

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
1	1	0	0	HCKNMB0	HCKNMB1	HCKNMB2	HCKNMB3	HCKNMB4	HCKNMB5	HCKNMB6	HCKNMB7
				1	1	0	0	1	0	0	0

HCKNMB[7:0] Setting number of CLKs per 1H period
A set value calculates the following expressions. It drops below the decimal point.

HCKNMB = (number of CLK per 1H period - 1024) ÷ 4

Example1. In case of Number of 1H period = 1100
HCKNMB[7:0] = (1100 - 1024) ÷ 4 = 19(dec) = 0001_0011(bin)

Example2. In case of Number of 1H period = 1430
HCKNMB[7:0] = (1430 - 1024) ÷ 4 = 101.5 → 101(dec) = 0110_0101(bin)

(5) R0Bh : R Data of TEST pattern (valid when R02h[D7:TEST] =1)

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
1	1	0	1	TDR0	TDR1	TDR2	TDR3	TDR4	TDR5	TDR6	TDR7
				0	0	0	0	0	0	0	0

TDR[7:0] Setting for Red data of TEST pattern when R02h[D7:TEST]=1. It is carried out by VSYNC.

(6) R0Ch : G Data of TEST pattern (valid when R02h[D7:TEST] =1)

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
0	0	1	1	TDG0	TDG1	TDG2	TDG3	TDG4	TDG5	TDG6	TDG7
				0	0	0	0	0	0	0	0

TDG[7:0] Setting for Green data of TEST pattern when R02h[D7:TEST]=1. It is carried out by VSYNC.

(7) R0Dh : B Data of TEST pattern (valid when R02h[D7:TEST] =1)

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
1	0	1	1	TDB0	TDB1	TDB2	TDB3	TDB4	TDB5	TDB6	TDB7
				0	0	0	0	0	0	0	0

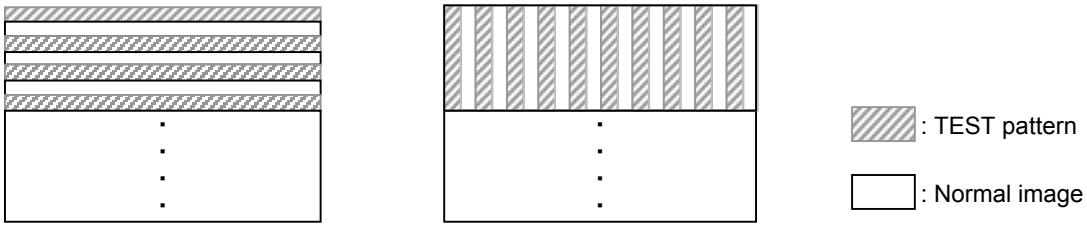
TDB[7:0] Setting for Blue data of TEST pattern when R02h[D7:TEST]=1. It is carried out by VSYNC.

(8) R0Eh : TEST patterns (valid when R02h[D7:TEST]=1)

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
0	1	1	1	TLINE	TPIX	TNINE	TCENT	TWAK	TRON	TGON	TBON
				0	0	0	0	0	0	0	0

TLINE Control to insert the TEST pattern at intervals of one line . It is carried out by VSYNC.
0 : Normal Display
1 : At intervals of one line , the TEST pattern is inserted.

TPIX Control to insert the TEST pattern at intervals of one pixel . It is carried out by VSYNC.
0 : Normal Display
1 : At intervals of one pixel , the TEST pattern is inserted.

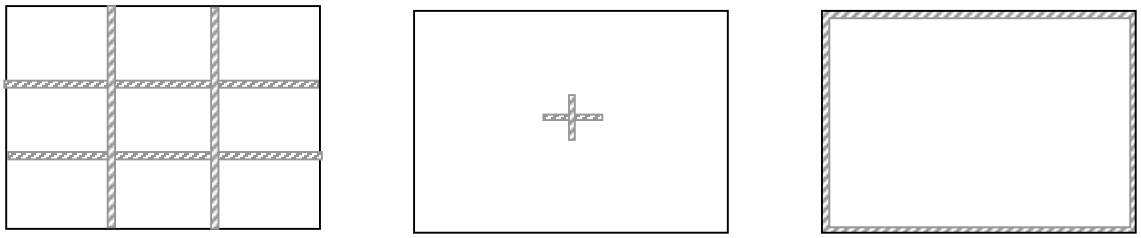


<TLINE=1> <TPIX=1>

TNINE Control the line which divides the screen into nine . It is carried out by VSYNC .
0 : Normal Display
1 : The line which divides the screen into nine is inserted.

TCENT Control the cross line which shows the center on the screen . It is carried out by VSYNC .
0 : Normal Display
1 : The cross line which shows the center on the screen is inserted.

TWAK Control the line which shows the frame of the screen . It is carried out by VSYNC .
0 : Normal Display
1 : The line which shows the frame of the screen is inserted.



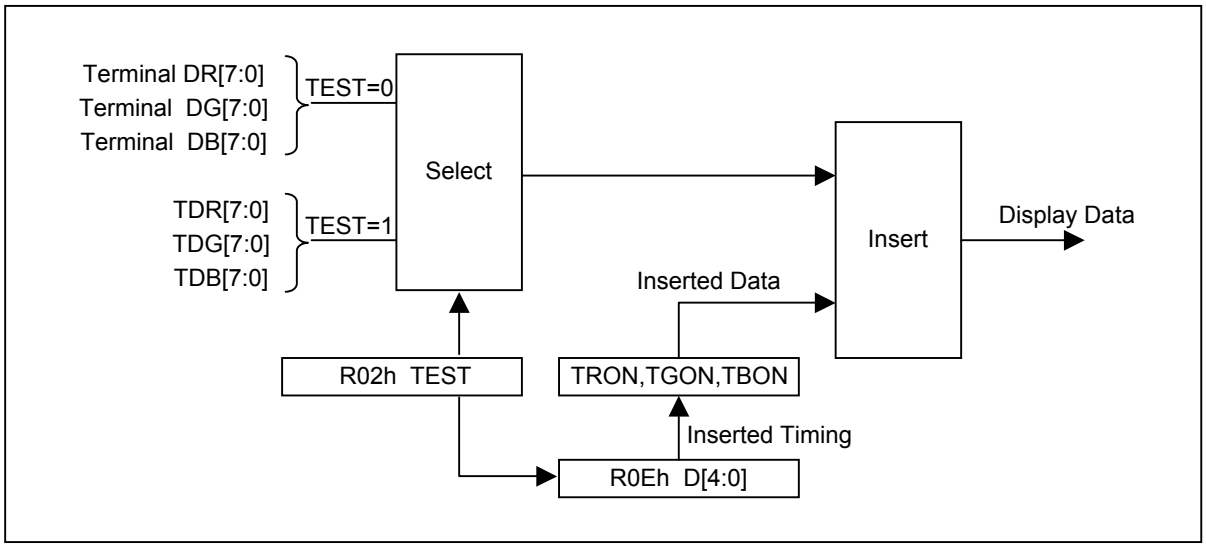
<TNINE=1> <TCENT=1> <TWAK=1>

TRON ON/OFF of a RED pixel of the TEST pattern . It is carried out by VSYNC .
0 : R OFF (DR[7:0]=00h)
1 : R ON (DR[7:0]=FFh)

TGON ON/OFF of a GREEN pixel of the TEST pattern . It is carried out by VSYNC .
0 : G OFF (DG[7:0]=00h)
1 : G ON (DG[7:0]=FFh)

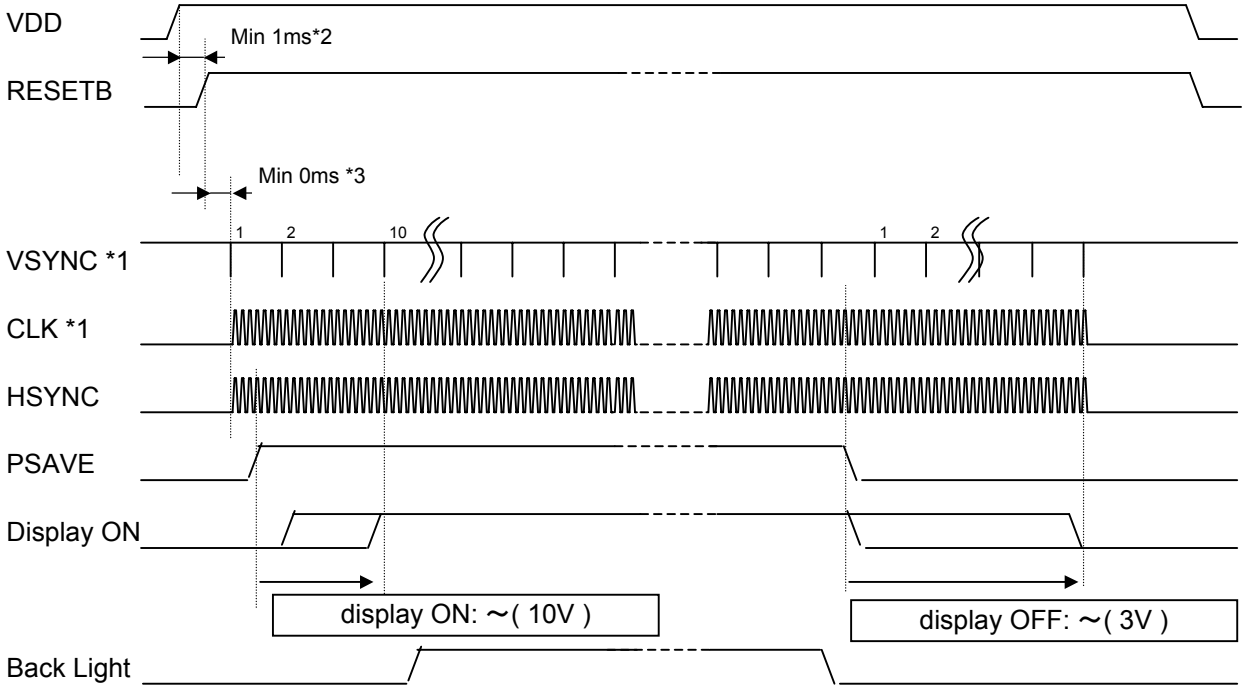
TBON ON/OFF of a BLUE pixel of the TEST pattern . It is carried out by VSYNC .
0 : B OFF (DB[7:0]=00h)
1 : B ON (DB[7:0]=FFh)

- The logic of each test signal is as follows.



9.3 Power ON/OFF sequence

TBD



*1 CLK is used for Timing Generator CLK on FPC
It becomes the operation after CLK(DOTCLK),VSYNC input.

*2 After the power suplly,Please excute RESETB.

*3 There is no regulations at time until each signal is supplied from RESETB"H"
But meanwhile, It is necessary to fix each signal to "H"or"L".

*4 It is necessary to supply VSYNC and CLK for (3V) period or less from PSAVE "L" to turning off the power supply without leaving the afterimage.

10. Characteristics

10.1 Optical Characteristics

< Measurement Condition >

Measuring instruments: CS1000（KONICA MINOLTA）, LCD7000(OTSUKA ELECTRONICS）, EZcontrast160D（ELDIM）

Driving condition: Typical Rating of "6. Recommended Operating Conditions". Optimized VCOMDC VLCD(White)=(V6-V7)/2 , VLCD(Black)=(V0-V13)/2

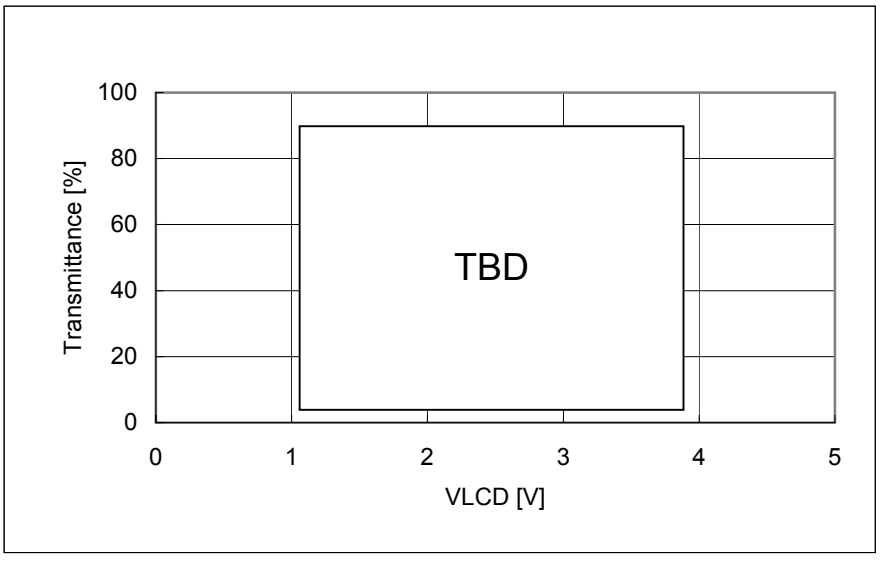
Backlight: IL=(25)mA

Measured temperature: Ta=25°C

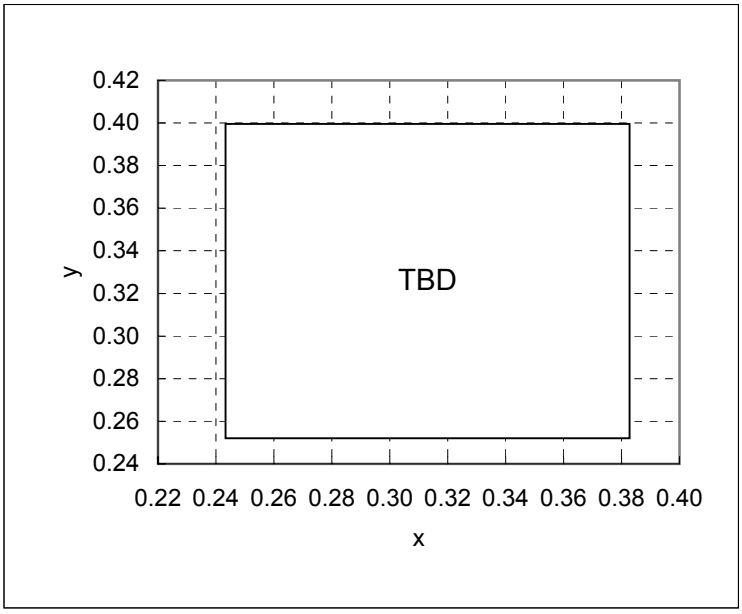
Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Remark
Response time	Rise time	TON	VLCD=(TBD)	－	－	TBD	ms	1	※
	Fall time	TOFF	VLCD=(TBD)	－	－	TBD	ms		
Contrast ratio		CR	VLCD=(TBD)	TBD	TBD	－		2	
Viewing angle	Left	θL	VLCD=(TBD) CR≧(TBD)	TBD	－	－	deg	3	※
	Right	θR		TBD	－	－	deg		
	Up	φU		TBD	－	－	deg		
	Down	φD		TBD	－	－	deg		
V-T threshold voltage		V90		TBD	TBD	TBD	V	4	※
		V50		TBD	TBD	TBD	V		
		V10		TBD	TBD	TBD	V		
White V-T Curve				White V-T Curve					Reference
White Chromaticity		x	VLCD=(TBD)	White chromaticity range				5	
		y							
Burn-in				No noticeable burn-in image should be observed after 2 hours of window pattern display.				6	
Center brightness			VLCD=(TBD)	TBD	TBD	－	cd/m^2	7	
Brightness distribution			VLCD=(TBD)	TBD	－	－	%	8	

* Note number 1 to 8: Refer to the APPENDIX of "Reference Method for Measuring Optical Characteristics".

※ Measured in the form of LCD module.



White V-T Curve



White Chromaticity Range

【White Chromaticity Range】

x	y
TBD	TBD
TBD	TBD
TBD	TBD
TBD	TBD
TBD	TBD
TBD	TBD
TBD	TBD

10.2 Temperature Characteristics

< Measurement Condition >
Measuring instruments: CS1000（KONICA MINOLTA）, LCD7000(OTSUKA ELECTRONICS）
Driving condition: Typical Rating of "6. Recommended Operating Conditions".
Optimized VCOMDC
VLCD(White)=(V6-V7)/2 , VLCD(Black)=(V0-V13)/2
Backlight: IL=(25)mA

Item			Specification		Remark
			Ta＝－10˚C	Ta＝70˚C	
Contrast ratio		CR	TBD	TBD	
Response time	Rise time	TON	TBD	TBD	※
	Fall time	TOFF	TBD	TBD	※
Display Quality			No noticeable display defect or ununiformity should be observed.		Use the criteria for judgment specified in the section 11.

※ Measured in the form of LCD module.

11. Criteria of Judgment

11.1 Defective Display and Screen Quality

Test Condition:	Observed TFT-LCD monitor from front during operation with the following conditions
Driving Signal	Raster Pattern (RGB in monochrome, white, black)
Signal condition	TBD
Observation distance	30 cm
Illuminance	200 to 350 lx
Backlight	IL=(25)mA

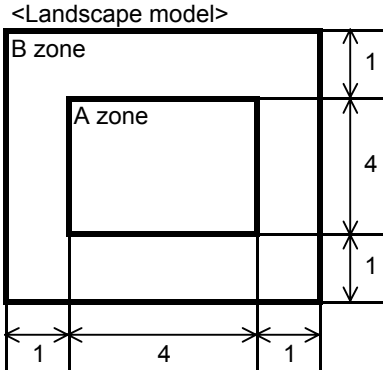
Defect item		Defect content		Criteria
Display Quality	Line defect	Black, White or color line, 5 or more neighboring defective dots.		Not exists
	Dot defect	Uneven brightness due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot) High bright dot: Visible through 2% ND filter at VLCD=(TBD)V Low bright dot: Visible through 5% ND filter at VLCD=(TBD)V Dark dot: Appear dark through white display at VLCD=(TBD)V		Refer to table 1
Screen Quality	Dirt	Point-like uneven brightness (white stain, black stain etc)		Invisible through 1% ND filter
	Foreign particle	Point-like	0.25mm<φ	N=0
			0.20<φ≦0.25mm	N≦2
			φ≦0.20mm	Ignored
		Liner	3.0mm<length and 0.08mm<width	N=0
			length≦3.0mm or width≦0.08mm	Ignored
	Others			Use boundary sample for judgment when necessary

φ(mm): Average diameter = (major axis + minor axis)/2
Permissible number: N

Table 1

Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
A	0	2	2	2	4 or less neighboring defective dots are counted as one. Permissible distance between same color bright dots : 3 mm or more
B	1	2	2	3	
Total	1	2	2	3	

<Landscape model>



Division of A and B areas
B area: Active area
Dimensional ratio between A and B areas: 1: 4: 1 (Refer to the left figure)

11.2 Screen and Other Appearance

Testing conditions

Observation distance 30cm

Illuminance 1200～2000 lx

Item		Criteria	Remark
Polarizer	Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only (Refer to the section 3.2 "Outward form")
S-case		No functional defect occurs	
FPC cable		No functional defect occurs	
Connector		No functional defect occurs	

12. Reliability Test

Test item		Test condition	number of failures /number of examinations
Durability test	High temperature storage	Ta=80°C 240H	TBD／3
	Low temperature storage	Ta=(-30°C) 240H	TBD／3
	High temperature & high humidity storage	Ta=60°C, RH=90% 240H non condensing ※	TBD／3
	High temperature operation	Tp=70°C 240H	TBD／3
	Low temperature operation	Tp=(-20°C) 240H	TBD／3
	High temp & humid operation	Tp=40°C, RH=90% 240H non condensing ※	TBD／3
	Thermal shock storage	(-30)←→80°C(30min/30min) 100 cycles	TBD／3
Mechanical environmental test	Surface discharge test (Non operation)	C=250pF, R=100Ω, V=±12kV Each 5 times of discharge in both polarities on the center of screen with the case grounded.	TBD／3
	Vibration test	Total amplitude 1.5mm, f=10～55Hz, X,Y,Z directions for each 2 hours	TBD／3
	Impact test	Use ORTUS TECHNOLOGY original jig (see next page)and make an impact with peak acceleration of 1000m/s2 for 6 msec with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS 60068-2-27-1995.	TBD／3
Packing test	Packing vibration-proof test	Acceleration of 19.6m/s^2 with frequency of 10→55→10Hz, X,Y, Zdirection for each 30 minutes	TBD／1 Packing
	Packing drop test	Drop from 75cm high. 1 time to each 6 surfaces, 3 edges, 1 corner	TBD／1 Packing

Note:Ta=ambient temperature Tp=Panel temperature

※ The profile of high temperature/humidity storage and High Temperature/humidity operation (Pure water of over 10MΩ·cm shall be used.)

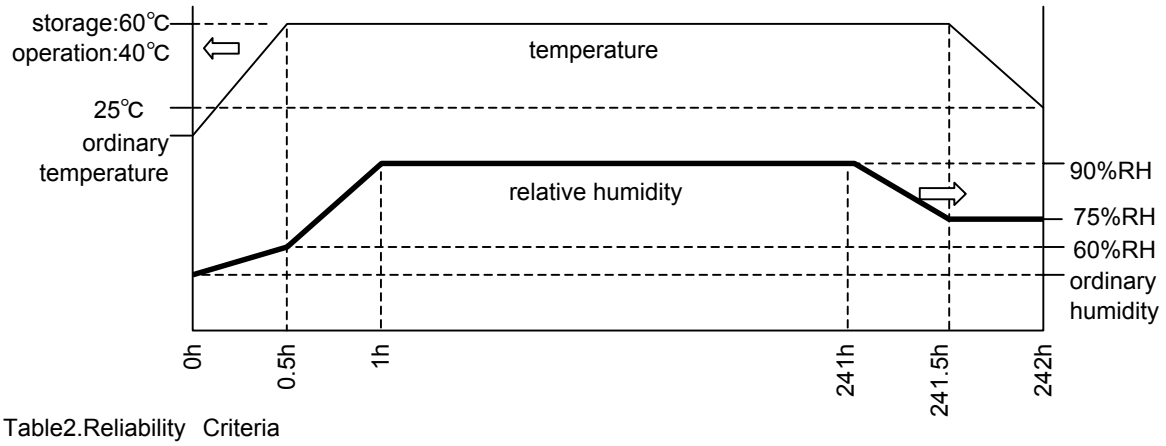
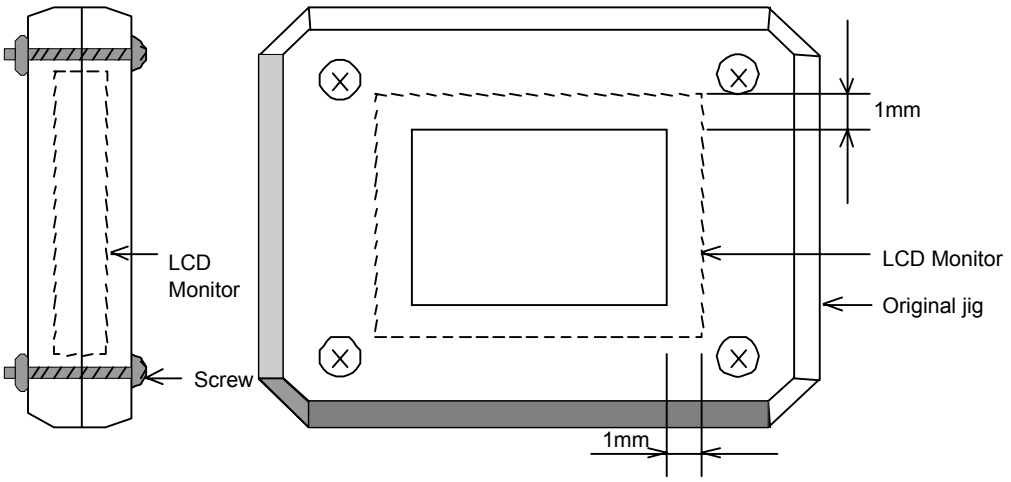


Table2.Reliability Criteria

Measure the parameters after leaving the monitor at the ordinary temperature for 2 hours or more after the test completion.

item	Standard	Remarks
Display quality	No visible abnormality shall be seen.	As criteria of "11 Criteria of Judgment".
Contrast ratio	40 or more	

ORTUS TECHNOLOGY Original Jig



13. Packing Specifications

TBD

14. Handling Instruction

14.1 Cautions for Handling LCD panels

Caution

(1) Do not make an impact on the LCD panel glass because it may break and you may get injured from it.

(2) If the glass breaks, do not touch it with bare hands.
（Fragment of broken glass may stick you or you cut yourself on it.

(3) If you get injured, receive adequate first aid and consult a medial doctor.

(4) Do not let liquid crystal get into your mouth.
（If the LCD panel glass breaks, try not let liquid crystal get into your mouth even toxic property of liquid crystal has not been confirmed.

(5) If liquid crystal adheres, rinse it out thoroughly.
（If liquid crystal adheres to your cloth or skin, wipe it off with rubbing alcohol or wash it thoroughly with soap. If liquid crystal gets into eyes, rinse it with clean water for at least 15 minutes and consult an eye doctor.

(6) If you scrap this products, follow a disposal standard of industrial waste that is legally valid in the community, country or territory where you reside.

(7) Do not connect or disconnect this product while its application products is powered on.

(8) Do not attempt to disassemble or modify this product as it is precision component.

(9) For protection your circuit, we recommend you to add excess current protection circuit to power supply.

Caution **This mark is used to indicate a precaution or an instruction which, if not correctly observed, may result in bodily injury, or material damages alone.**

14.2 Precautions for Handling

1) Wear finger tips at incoming inspection and for handling the TFT monitors to keep display quality and keep the working area clean.
Do not touch the surface of the monitor as it is easily scratched.

2) Wear grounded wrist-straps and use electrostatic neutralization blowers to prevent static charge and discharge when handling the TFT monitors as the LED in this TFT monitors is damageable to electrostatic discharge.
Designate an appropriate operating area, and set equipment, tools, and machines properly when handling this product.

3) Avoid strong mechanical shock including knocking, hitting or dropping to the TFT monitors for protecting their glass parts. Do not use the TFT monitors that have been experienced dropping or strong mechanical shock.

4) Do not use or storage the TFT monitors at high temperature and high humidity environment.
Particularly, never use or storage the TFT monitors at a location where condensation builds up.

5) Avoid using and storing TFT monitors at a location where they are exposed to direct sunlight or ultraviolet rays to prevent the LCD panels from deterioration by ultraviolet rays.

6) Do not stain or damage the contacts of the connector .
FPC cable needs to be inserted until it can reach to the end of connector slot.
During insertion, make sure to keep the cable in a horizontal position to avoid an oblique insertion.
Otherwise, it may cause poor contact or deteriorate reliability of the connector.

7) Peel off the protective film on the TFT monitors during mounting process.
Refer to the section 14.5 on how to peel off the protective film.
We are not responsible for electrostatic discharge failures or other defects occur when peeling off the protective film.

14.3 Precautions for Operation

1) Since this TFT monitors are not equipped with light shielding for the driver IC, do not expose the driver IC to strong lights during operation as it may cause functional failures.

2) When turning off the power, turn off the input signal before or at the same timing of switching off the power.

3) Do not plug in or out the connector while power supply is switch on.
Plug the connector in and out while power supply is switched off.

4) Do not operate the TFT monitors in the strong magnetic field. It may break the TFT monitors.

5) Do not display a fixed image on the screen for a long time.
Use a screen-saver or other measures to avoid a fixed image displayed on the screen for a long time.
Otherwise, it may cause burn-in image on the screen due the characteristics of liquid crystal.

14.4 Storage Condition for Shipping Cartons

Storage environment

- Temperature: 0 to 40°C
- Humidity: 60%RH or less
  No-condensing occurs under low temperature with high humidity condition.
- Atmosphere: No poisonous gas that can erode electronic components and/or wiring materials should be detected.
- Time period: 3 months
- Unpacking: To prevent damages caused by static electricity, anti-static precautionary measures (e.g. earthing, anti-static mat) should be implemented.
- Maximum piling up: (TBD) cartons

14.5 Precautions for Peeling off the Protective film

The followings work environment and work method are recommended to prevent the TFT monitors from static damage or adhesion of dust when peeling off the protective films.

A) Work Environment

a) Humidity: 50 to 70 %RH, Temperature15 to 27°C
b) Operators should wear conductive shoes, conductive clothes, conductive finger tips and grounded wrist-straps. Anti-static treatment should be implemented to work area's floor.
c) Use a room shielded against outside dust with sticky floor mat laid at the entrance to eliminate dirt.

B) Work Method

TBD

APPENDIX

Reference Method for Measuring Optical Characteristics and Performance

1. Measurement Condition

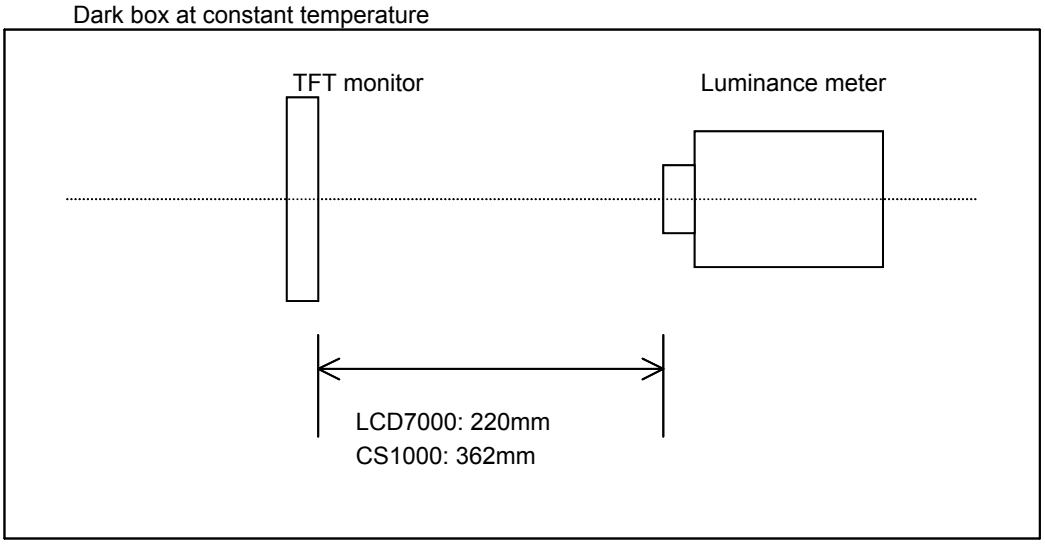
Measuring instruments: CS1000（KONICA MINOLTA）, LCD7000(OTSUKA ELECTRONICS）,EZcontrast160D（ELDIM）

Driving condition: Refer to typical rating of the section "Recommended Operating Conditions".

Measured temperature: 25˚C unless specified

Measurement system: See the chart below. The luminance meter is placed on the normal line of measurement system.

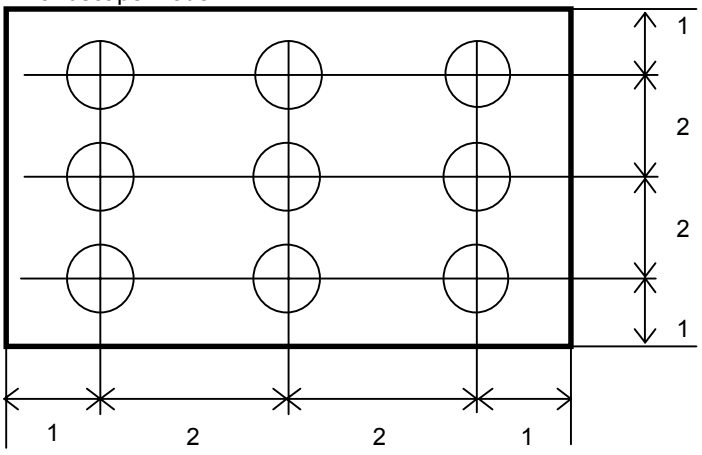
Measurement point: At the center of the screen unless otherwise specified



Measurement is made after 30 minutes of lighting of the backlight.

Measurement point: At the center point of the screen
Brightness distribution: 9 points shown in the following drawing.

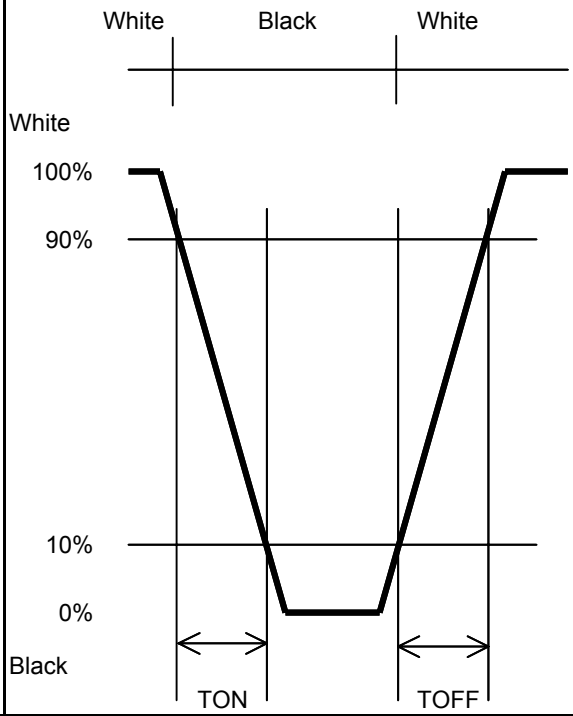
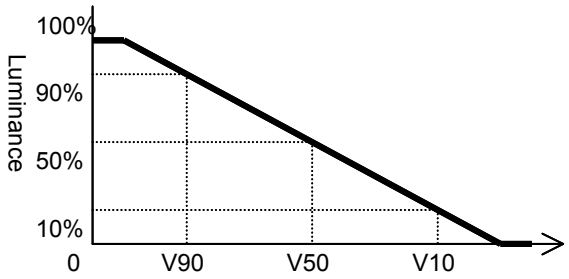
<Landscape model>



Dimensional ratio of active area

Backlight IL=(25)mA

2. Test Method

Notice	Item	Test method	Measuring instrument	Remark
1	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. 	LCD7000	Black display VLCD=(TBD)V White display VLCD=(TBD)V TON Rise time TOFF Fall time
2	Contrast ratio	Measure maximum luminance Y1(VLCD=(TBD)V) and minimum luminance Y2(VLCD=(TBD)V) at the center of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast ratio = Y1/Y2 Diameter of measuring point: 8mmφ	CS1000	
3	Viewing angle Horizontalθ Verticalφ	Move the luminance meter from right to left and up and down and determine the angles where contrast ratio is (TBD).	EZcontrast160D	
4	V-T threshold value	Change VLCD by 0.1V step and plot the points where the luminance is 90% as V90, 50% as V50 and 10% as V10 of maximum luminance. 	LCD7000	
5	White chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system at VLCD = (TBD)V Color matching faction: 2°view	CS1000	

Notice	Item	Test method	Measuring instrument	Remark
6	Burn-in	Visually check burn-in image on the screen after 2 hours of "window display" (VLCD=(TBD)V).		At optimized VCOMDC
7	Center brightness	Measure the brightness at the center of the screen.	CS1000	
8	Brightness distribution	(Brightness distribution) = 100 x B/A % A : max. brightness of the 9 points B : min. brightness of the 9 points	CS1000	