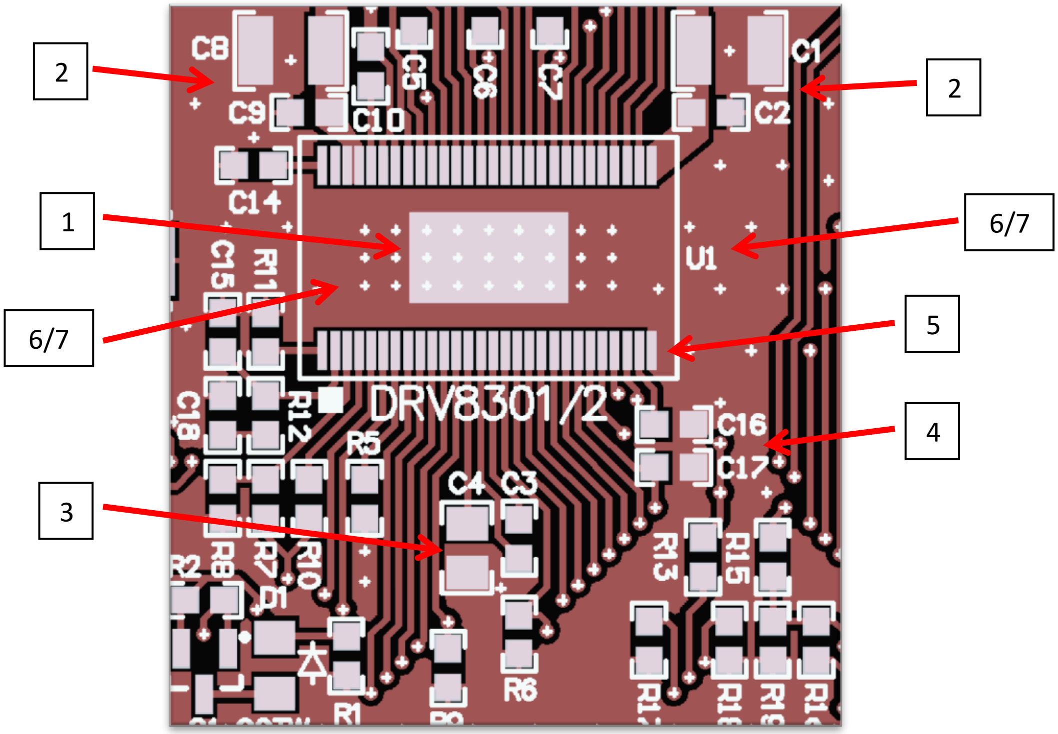
PCB LAYOUT RECOMMENDATIONS

Below are a few layout recommendations to utilize when designing a PCB for the DRV8301/2.



1. The DRV8301/2 makes an electrical connection to GND through the PowerPAD™. Always check to ensure that the PowerPAD™ has been properly soldered.
2. C1, C2, C8, & C9, PVDD decoupling capacitors should be placed close to their corresponding pins with a low impedance path to device GND (PowerPAD™).
3. C4, GVDD capacitor should be placed close its corresponding pin with a low impedance path to device GND (PowerPAD™).
4. C16 & C17, AVDD & DVDD capacitors should be placed close to their corresponding pins with a low impedance path to the AGND pin. It is preferable to make this connection without jumping layers.
5. AGND should be tied to device GND (PowerPAD™) through a low impedance trace/copper fill.
6. Add many vias to reduce the impedance of the ground path from the top to bottom side.
7. Try to clear the space around and underneath the DRV8301/2 to allow for better heat spreading from the PowerPAD™.

Designator	Recommended Value	Description
C1, C8	2.2uF	CAP CER 2.2UF 100V 10% X7R
C2, C9	0.1uF	CAP CER 0.1UF 100V 10% X7R
C4	2.2uF	CAP CER 2.2UF 25V 10% X7R
C16, C17	1.0uF	CAP CER 1UF 25V 10% X7R