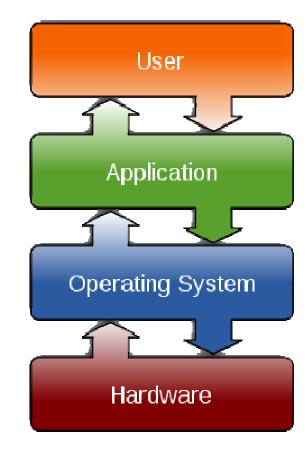
Introduction to SYS/BIOS

Intro to SYS/BIOS

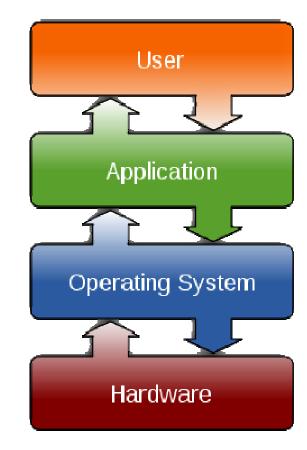
- Overview
- Threads and Scheduling
- Creating a BIOS Thread
- System Timeline
- Real-Time Analysis Tools
- Create A New Project
- BIOS Configuration (.CFG)
- Platforms
- For More Information



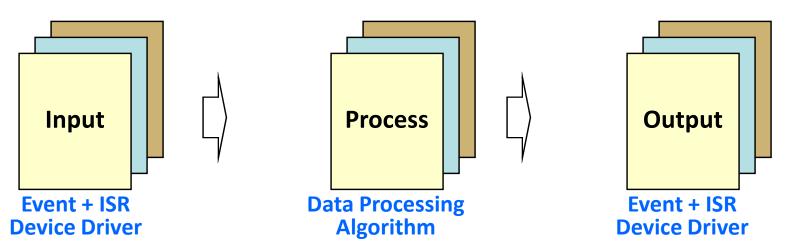
Intro to SYS/BIOS

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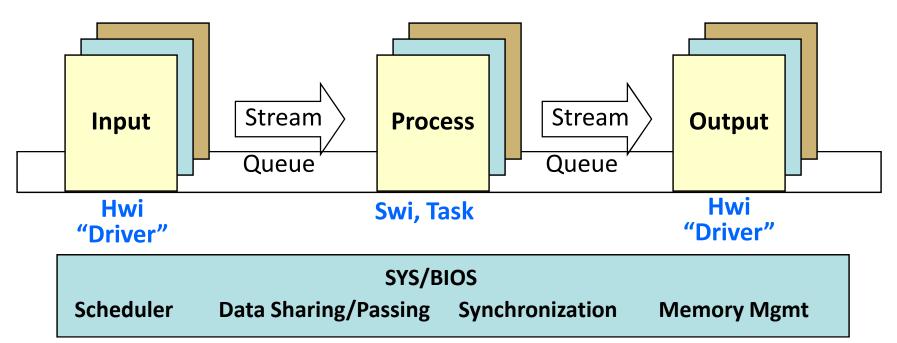
Need for an Operating System



- Simple system: single I-P-O is easy to manage
- As system complexity increases (multiple threads):
 - Can they all meet real time ?
 Synchronization of events?
 - Priorities of threads/algos ?
- Data sharing/passing ?
- Two options: "home-grown" or use existing (SYS/BIOS) (either option requires overhead)
- If you choose an existing O/S, what should you consider?
- \succ Is it modular? Is it easy to use?
- > How much does it cost?

- \succ Is it reliable?
- > Data sharing/passing?
- > What code overhead exists?

SYS/BIOS Overview

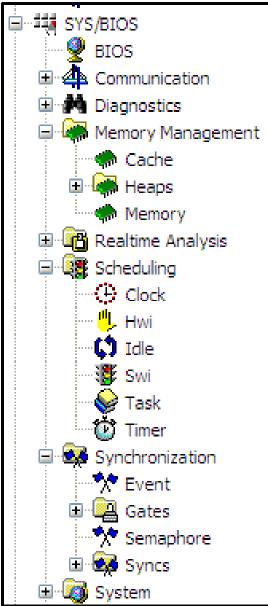


SYS/BIOS is a scalable, real-time kernel used in 1000s of systems today:

- Pre-emptive <u>Scheduler</u> to design system to meet real-time (including sync/priorities)
- <u>Modular</u> Include only what is needed
- •API pre-defined interface for inter-thread communications
- <u>Reliable</u> 1000s of applications have used it for more than 10 years
- <u>Footprint</u> deterministic, small code size, can choose which modules you desire
- Cost <u>free of charge</u>

TEXAS INSTRUMENTS

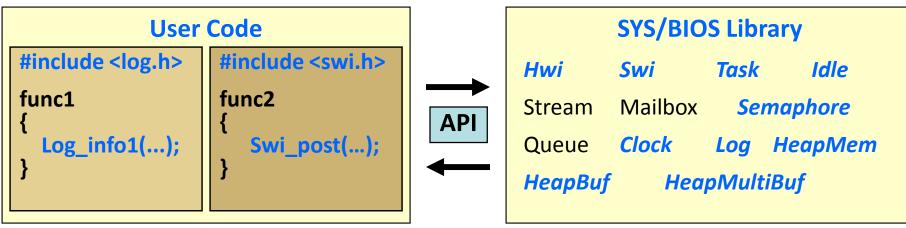
SYS/BIOS Modules & Services



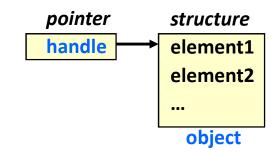
BIOS Configuration

- Memory Management
 - Cache
 - Heaps
- Realtime Analysis
 - Logs
 - Loads
 - Execution Graph
- Scheduling
 - All thread types
- Synchronization
 - Events
 - Gates
 - Semaphores

SYS/BIOS Environment



- SYS/BIOS is a <u>library</u> that contains modules with a particular interface and data structures.
- Application Program Interfaces (API) define the interactions (methods) with a module and data structures (objects).
- Objects are structures that define the state of a component.
 - Pointers to objects are called handles.
 - Object-based programming offers:
 - Better encapsulation and abstraction
 - Multiple instance ability



Definitions / Vocabulary

In this workshop, we'll be using these terms often:

Real-time System

> Where processing must keep up with the rate of I/O

Function

Sequence of program instructions that produce a given result





Function that executes within a specific context (regs, stack, PRIORITY)

API

Application Programming Interface provides <u>methods</u> for interacting with library routines and data objects

TEXAS INSTRUMENTS

Multicore Training

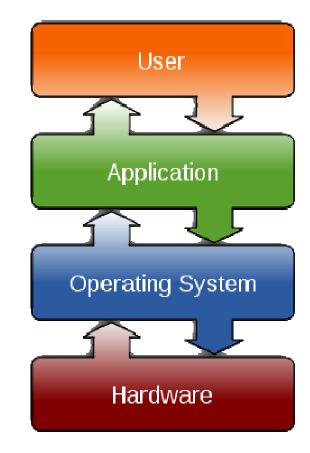
Comparing RTOS and GP/OS

	GP/OS (e.g. Linux)	RTOS (e.g. SYS/BIOS)		
Scope	General	Specific		
Size	Large: 5M-50M	Small: 5K-50K		
Event response	1ms to .1ms	100 – 10 ns		
File management	FAT, etc.	FatFS		
Dynamic Memory	Yes	Yes		
Threads	Processes, pThreads, Ints	Hwi, Swi, Task, Idle		
Scheduler	Time Slicing	Preemption		
Host Processor	ARM, x86, Power PC ARM, MSP430, D			

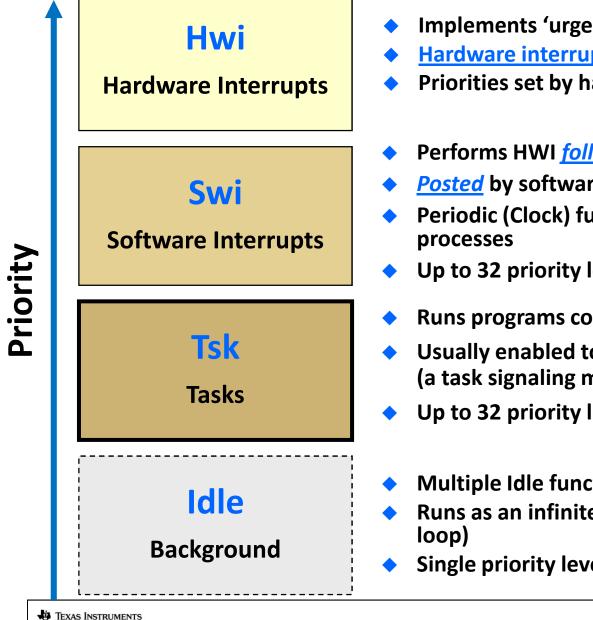
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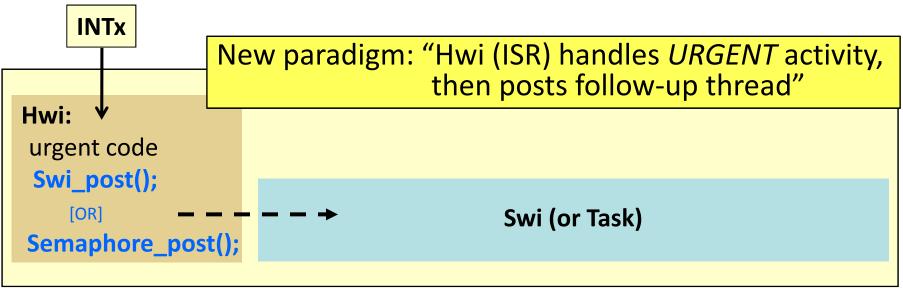


SYS/BIOS Thread Types



- Implements 'urgent' part of real-time event
- Hardware interrupt triggers ISRs to run
- **Priorities set by hardware**
- Performs HWI *follow-up* activity
- *Posted* by software
- Periodic (Clock) functions are prioritized as Swi
- Up to 32 priority levels
- **Runs programs concurrently under separate contexts**
- Usually enabled to run by posting a *semaphore* (a task signaling mechanism)
- Up to 32 priority levels
- **Multiple Idle functions**
- **Runs as an infinite loop (like traditional** while(1)
- **Single priority level**

Hwi Signaling Swi/Task



← ints disabled → rather than all this time

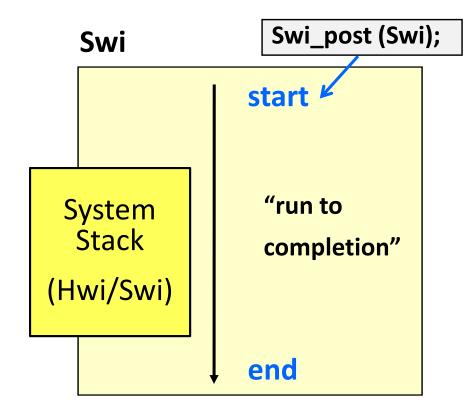
Hwi

- Fast response to interrupts
- Minimal context switching
- High priority only
- Can post Swi
- Use for urgent code only then post follow up activity

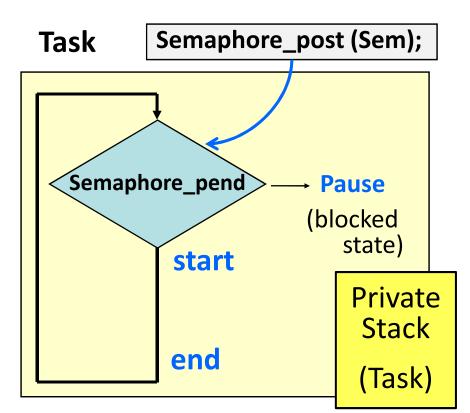
Swi

- Latency in response time
- Context switch performed
- Selectable priority levels
- Can post another Swi
- Execution managed by scheduler

Swi and Tasks



- Similar to hardware interrupt, but triggered when posted
- All Swi activities share system software stack with Hwi activities.



- Unblocking triggers execution (also could be mailbox, events, etc.)
- Each <u>Task</u> has its own stack, which allows them to pause (i.e. block)
- Topology: prologue, loop, epilogue...

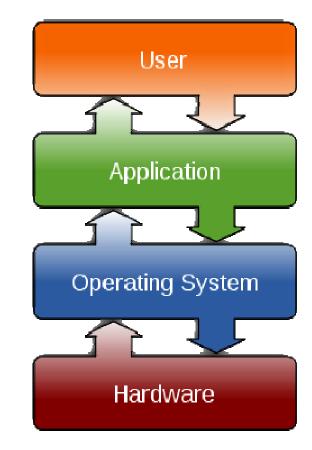
Intro to SYS/BIOS

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Creating a BIOS Thread

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Thread (Object) Creation in BIOS

Users can create threads (BIOS resources or "objects"):

- Statically (via the GUI or .cfg script)
- Dynamically (via C code)
- BIOS doesn't care but you might...

Dynamic (C Code)

Static (GUI or Script) Generic Hardware Interrupt Instance Basic Advanced	<pre>#include <ti hal="" hwi.h="" sysbios=""> Hwi_Params hwiParams; app.c Hwi_Params_init(&hwiParams); hwiParams.eventId = 61; Hwi_create(5, isrAudio, &hwiParams, NULL);</ti></pre>				
Basic Settings Name HWI_INT5 ISR function isrAudio Interrupt Number 5	▼ Interrupt Scheduling Options Interrupts to mask MaskingOption_SELF Priority 5 Event Id 61 ▼ Enabled at startup				
var Hwi = xdc.useModule('ti.sysbios.hal.Hwi'); var hwiParams = new Hwi.Params(); nwiParams.eventId = 61; Hwi.create(5, "&isrAudio", hwiParams);	app.cfg				

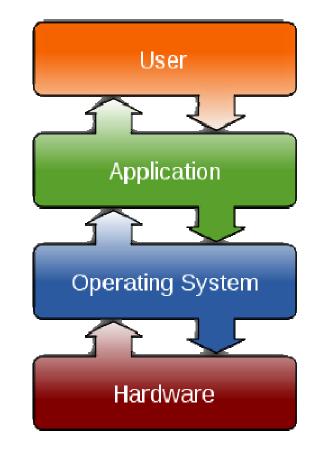
Intro to SYS/BIOS

Overview

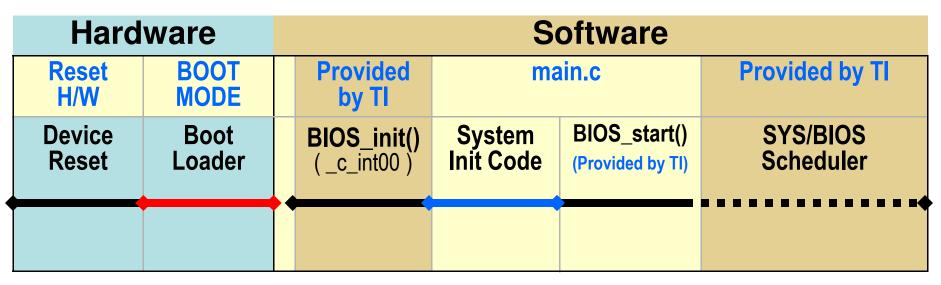
- Threads and Scheduling
- Creating a BIOS Thread

System Timeline

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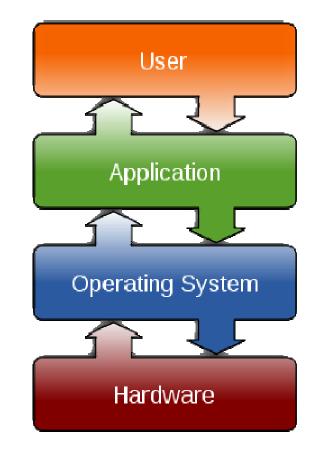
System Timeline



- RESET: Device is reset, then jumps to bootloader or code entry point (c_int00)
- BOOT MODE runs bootloader (if applicable)
- BIOS_init() configures static BIOS objects, jumps to c_int00 to init Stack Pointer (SP), globals/statics, then calls main()
- main()
 - User initialization
 - Must execute BIOS_start() to enable BIOS Scheduler & INTs

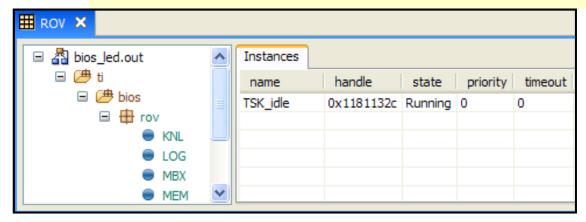
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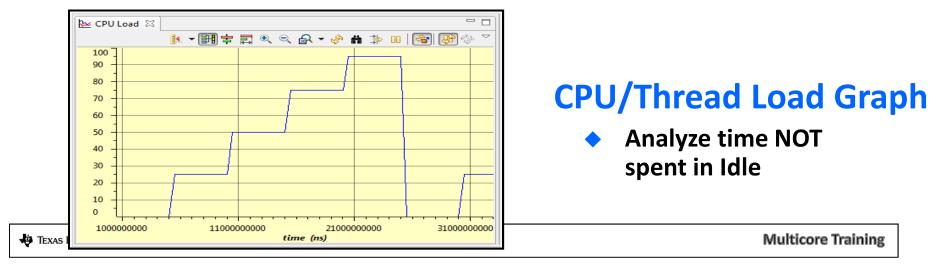
Built-in Real-Time Analysis Tools

- Gather data on target (30-40 CPU cycles)
- Format data on host (1000s of host PC cycles)
- Data gathering does NOT stop target CPU
- Halt CPU to see results (stop-time debug)



RunTime Obj View (ROV)

- Halt to see results
- Displays stats about all threads in system



Built-in Real-Time Analysis Tools

Logs

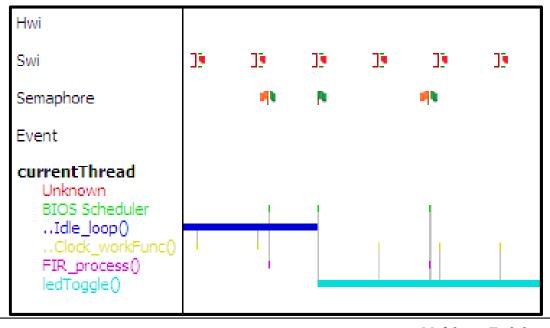
- Send DBG Msgs to PC
- Data displayed during stop-time
- Deterministic, low CPU cycle count
- WAY more efficient than traditional printf()

Execution Graph

- View system events down to the CPU cycle
- Calculate benchmarks

🇮 Raw Logs 🗙			
time	seqID	module	formattedMsg
4,257,279,253	125	Main	"/led.c", line 47: CPU LOAD = [38]
4,257,280,226	126	Main	"/led.c", line 49: TOGGLED LED [42] times
4,357,270,273	127	Main	"/led.c", line 43: BENCHMARK = [3221757] cycles
4,357,271,406	128	Main	"/led.c", line 47: CPU LOAD = [38]
4,357,275,486	129	Main	"/led.c", line 49: TOGGLED LED [43] times
4,457,286,080	130	Main	"/led.c", line_43: BENCHMARK = [3224677] cycles

Log_info1("TOGGLED LED [%u] times", count);

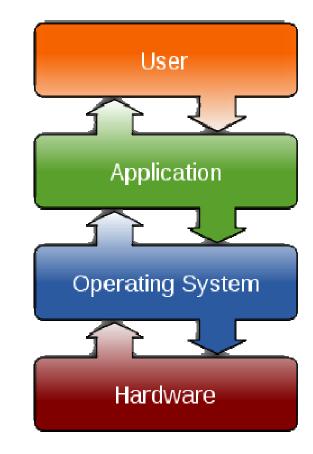


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Multicore Training

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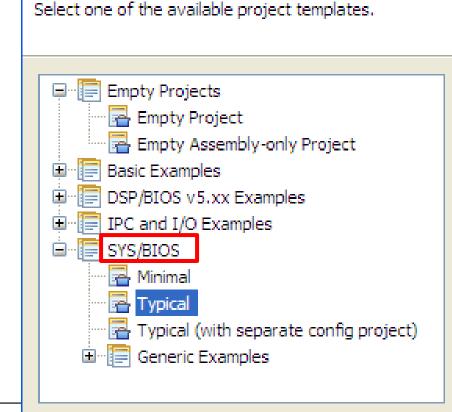


Building a <u>NEW</u> SYS/BIOS Project

- Create CCS Project (as normal), then click:
- Select a SYS/BIOS Example:

Project Templates

New CCS Project



What is in the project created by *Typical*?

Next >

Finish

- Paths to SYS/BIOS tools
- .CFG file (app.cfg) that contains a "typical" configuration for static objects (e.g. Swi, Task).
- Source files (main.c) that contain the appropriate #includes of header files.

SYS/BIOS Project Settings

Select versions for XDC, IPC, SYS/BIOS, xDAIS.

TEXAS INSTRUMENTS

Select the *Platform* (similar to the .tcf seed file for memory).

CCS Build						
Build configuration:	RTSC 🍫 Li	nk Order	●L <mark>I®</mark> Depe	ndencies		
	r-processor Co 1.23.2.27 /BIOS 6.32.2.39	•				
Target: Platform:	ti.targets.C6 ti.platforms.e		$\langle \cdot \rangle$]		
Build-profile:	release				Multicore Tra	ainin

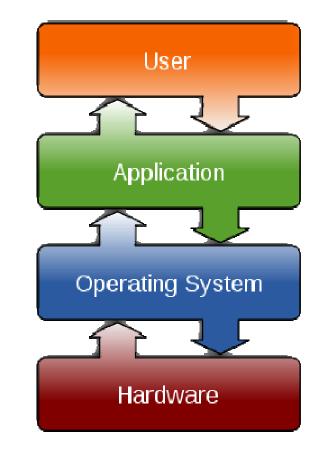
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Static BIOS Configuration

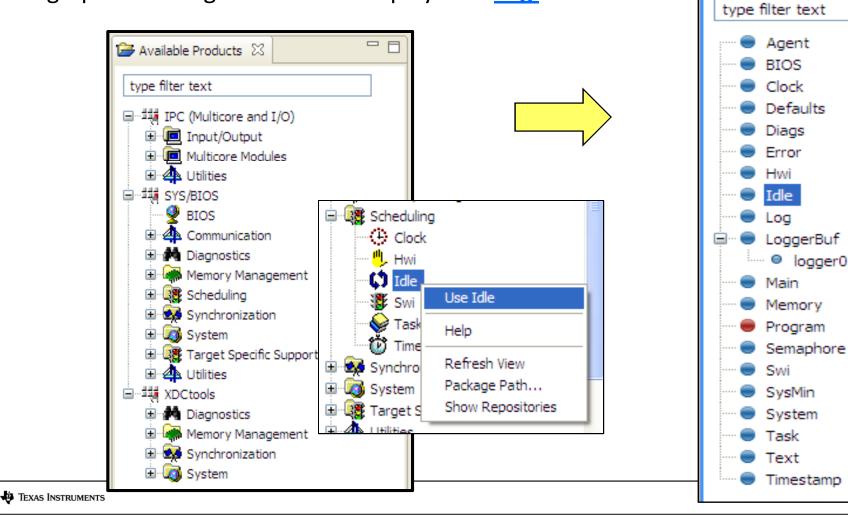
🗄 Outline 🗙

Search

logger0

Users interact with the CFG file via the GUI – XGCONF:

- XGCONF shows Available Products; Right-click and select Use Mod.
- *Mod* shows up in *Outline* view. Right-click and select *Add New*.
- All graphical changes in GUI are displayed in <u>.cfg</u> source code.

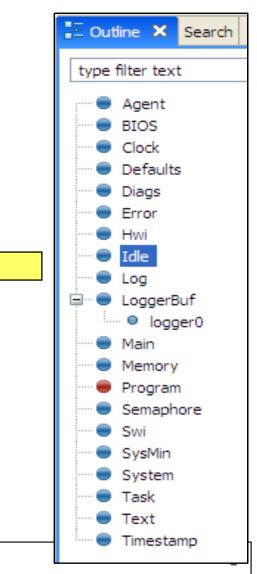


Static Config – .CFG Files

Users interact with the CFG file via the GUI – XGCONF

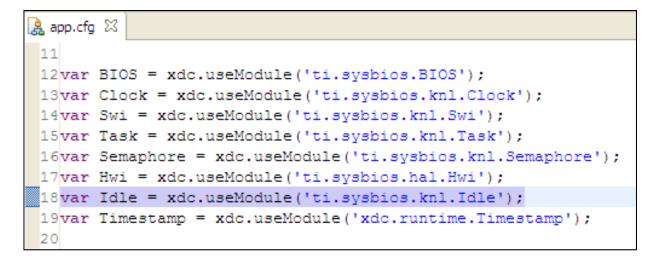
- When you Add New, a dialogue box is provided to set up parameters.
- This window provides two views:
 - Basic
 - Advanced

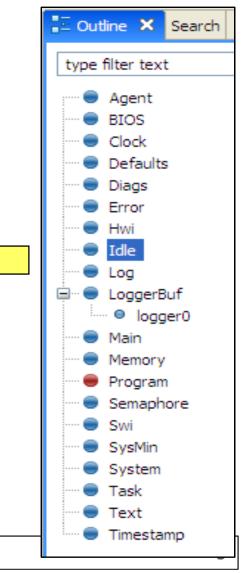
SYS/BIOS Idle - Basic Options
Basic Advanced
Add Idle function management to my configuration
 User Defined Idle Functions
The functions below are added to the list of functions executed whenever there is no not idled.
User idle function 0 ledToggle
User idle function 1 null
User idle function 2 null



.CFG Files (XDC script)

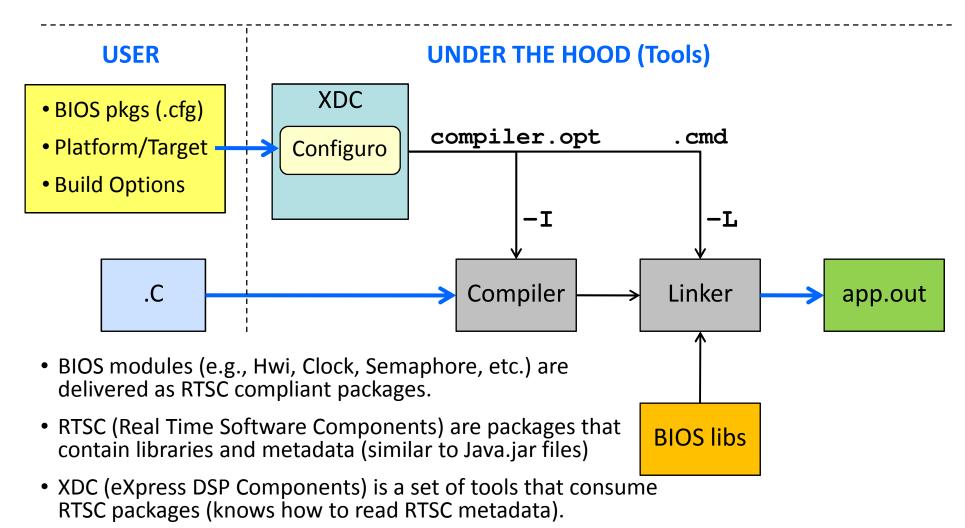
- All changes made to the GUI are reflected with java script in the corresponding .CFG file.
- Click on a module in the Outline view to see the corresponding script in the app.cfg file.





Configuration Build Flow (CFG)

- SYS/BIOS: User configures system with CFG file
- The rest is "under the hood."

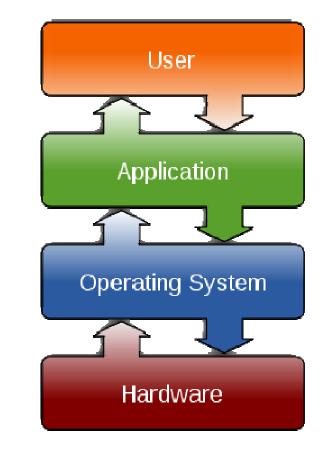


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Platform (Memory Config)

Memory Configuration

- Create Internal Memory Segments (e.g. IRAM)
- Configure cache
- Define External Memory Segments

Section Placement

 Can link code, data, and stack to any defined mem segment

Custom Platform

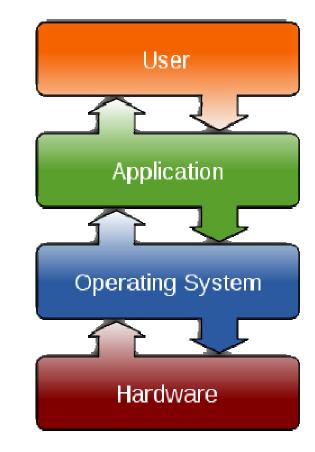
 Use Import button to copy "seed" platform and then customize

		Tools Scripts	Window	Help		
		Port Conne		- 🌾 🦕	• 🔶 •	
		Pin Connect		pp.cfg 🕅		
		RTSC Tool	s 🕨	Path		
Device Details		Profile	•	Platform ▶	Edit/View	
Device Name	TMS320C6748	ROV	L		New	
Device Family	c6000	ROV			TACICOTIC 1	
Clock Speed (MHz)	300.0				Import	
Device Memory						
Name	Base	Ler	ngth	Space	Access	
IRAM	0x11800000		40000	code/data	RWX	
L3_CBA_RAM	0x8000000		20000	code/data	RWX	
IROM	0x11700000		00000	code/data	RX	
L1PSRAM	0x11E00000		00000	code	RWX	
L1DSRAM	0x11F00000) 0x000	00000	data	RW	
L1D Cache: 32k	✓ L1	1P Cache: 32k		🖌 L2 Cache: 🛛	Dk 🗸	
Customize Memo	ry					
External Memory						
Name	Base	Ler	ngth	Space	Access	
DDR	0xC000000	0 0x080	00000	code/data	RWX	
Memory Sections -						
Code Memory: IRA	M 🔽 Di	ata Memory: IR	AM	Stack Memor	ry: IRAM 🔽	

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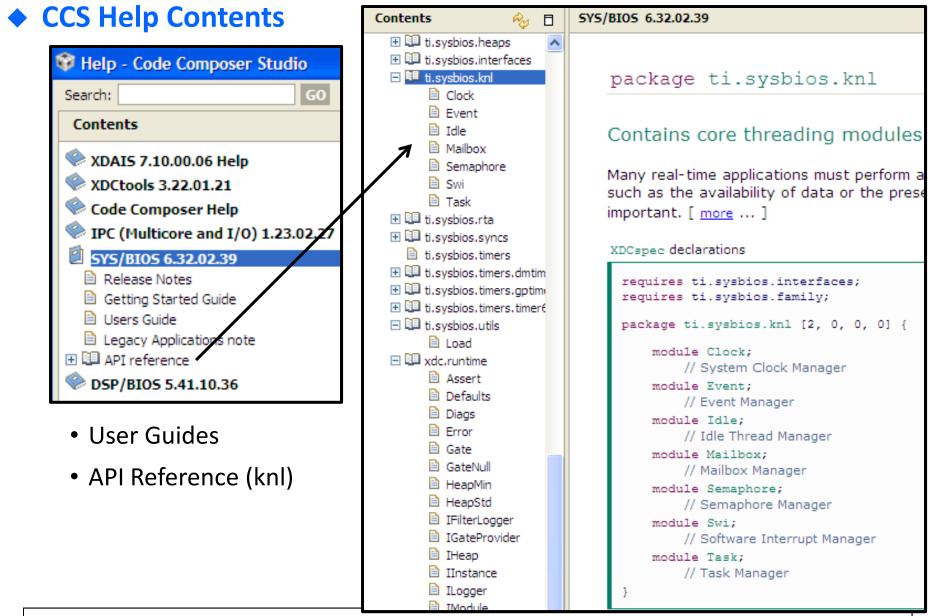
For More Information (1)

SYS/BIOS Product Page http://www.ti.com/sysbios

SYS/BIOS Real-Time Operating System (RTOS) Status : ACTIVE SYSBIOS								
Description/Features	Technical Documents	Support & C	ommunity					
Order Now								
Part Number		Texas Instruments	Status F					
SYSBIOS6: SYS/BIOS 6.x Real-Time Operating	Get Software	ACTIVE F						
Description								
Advanced RTOS Solution								
SYS/BIOS [™] 6.x is an advanced, real-time operating system for use in a wide range of DSPs, ARMs, and microcontrollers. It is designed for use in embedded applications that need real-time scheduling, synchronization, and instrumentation. It provides preemptive multitasking, hardware abstraction, and memory management. Compared to its predecessor, DSP/BIOS [™] 5.x, it has numerous enhancements in functionality and performance.								

TEXAS INSTRUMENTS

For More Information (2)



TEXAS INSTRUMENTS

Multicore Training

Download Latest Tools

Download Target Content

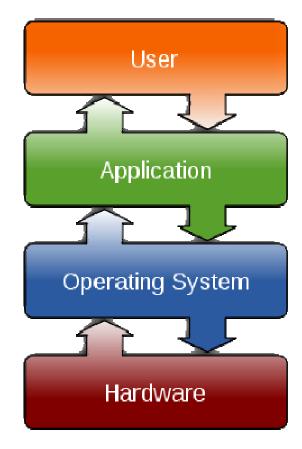
http://software-dl.ti.com/dsps/dsps_public_sw/sdo_sb/targetcontent/

Target Content Infrastructure Product Downloads	
BIOS Platform Support Packages	
DSP/BIOS and SYS/BIOS	DSP/BIOS
DSP/BIOS BIOSUSB Product	SYS/BIOS
DSP/BIOS Utilities	Utilities
Digital Video Sotware Development Kits (DVSDK)	SysLink
DSP Link and SysLink	DSP Link
• SysLink (BIOS 6)	IPC
• DSP Link (BIOS 5)	♦ Etc.
Graphics SDK	
EDMA3 Low-level Driver	
Interprocessor Communication (IPC)	
	Γ.Λ. εl÷

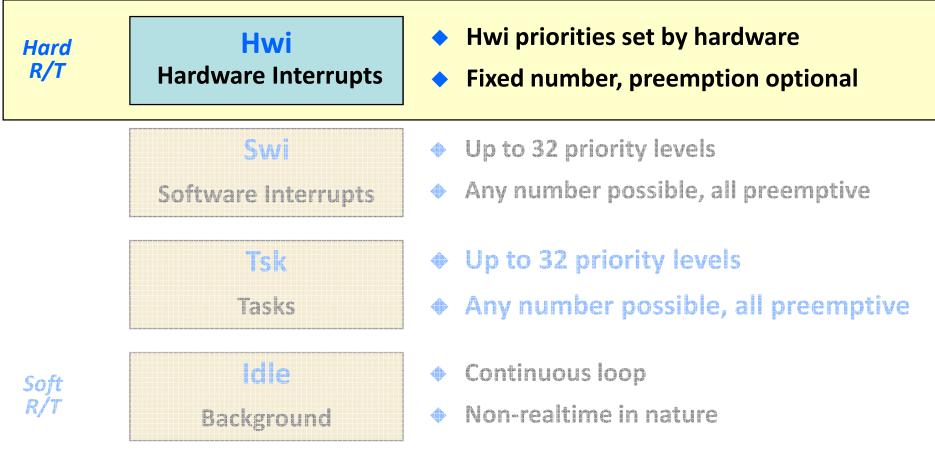
- Intro to SYS/BIOS
- BIOS Threads

Hardware Interrupts (Hwi)

- Software Interrupts (Swi)
- Tasks (Tsk)
- Semaphores (Sem)

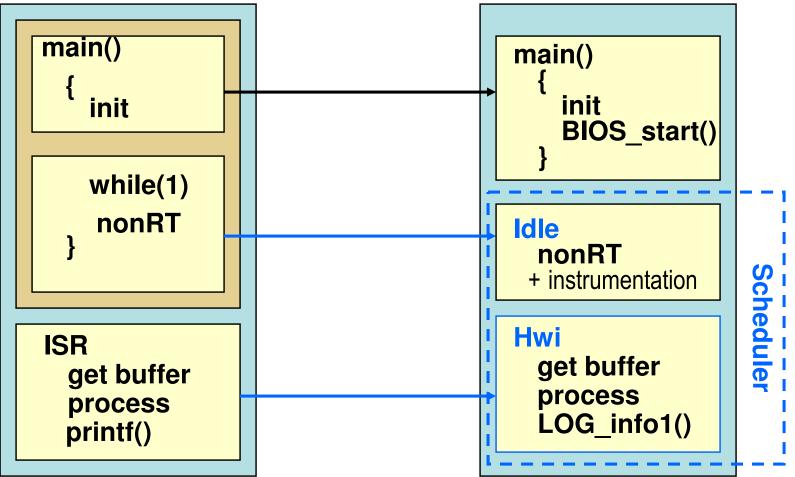


Hwi Scheduling



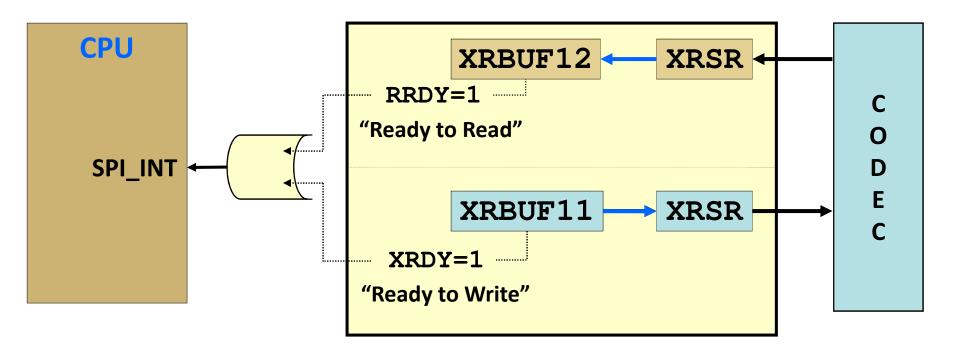
- ◆ Idle events run in sequence when no Hwi are posted.
- Hwi is ISR with automatic vector table generation + context save/restore.
- Any Hwi preempts Idle, Hwi may preempt other Hwi if desired.

Foreground / Background Scheduling



- ◆ Idle events run in sequence when no Hwi are posted.
- Hwi is ISR with automatic vector table generation + context save/restore.
- Any Hwi preempts Idle, Hwi may preempt other Hwi if desired.

CPU Interrupts from Peripheral (SPI)



 A peripheral (e.g., SPI on C6678) causes an interrupt to the CPU to indicate "service required."

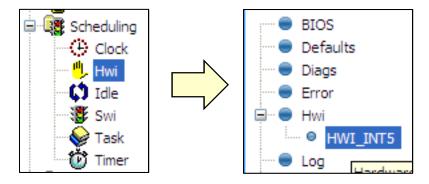
 This "event" will have an ID (datasheet) and can be tied to a specific CPU interrupt (target specific).

> How do we configure SYS/BIOS to respond to this interrupt and call the appropriate ISR?

Configuring an Hwi: Statically via GUI

Example: Tie SPI_INT to the CPU HWI₅

Use Hwi module (Available Products), insert new Hwi (Outline View)



NOTE: BIOS objects can be created via the GUI, script code, or C code (dynamic).

Configure Hwi: Event ID, CPU Int #, ISR vector:

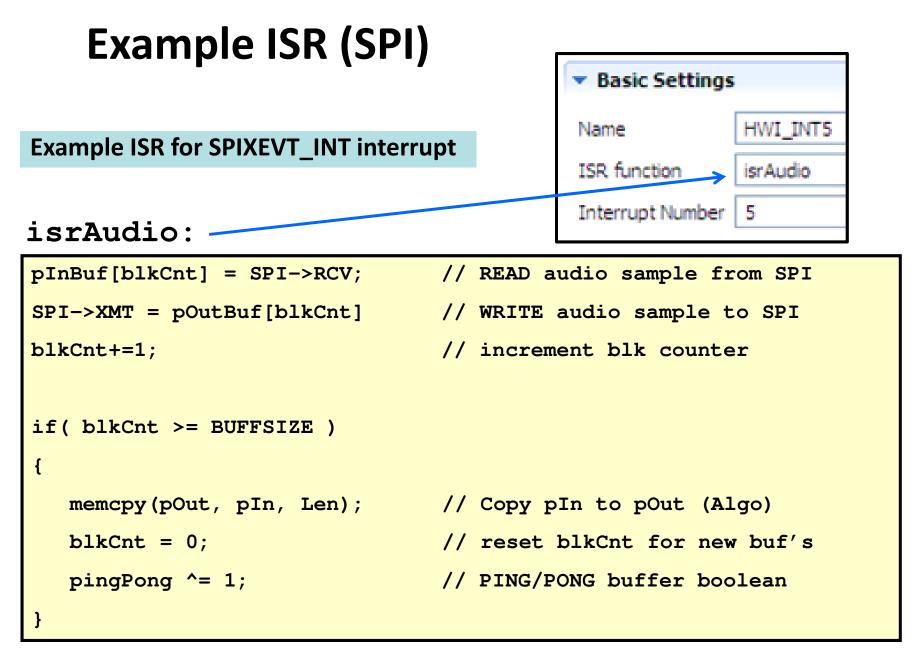
Basic Setting	5	•	Interrupt Sche	duling Options
Name	HWI_INT5		Interrupts to mask	MaskingOption_SELF
ISR function	isrAudio		Priority	5
Interrupt Number	5		Event Id	61

Hardware Event IDs

How do you know the names of the interrupt events and their corresponding event numbers?

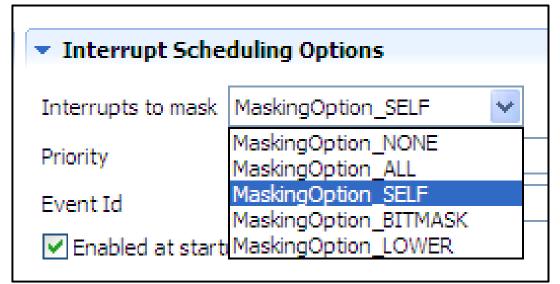
Look it up in the datasheet. *Source: TMS320C6678 datasheet* PCIEXpress_Legacy_INTC Legacy interrupt mode 52 PCIEXpress_Legacy_INTD Legacy interrupt mode 53 54 SPIINTO SPI interrupt0 SPI interrupt1 55 SPIINT1 56 SPIXEVT Transmit event X 57 SPIRE! 😯 Create new Hwi Params I2CIN 58 Value Name Summary hwi0 Name of the instance name ⊿ Create Args intNum null interrupt number Create Args pointer to ISR function hwiFxn null ⊿ Parana maskSetting MaskingOption_SELF maskSetting. Default is Hwi_MaskingOption_SELF 0 ISR function argument. Default is 0 arg enableInt true Enable this interrupt now? Default is true 56 Interrupt event ID (Interrupt Selection Number) eventId priority 5 Interrupt priority ? 0K Cancel

As appropriate, refer to the datasheet for your target platform.



Can one interrupt preempt another?

Enabling Preemption of Hwi



- Default mask is SELF, which means all other Hwi activities can pre-empt except for itself.
- Can choose other masking options as required:

ALL:	Best choice if ISR is short & fast
NONE:	Dangerous; Make sure ISR code is re-entrant.
BITMASK:	Allows custom mask
LOWER:	Masks any interrupt(s) with lower priority (ARM)

SYS/BIOS Hwi APIs

Other useful Hwi APIs:

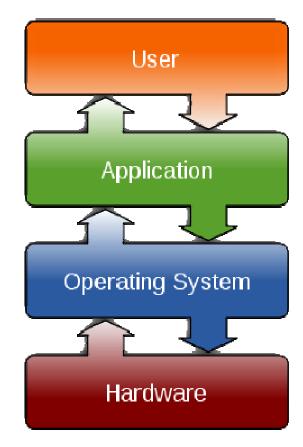
Hwi_disableInterrupt()	Set enable bit = 0
Hwi_enableInterrupt()	Set enable bit = 1
Hwi_clearInterrupt()	Clear INT flag bit = 0
Hwi_post() New in SYS/BIOS	Post INT # (in code)
Hwi_disable()	Global INTs disable
Hwi_enable()	Global INTs enable
Hwi_restore()	Global INTs restore

Outline

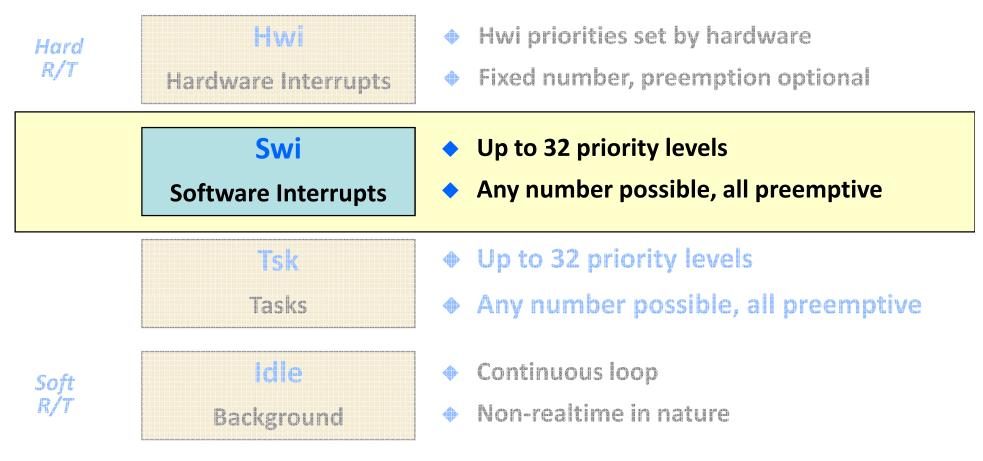
- Intro to SYS/BIOS
- BIOS Threads
 - Hardware Interrupts (Hwi)

Software Interrupts (Swi)

- Tasks (Tsk)
- Semaphores (Sem)



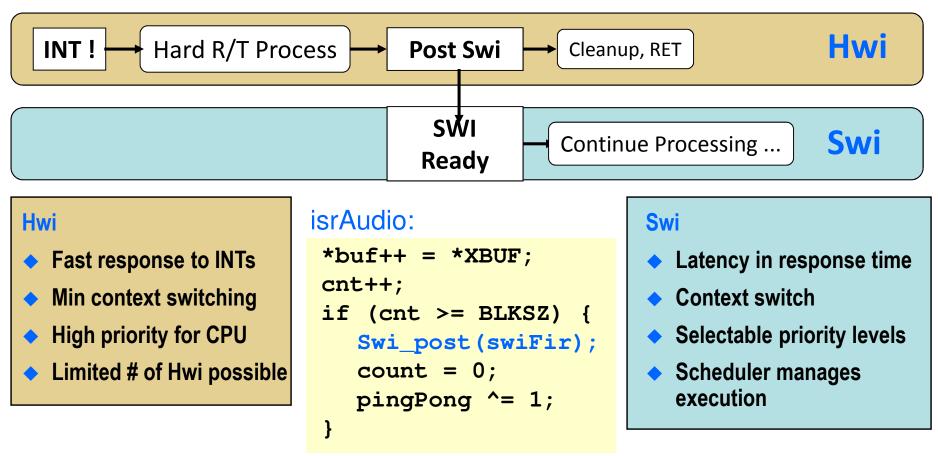
Swi Scheduling



SYS/BIOS provides for Hwi and Swi management.
SYS/BIOS allows the Hwi to post a Swi to the ready queue.

Hardware and Software Interrupt System

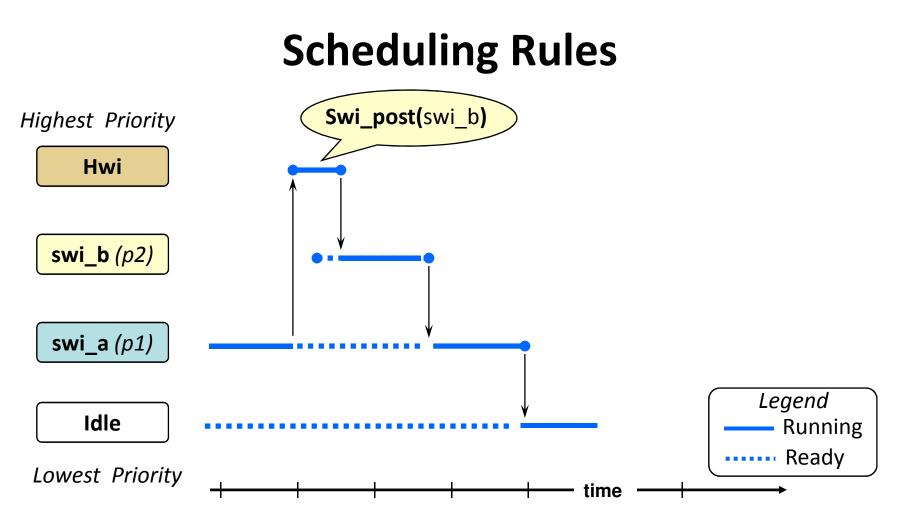
Execution flow for flexible real-time systems:



◆ SYS/BIOS provides for Hwi and Swi management.

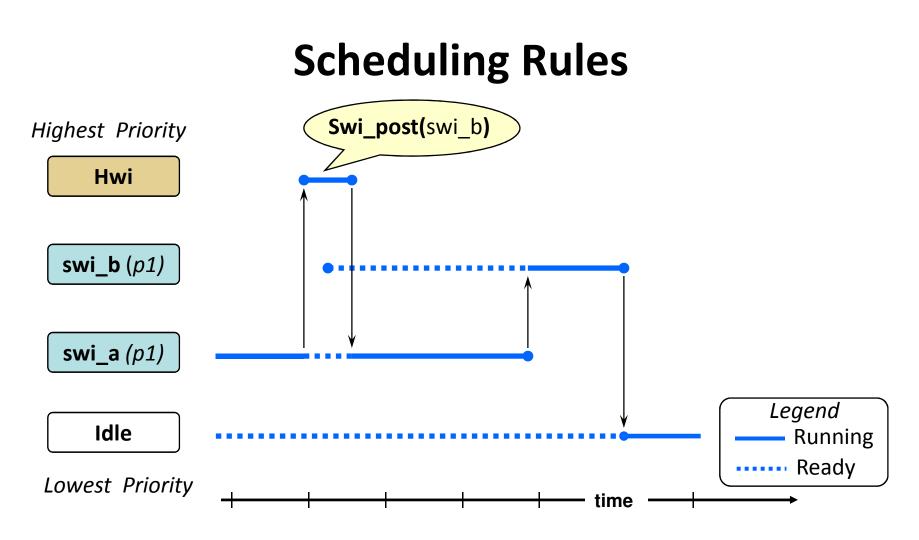
◆ SYS/BIOS allows the Hwi to post a Swi to the ready queue.

TEXAS INSTRUMENTS



- Swi_post(mySwi) : Unconditionally post a software interrupt (in the ready state).
- If a higher priority thread becomes ready, the running thread is preempted.
- Swi priorities range from 1 to 32.
- Automatic context switch (uses system stack)

What if more than one Swi process is set to the same priority?

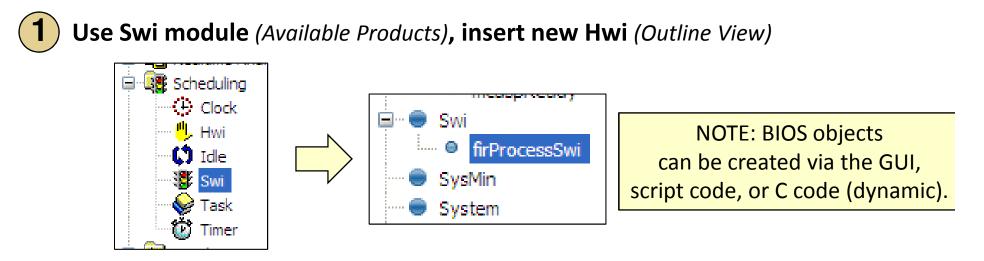


Processes of same priority are scheduled first-in first-out (FIFO).

 Having threads at the SAME priority offers certain advantages, such as resource sharing (without conflicts).

Configuring a Swi: Statically via GUI

Example: Tie isrAudio() fxn to Swi; Use priority 1



) Configure Swi – Object name, function, priority:

2

	🤱 *app.cfg	×
	A Software Interrupt Instance	
	Basic Advanced	
	 Thread Settings 	
	Name	firProcessSwi
	Function	FIR_process
🔹 Texas Instruments	Priority	1

Multicore Training

SYS/BIOS Swi APIs

Other useful Swi APIs:

Swi_inc()	Post, increment count
Swi_dec()	Decrement count, post if 0
Swi_or()	Post, OR bit (signature)
Swi_andn()	ANDn bit, post if all posted
Swi_getPri()	Get any Swi Priority
Swi_enable	Global Swi enable
Swi_disable()	Global Swi disable
Swi_restore()	Global Swi restore

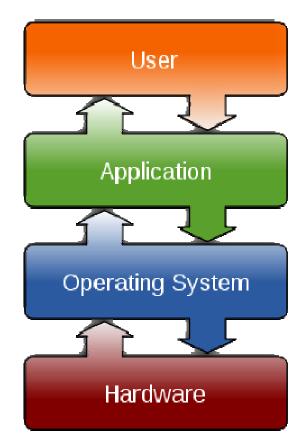
Outline

Intro to SYS/BIOS

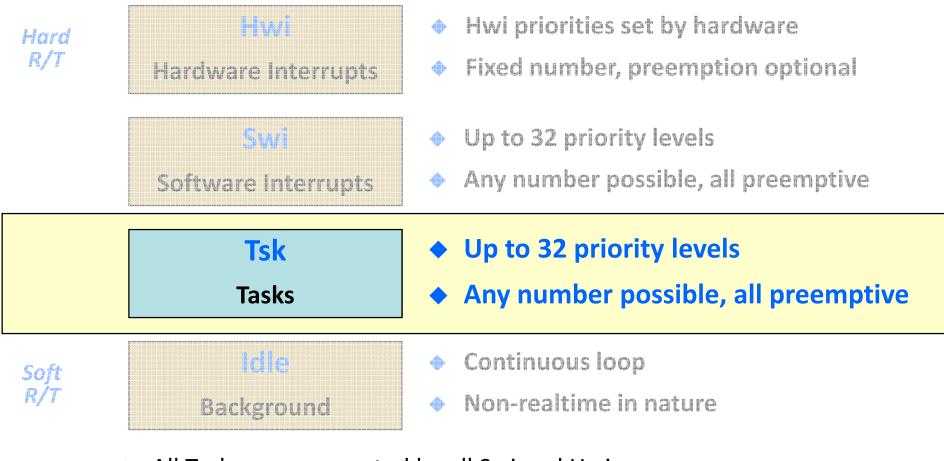
- BIOS Threads
 - Hardware Interrupts (Hwi)
 - Software Interrupts (Swi)

Tasks (Tsk)

Semaphores (Sem)

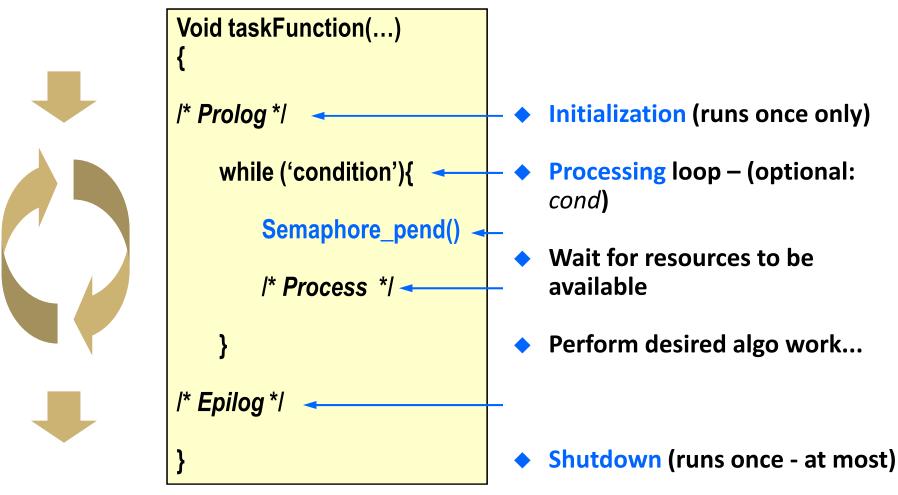


Task Scheduling



- All Tasks are preempted by all Swi and Hwi.
- All Swi are preempted by all Hwi.
- Preemption amongst Hwi is determined by user.
- In absence of Hwi, Swi, and Tsk, Idle functions run in loop.

Task Code Topology – Pending



- Task can encompass *three* phases of activity.
- Semaphore can be used to signal resource availability to Task.
- Semaphore_pend() blocks Task until semaphore (flag) is posted.

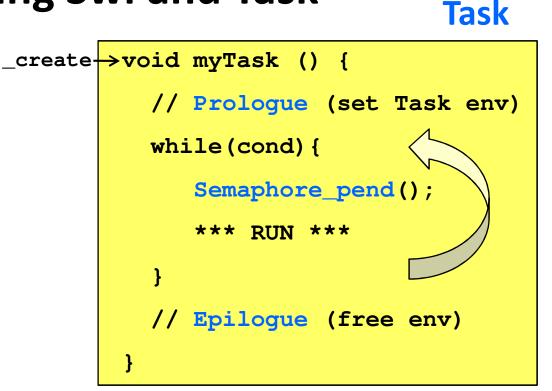
Comparing Swi and Task

_post \rightarrow	<pre>void mySwi () {</pre>		
	// set local env		
	*** RUN ***		
\checkmark	,		
	}		

• "Ready" when <u>POSTED</u>

Swi

- Initial state NOT preserved; Must set each time Swi is run
- CanNOT block (runs to completion)
- Context switch speed (~140c)
- All Swi share system stack w/ Hwi
- Usage: As follow-up to Hwi and/or when memory size is an absolute premium



- "Ready" when <u>CREATED</u> (BIOS_start or dynamic)
- P-L-E structure handy for resource creation (P) and deletion (E), initial state preserved
- Can block/suspend on semaphore (flag)
- Context switch speed (~160c)
- Uses its <u>OWN stack</u> to store context
- Usage: Full-featured sys, CPU w/more speed/mem

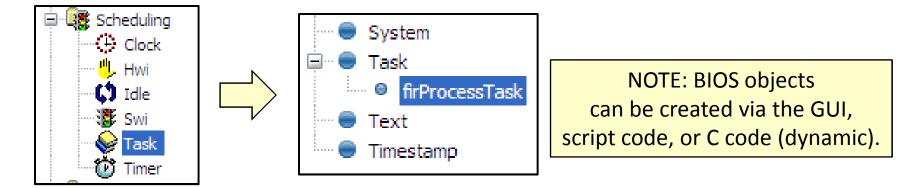


Configuring a Task: Statically via the GUI

Example:

Create firProcessTask, tie to FIR_process(), priority 2

Use Task module (Available Products) **, insert new Task** (Outline View)



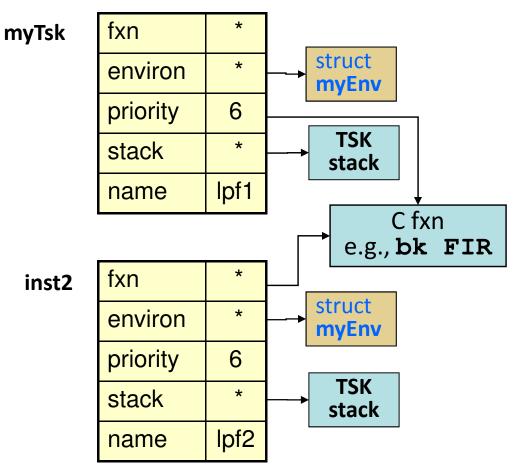
Configure Task: Object name, function, priority, stack size

	▼ Threa	d Settings	
	Name	firProcessTask	
	Function	FIR_process	
	Priority	2	
	Use the v V Task is	ital flag to prevent system exit until thi s vital	
	 Stack 	Control Options	
TEXAS INSTRUMENTS	Stack size	2048	Multicore Training

Task Object Concepts

Task object:

- Pointer to task function
- Priority: changable
- Pointer to task's stack
 - Stores local variables
 - Nested function calls
 - makes blocking possible
 - Interrupts run on the system stack
- Pointer to text name of TSK
- Environment: pointer to user defined structure:



Task_setenv(Task_self(),&myEnv);

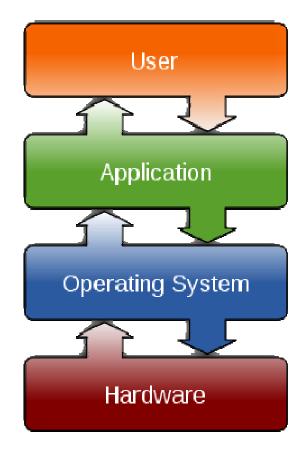
hMyEnv = Task_getenv(&myTsk);

Outline

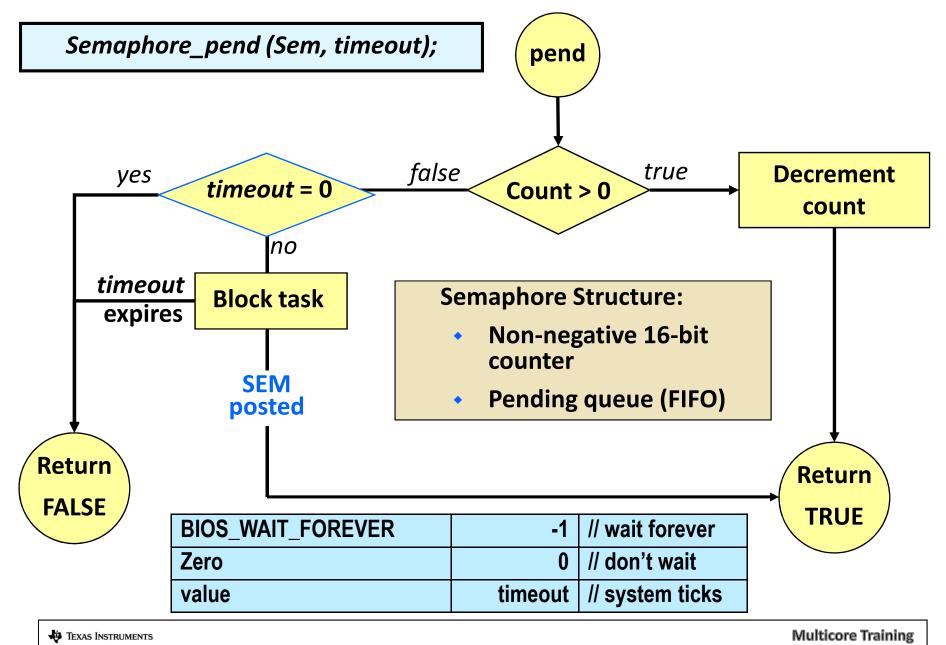
Intro to SYS/BIOS

- BIOS Threads
 - Hardware Interrupts (Hwi)
 - Software Interrupts (Swi)
 - Tasks (Tsk)

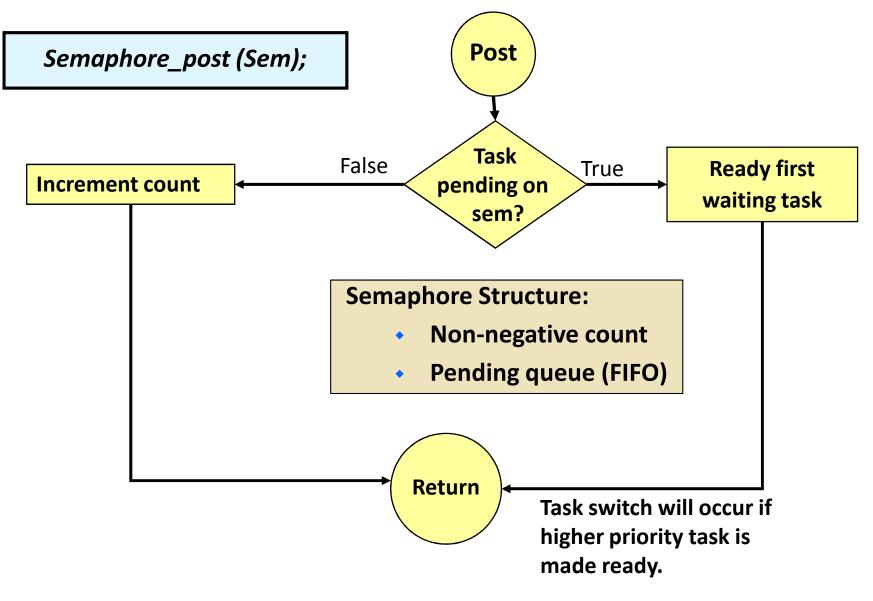
Semaphores (Sem)



Semaphore Pend



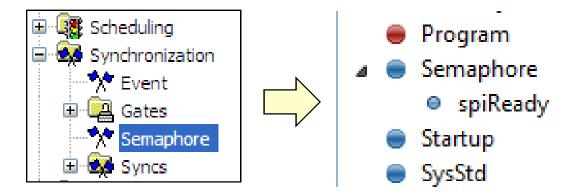
Semaphore Post



Configuring a Semaphore: Statically via GUI

Example: Create *spiReady*, counting

Use Semaphore (Available Products), insert new Semaphore (Outline View)



2 Configure Semaphore: Object name, initial count, type

A Semaphore	A Semaphore Instance - Basic Options		
Basic Advanced			
▼ Required Setti	▼ Required Settings		
Name	spiReady		
Initial count	0		
Semaphore type	 Counting semaphore Binary Semaphore 		

SYS/BIOS Semaphore/Task APIs

Other useful Semaphore APIs:

Semaphore_getCount()	Get semaphore count
----------------------	---------------------

Other useful Task APIs:

Task_sleep()	Sleep for N system ticks
Task_yield()	Yield to same pri Task
Task_setPri()	Set Task priority
Task_getPri()	Get Task priority
Task_get/setEnv()	Get/set Task Env
Task_enable()	Enable Task Mgr
Task_disable()	Disable Task Mgr
Task_restore()	Restore Task Mgr

TEXAS INSTRUMENTS

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Questions?

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