Key Points to Setting up SYNC & SYSREF on LMK0482x with CodeLoader

2014-04-22

Overview

- SYNC and SYSREF on the LMK0482x share the same internal path.
  - We refer to this signal/path as SYNC when resetting the internal dividers on LMK0482x
  - We refer to this signal/path as SYSREF when providing a SYSREF for target JESD204B devices.
- Since it is required to SYNC Device Clock and SYSREF Divider before enabling SYSREF, it is not possible to achieve JESD204B operation with a single programming of the registers. Instead divides must first be synchronized, and then SYSREF functionality can be enabled. The following slides illustrate the procedure.

1. Setup Clock Outputs
2. Power up SYSREF and prepare SYNC path to Dividers
3. Reset SYSREF after SYSREF powered up.
4. SYNC Dividers
5. Disable SYNC/SYSREF Path from Resetting Dividers
6. Set Desired SYSREF Generation Mode

   a) Continuous b) Pulsed c) SYSREF Request

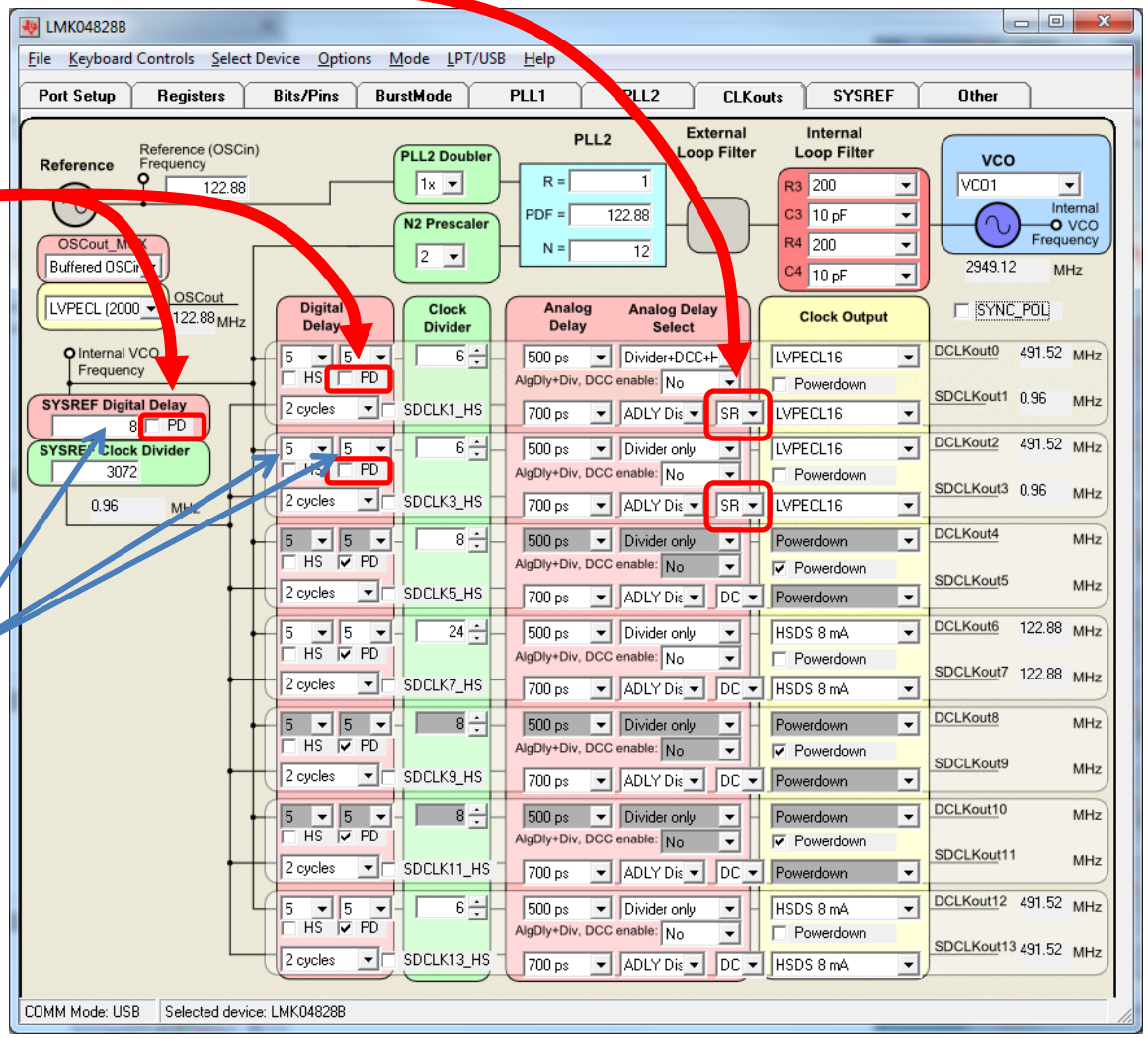
1) Setup Clock Outputs

Set SDCLKoutY_MUX = SR
Select SYSREF source for SDCLKoutY.

Set DCLKoutX_DDLY_PD = 0 &
SYSREF_DDLY_PD = 0

The digital delay can be adjusted on Device Clocks & SYSREF to achieve desired phase relationship between device clocks and to set a ‘global’ digital delay for SYSREF with respect to Device Clocks when the divider reset.

Half step digital delay always takes effect immediately upon change.



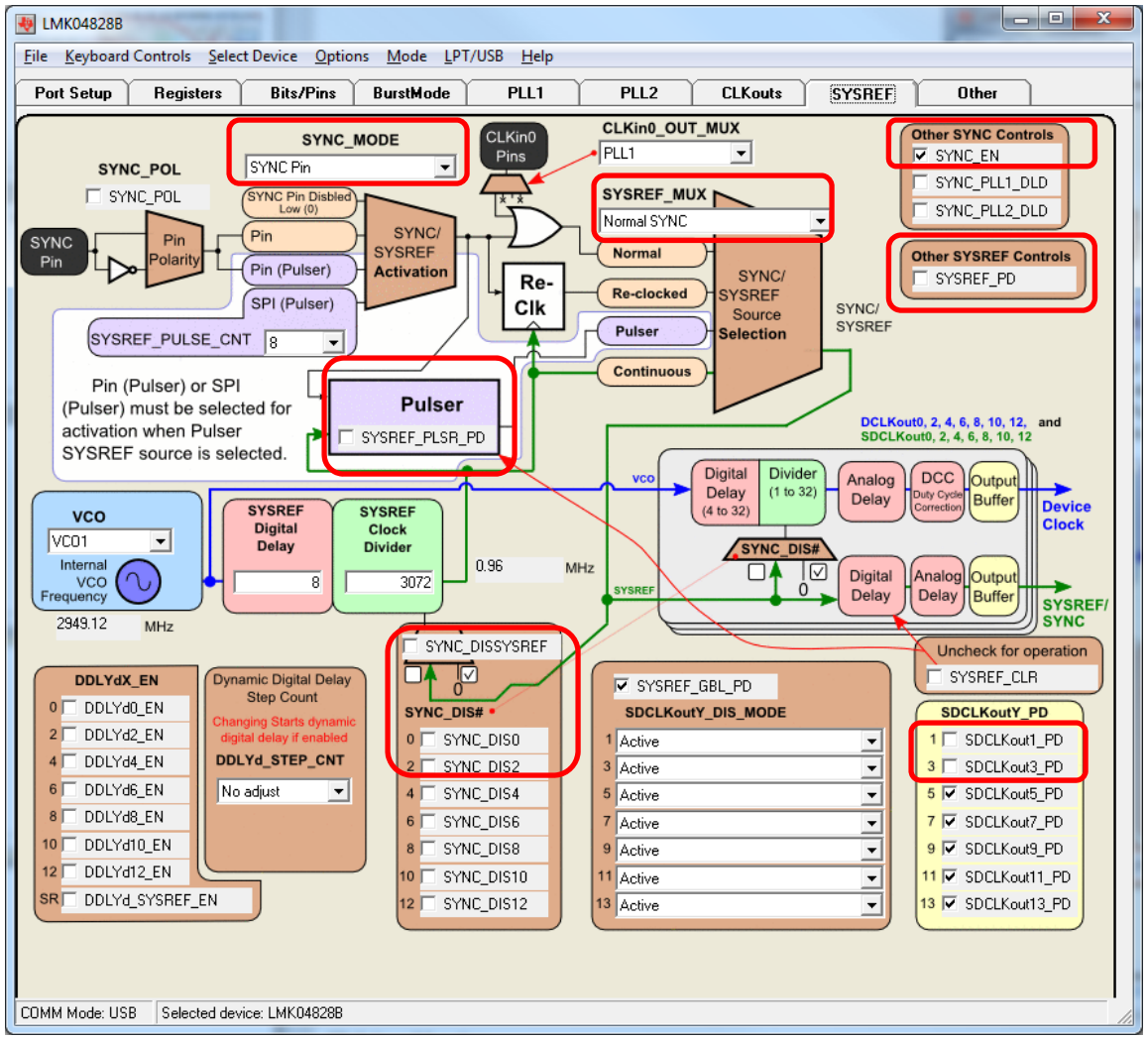
2) Power up SYSREF and prepare SYNC path to Dividers

These bits enable SYNC/SYSREF and prepare device for synchronizing dividers

SYNC_EN = 1
SYSREF_PD = 0
SYSREF_PLSR_PD = 0
    If SYSREF pulser will be used
SYNC_DISSYSREF = 0
SYNC_DISX = 0
SDCLKoutY_PD = 0

This bits setup how SYNC will be generated

SYNC_MODE = Sync Pin
SYSREF_MUX = Normal
                SYNC

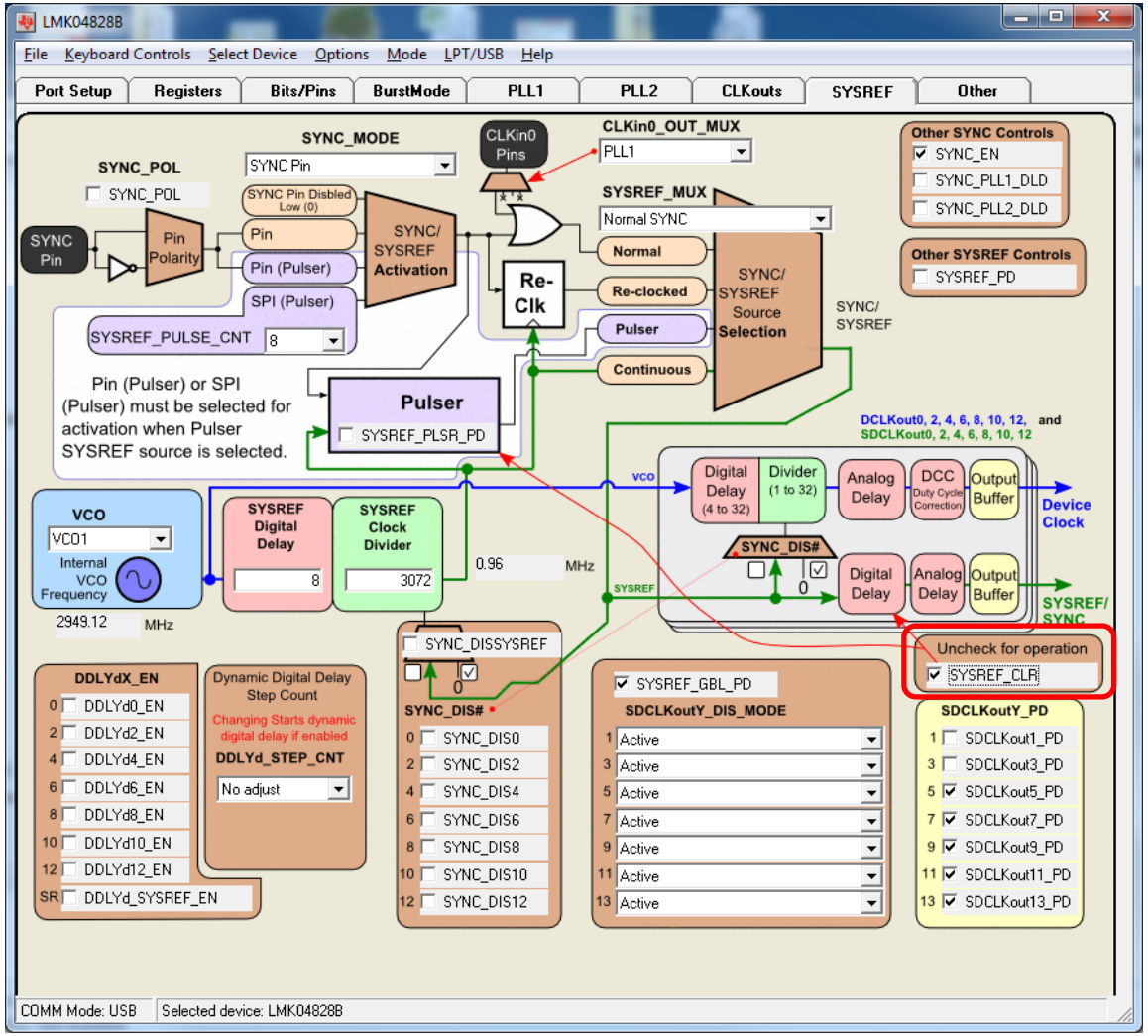


3) Reset SYSREF

After SYSREF is powered up, to ensure proper operation of pulser block and prevent possibility of glitch pulses from SYSREF output,

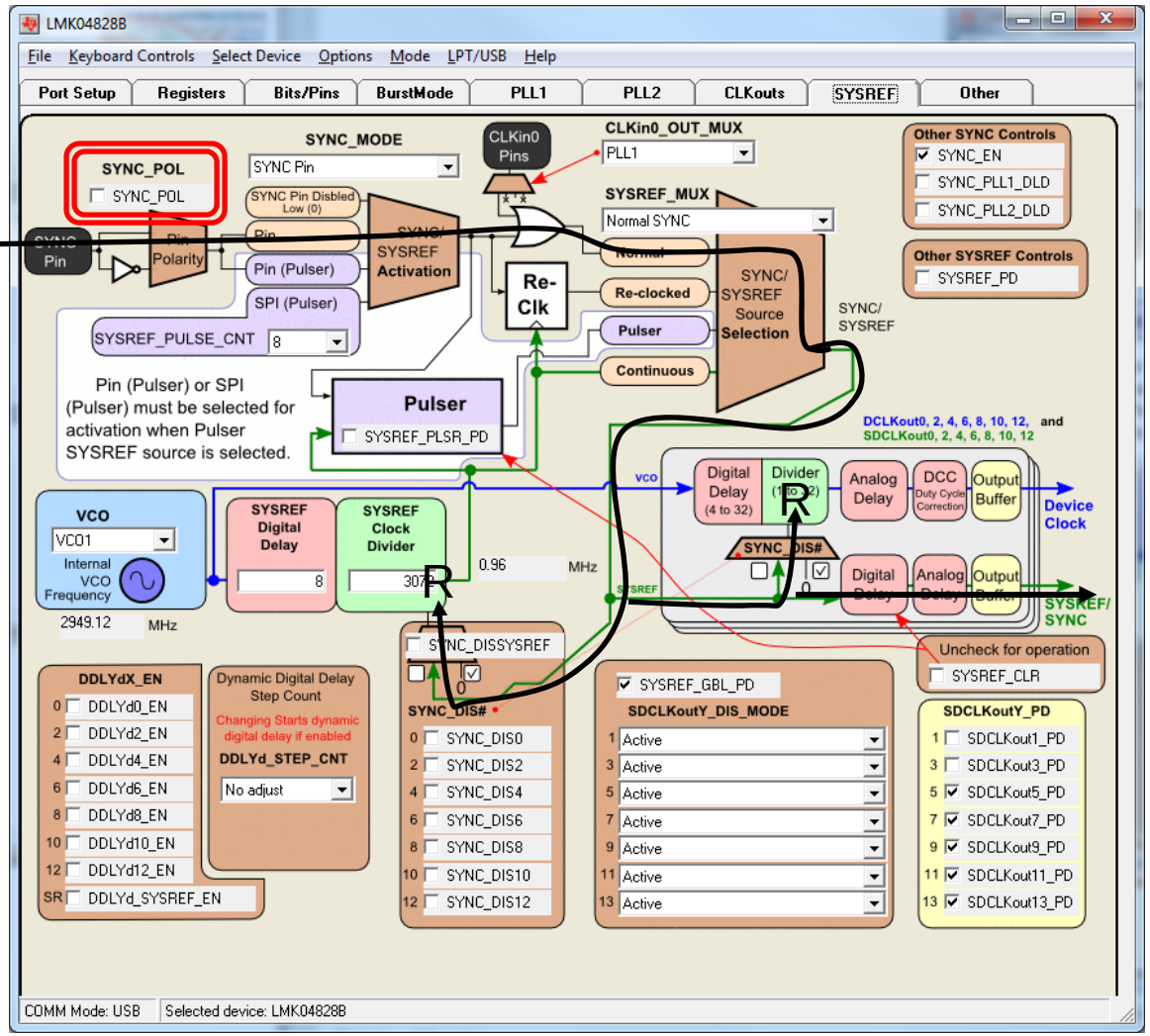
Set SYSREF_CLR = 1 for 15 or more VCO clock cycles.

It is necessary to set SYSREF_CLR = 0 for SYSREF output. Otherwise SYSREF is held in reset.



4) SYNC Dividers

Toggle SYNC **Pin** or **SYNC_POL bit** to generate a SYNC which will reset SYSREF and Device Clock Dividers

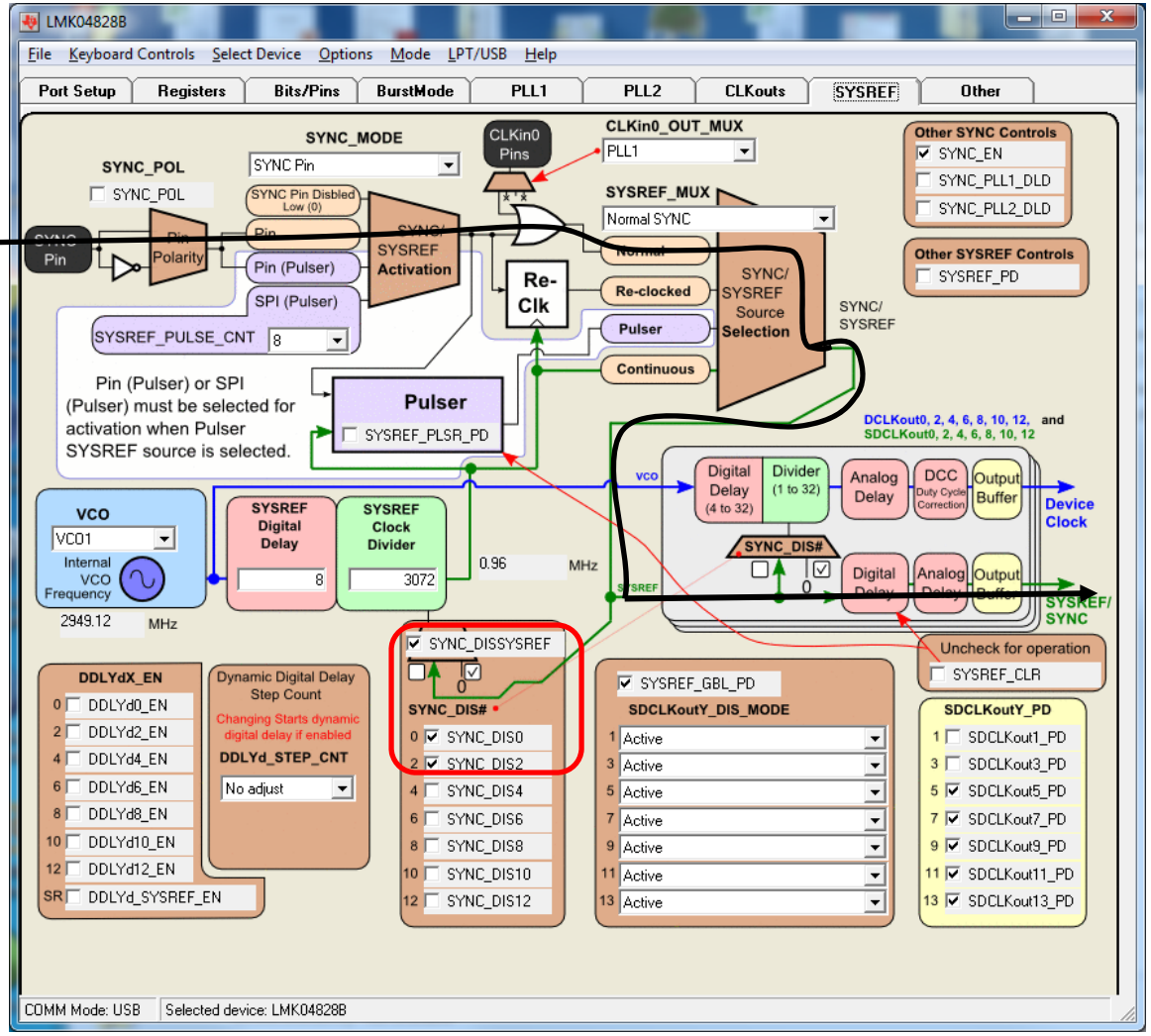


5) Disable SYNC/SYSREF Path from Resetting Dividers

Very important. **Before** enabling SYSREF **disable divider reset**.

Since SYSREF travels on the same bus which SYNC does to reset dividers then the SYSREF signal will reset the clock out divider or the SYSREF divider – which may be the source for the SYSREF signal itself!

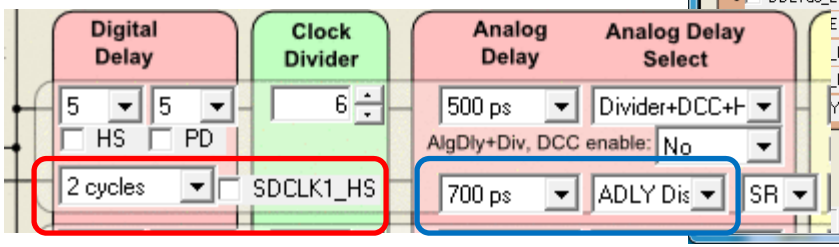
Once this is done desired SYSREF mode may be setup. → See next 3 slides.

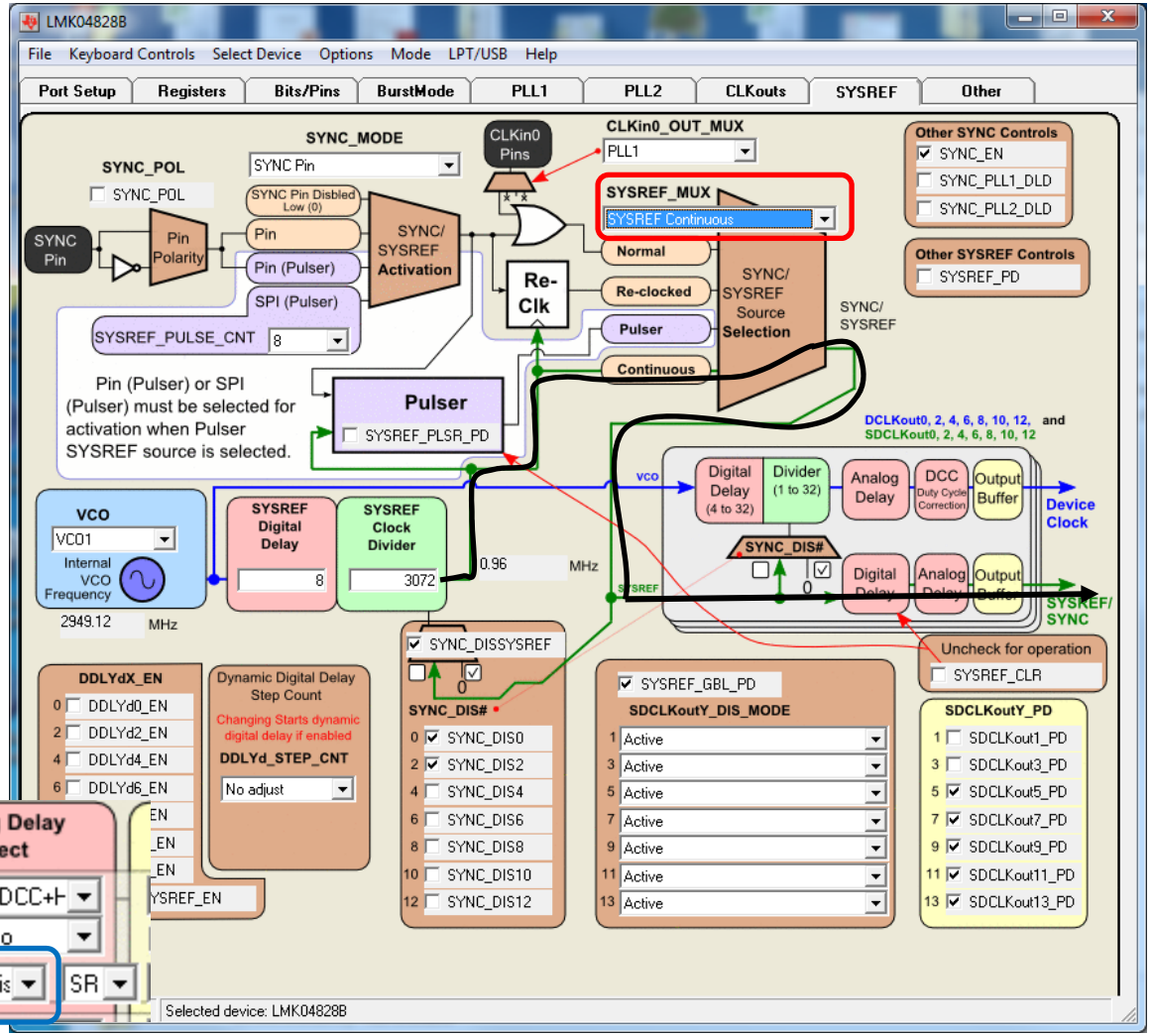


6a) Set Desired SYSREF Generation Mode - Continuous

While not recommended for normal operation because of crosstalk. This mode is excellent for adjusting timing of SYSREF to device clock setup time.

To adjust use the bits circled in red below: **SDCLKoutY_DDLY** and **SDCLKoutY_HS**. Changes to these registers to effect immediately.





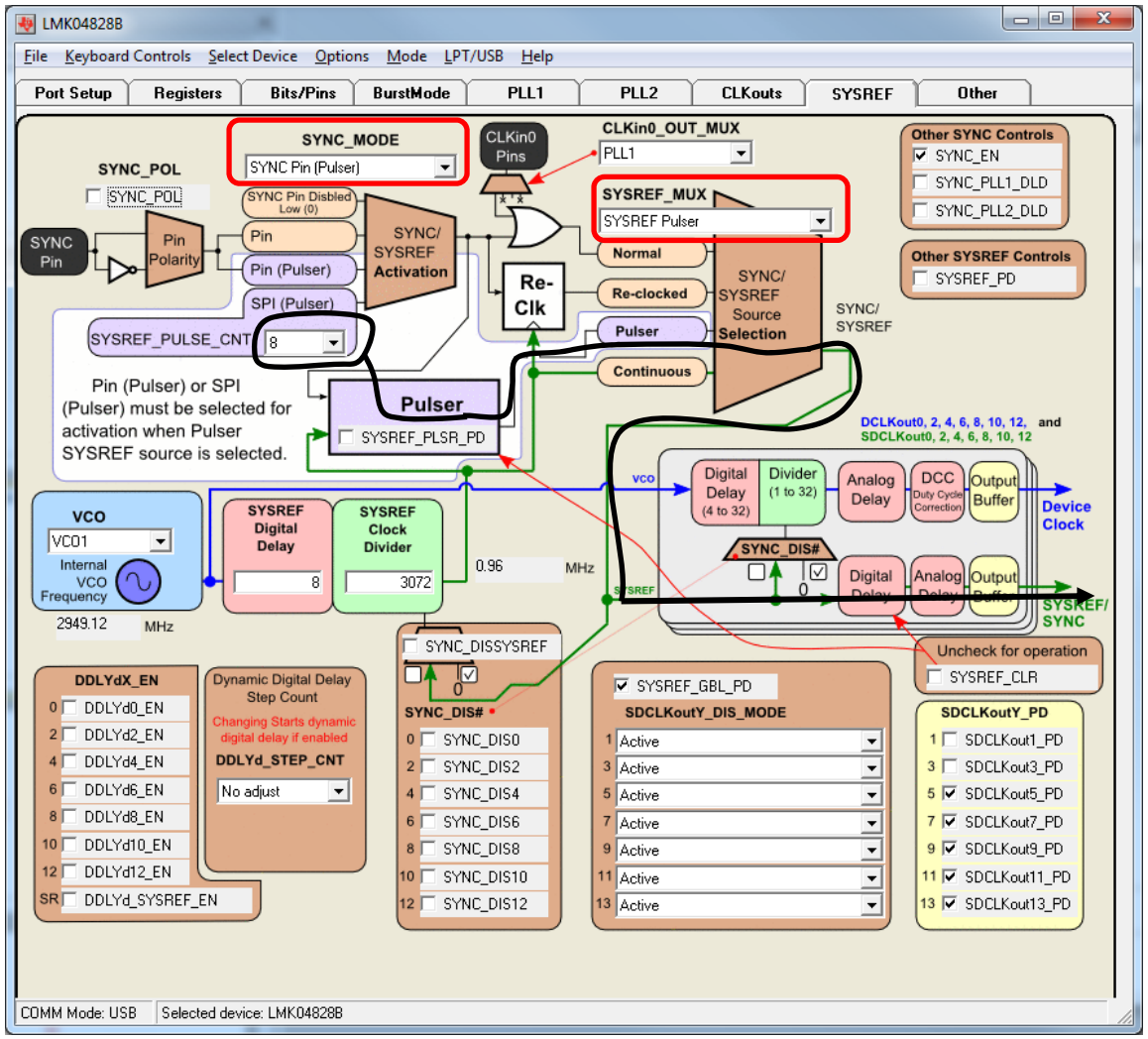
Analog delay (blue box) has +/- 30% variation over PVT. It is best to use analog delay only with slower device clock frequencies.

6b) Set Desired SYSREF Generation Mode - Pulsed

Once proper settings for SYSREF digital delay have been achieved, pulser mode allows the LMK0482x to send a programmable number SYSREF pulses upon pin or SPI request.

Note, even when programmed for SYNC_MODE = Pin (Pulser), it is possible to generate SYSREF pulses via SPI programming by toggling SYNC_POL bit.

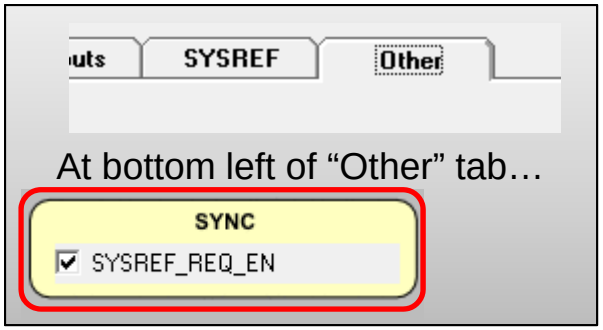
For SPI SYSREF generation, it is more efficient to set SYNC_MODE = SPI (Pulser) and then program the SYSREF_PULSE_CNT register once.

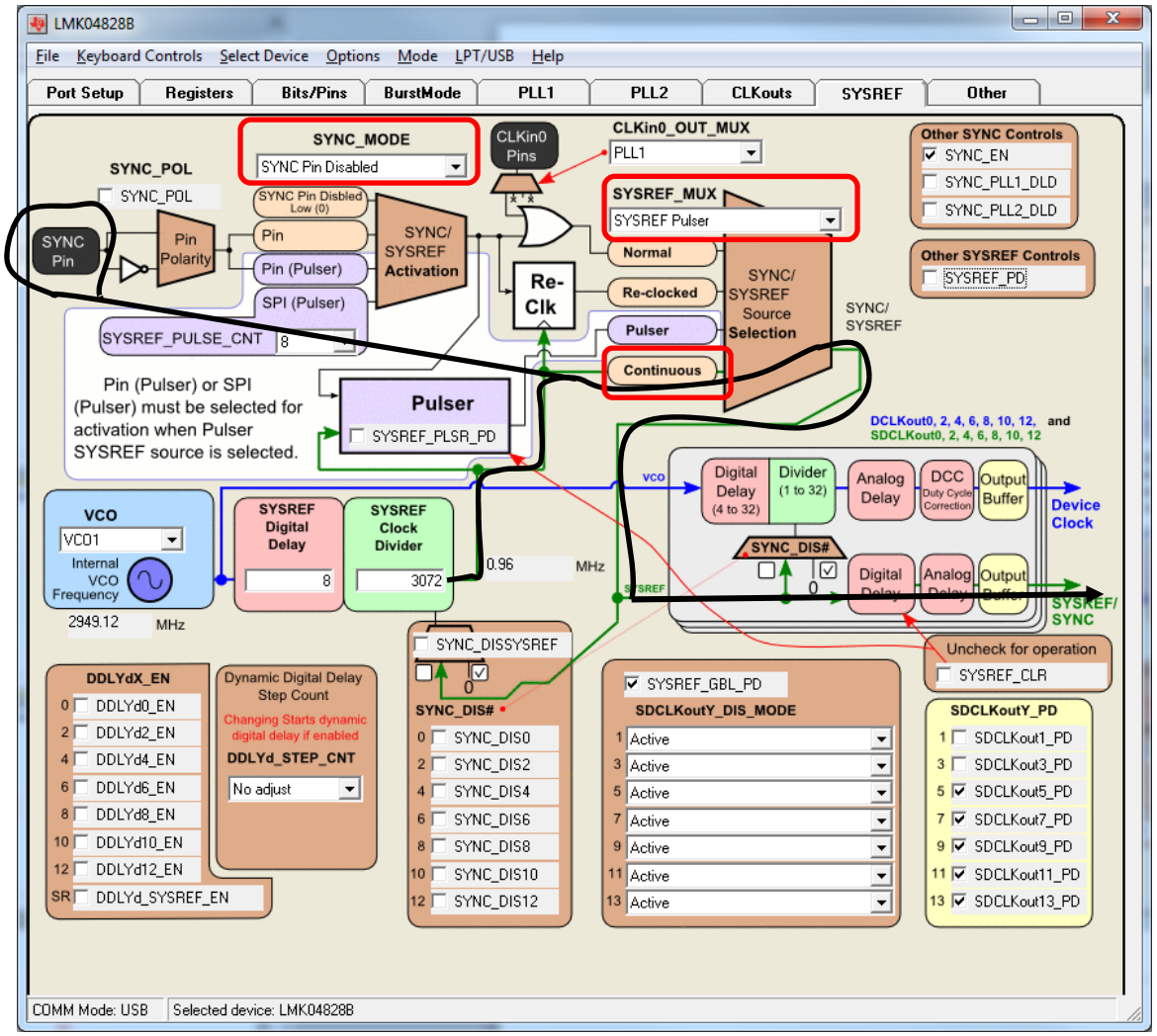


6c) Set Desired SYSREF Generation Mode - SYSREF Request

When SYSREF_REQ_EN = 1, a high input into the SYNC pin results in a continuous stream of SYSREF pulses until SYNC pin is set low.

To eliminate possible glitches on SYSREF, program the SYSREF_MUX = “SYSREF Pulser” and power up the Pulser block, SYSREF_PLSR_PD = 0.

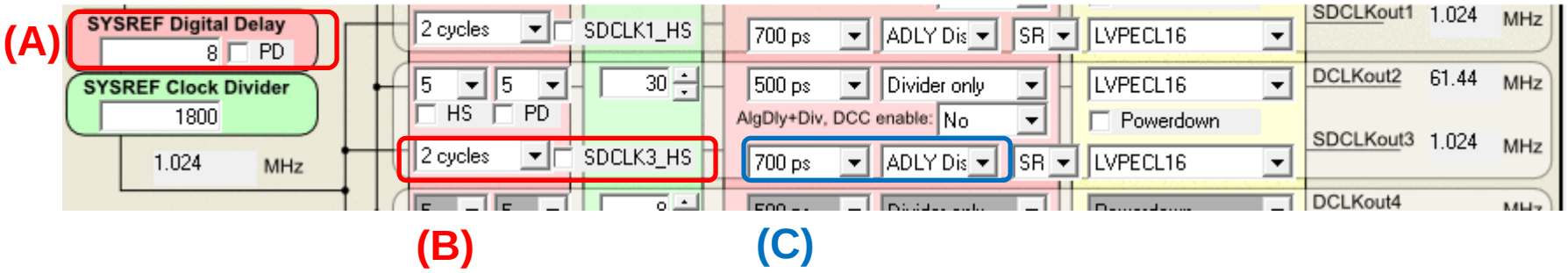




Adjusting SYSREF Digital Delay

Adjusting SYSREF to Device Clock

- Once device clock digital delay is set as desired, SYSREF adjustment can be performed by adjusting…
  - The global SYSREF digital delay **(A)**. Must execute a SYNC to cause this digital delay to take effect. This is a coarse adjustment.
  - Best method to adjust SYSREF is using the local digital delay **(B)** on each SYSREF output.
    - SDCLKoutY_DDLY and SDCLKoutY_HS
  - Alternative method is to use analog delay **(C)**. This is good adjustment of SYSREF with lower frequency Device Clock due to PVT variation on analog delay. Also useful when digital delay has a large steps because of low external VCO frequency.



- The best way to adjust SYSREF to Device Clock setup-hold time is with SYSREF operating in continuous mode.