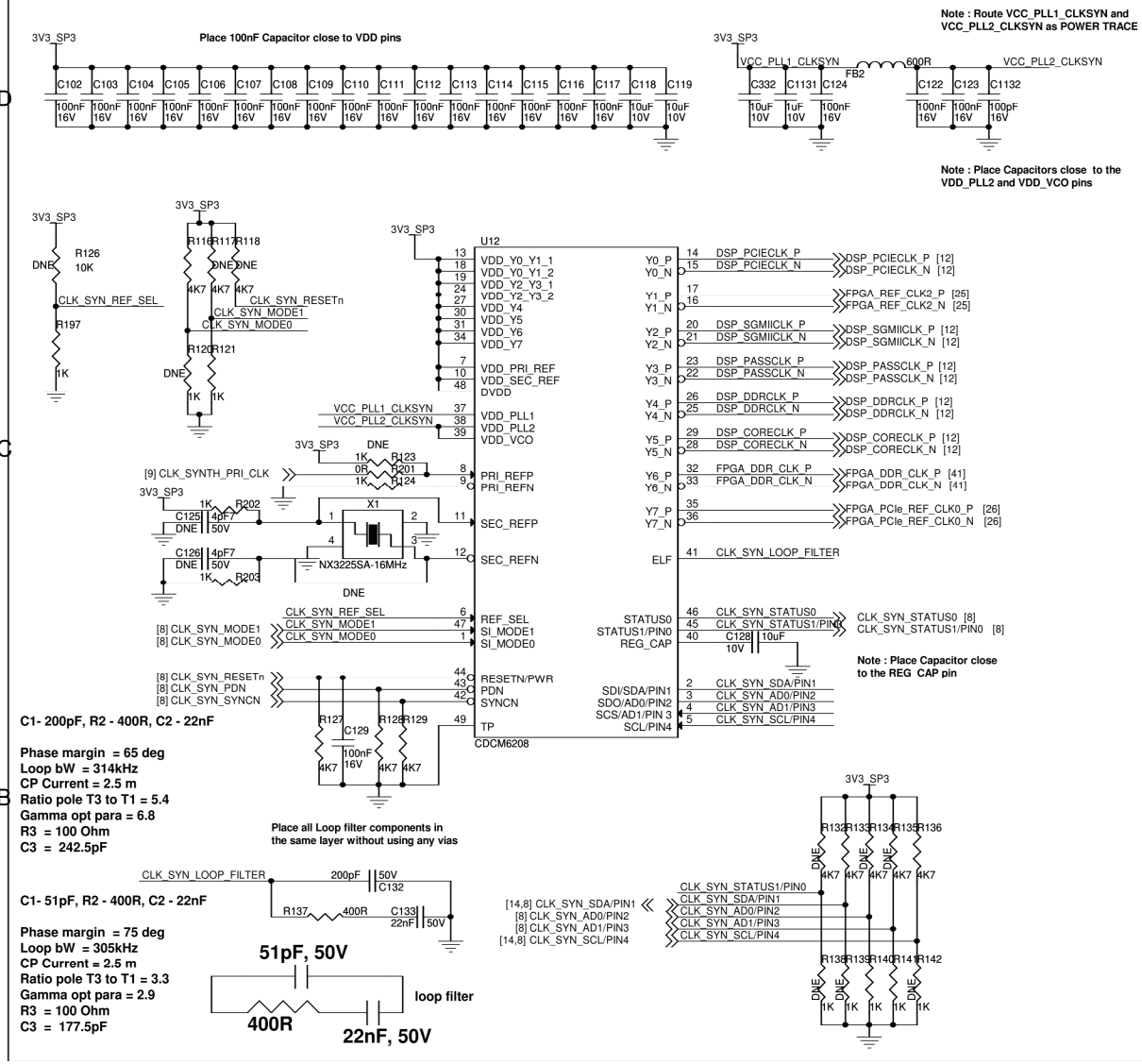
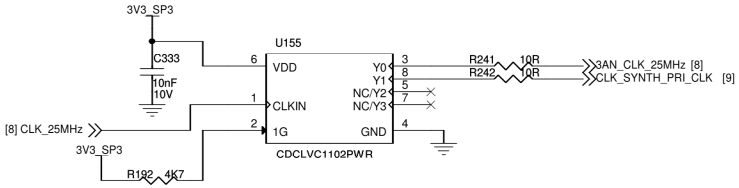
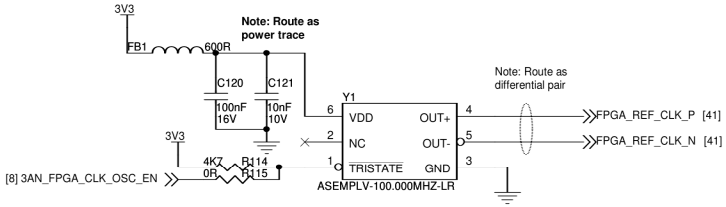
CLOCK SYNTHESIZER



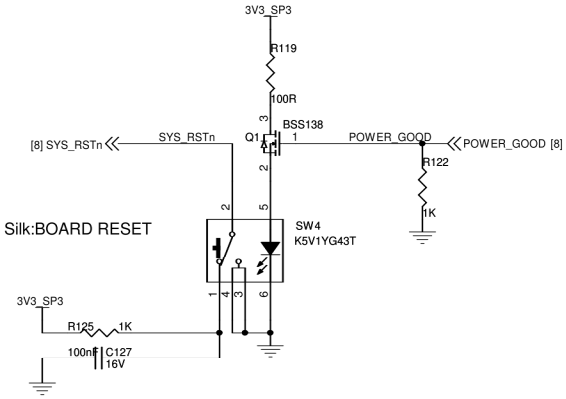
CLOCK BUFFER



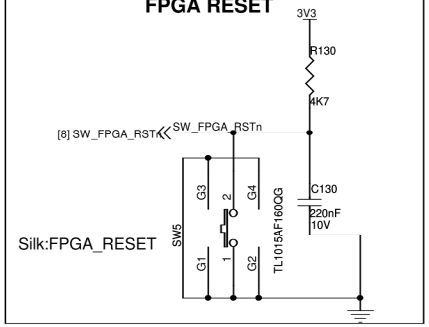
FPGA SYSTEM CLOCK



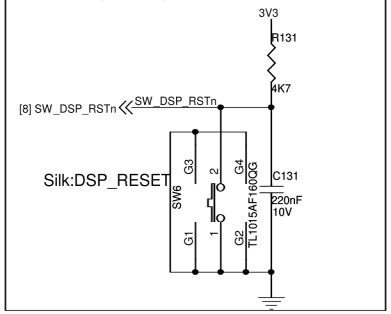
RESET SECTION (SYSTEM , DSP, FPGA RESET)



FPGA RESET



DSP RESET



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DATE	19/03/2014	
CHKD BY	Sakthi	Title: 09. CLK_SYNTH_FPGA_CLK_SYS_RST
DATE	6/04/2014	
APPD BY	Amrendra	Size: A3 / Document: NPOL-TCC / Rev: 0.2
DATE	20/06/2014	
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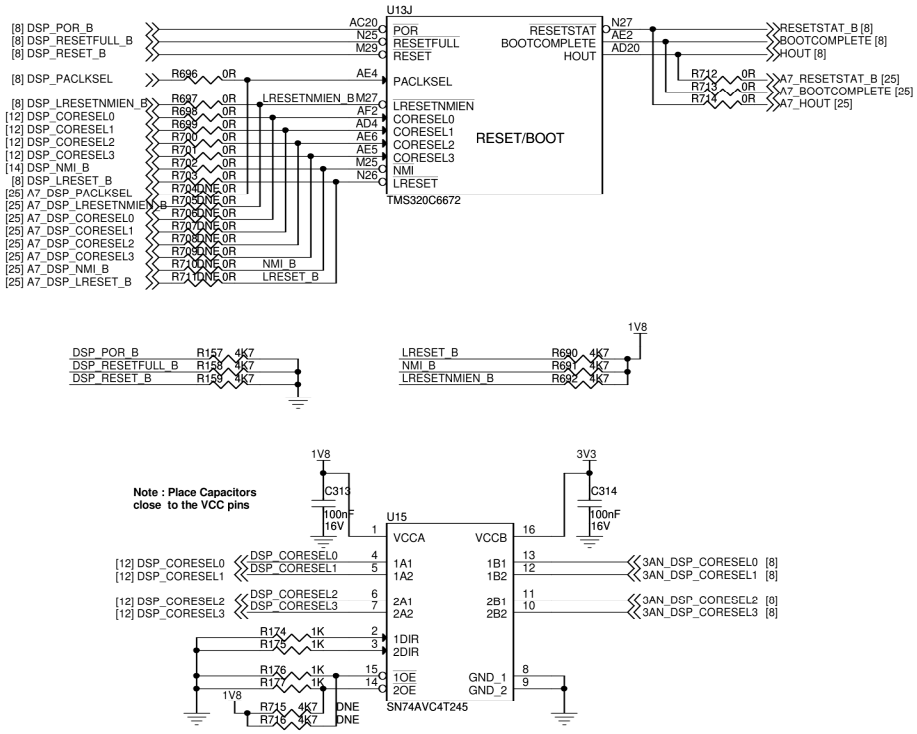
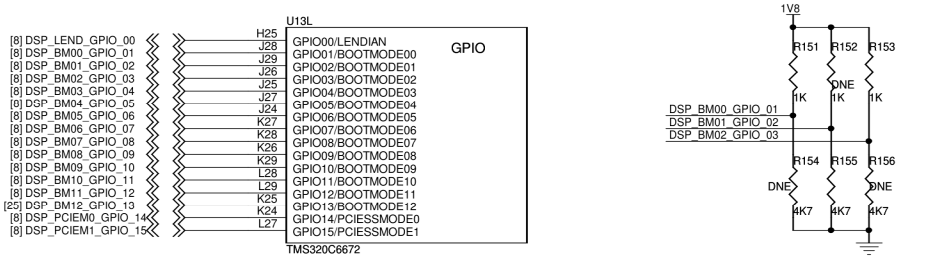
DSP RESET/BOOT

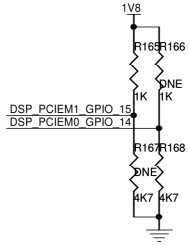


DSP BOOTSTRAP/GPIO

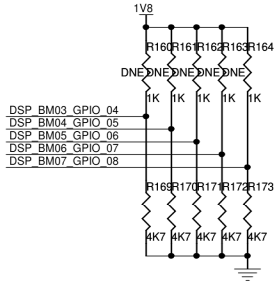


IIC MODE

PCIe ROOT COMPLEX MODE



IIC PARAMETER INDEX



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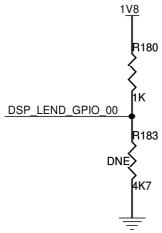
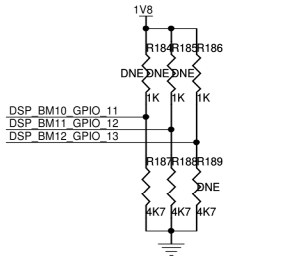


IIC ADD AND SPEED



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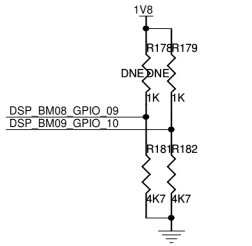
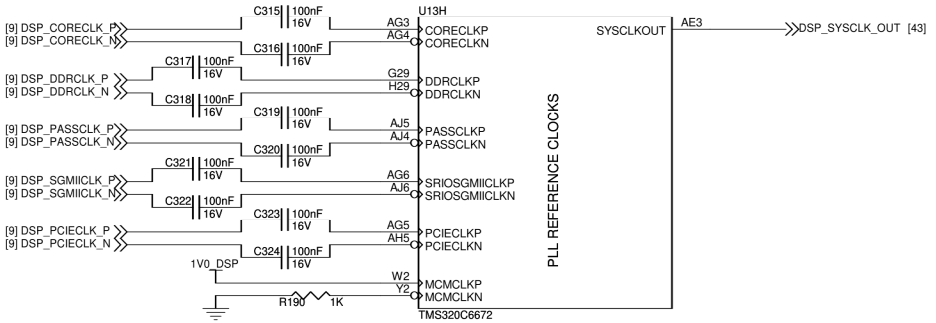
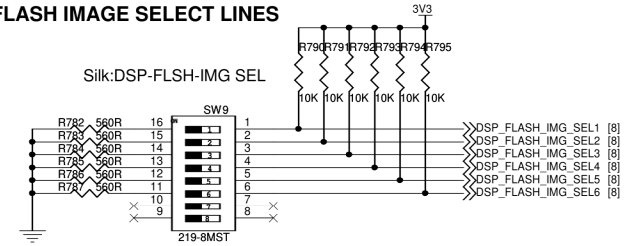


DSP CLOCKS



DSP FLASH IMAGE SELECT LINES



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DATE	19/03/2014	
CHKD BY	Sakthi	Title: 12. DSP_RESET_BOOTSTRAP_CLK
DATE	6/04/2014	
APPD BY	Amrendra	Size: A3 / Document: NPOL-TCC / Rev: 0.2
DATE	20/06/2014	
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