

Customer Configuration & Results

Clock Design Tool

File Help

Design Flow: Home Customer Requirements Select Solution Select Configuration Simulation

Color Legend

CLKin Custom Dual Loop Clock Conditioner with JESD204B VCXO VCXO

CLKinX 122.88 MHz

PLL1_R 256

PLL1 PDF 480 kHz CP 0.45 mA

LOOPFILTER1 2nd Order R (kohms) C (nF) C1 0.056 R2 270.0 C2 2.7

VCXO 30.72 MHz 2.0 kHz/V

OSCout 2VPECL MHz

PLL1_N 64

PLL2_R 1

PLL2 PDF 30720 kHz CP 3.2 mA

LOOPFILTER2 4th Order R (kohms) C (nF) C1 0.039 R2 1.2 C2 3.3 R3 0.2 C3 0.01 R4 0.2 C4 0.01

VCO 2920.0 to 3080.0 2949.12 MHz 18.3734 MHz/V

Manual Kvco

PLL2_N_PRE 2 **PLL2_N** 48

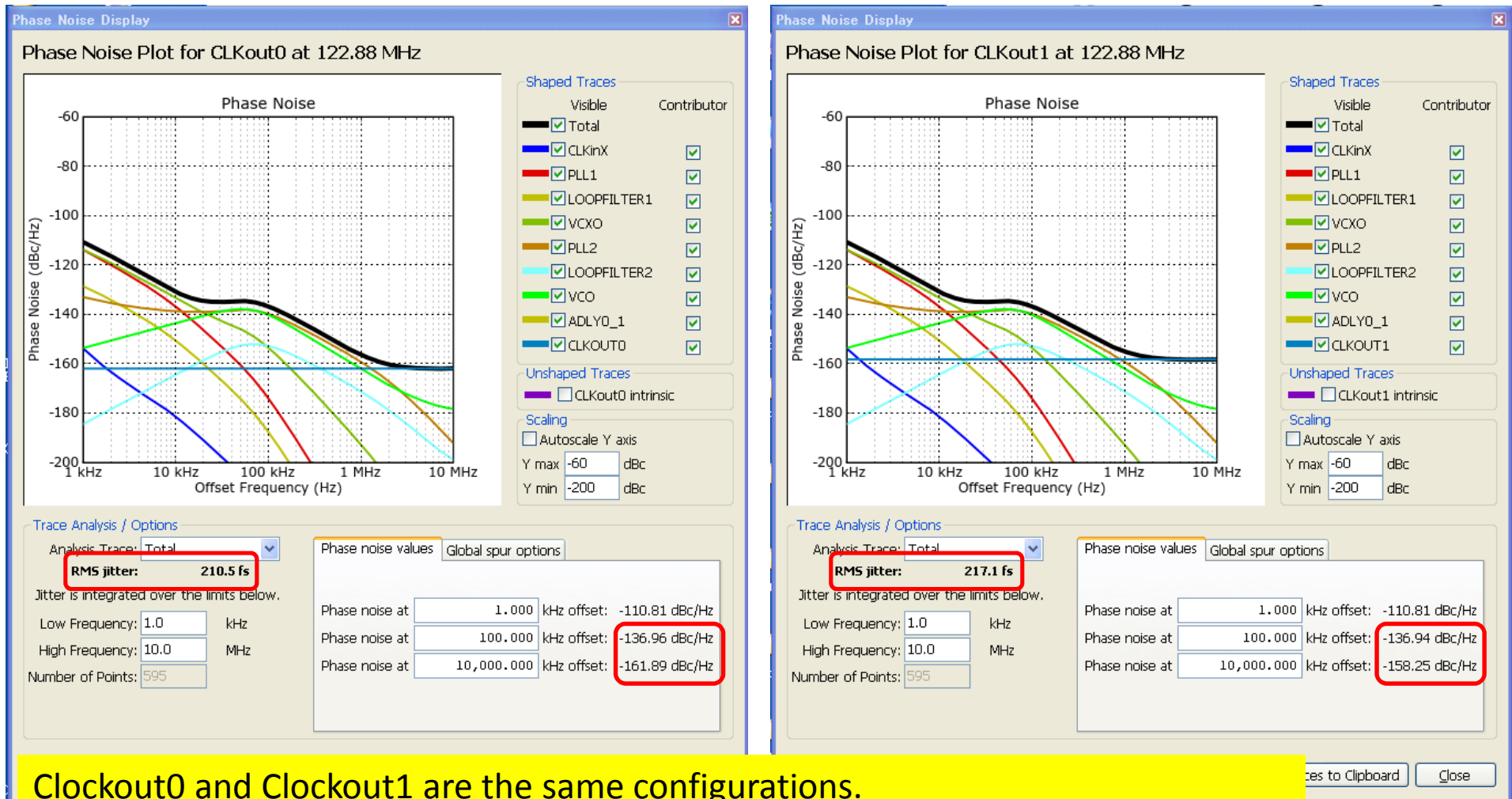
DIVIDE0_1 24 **ADLY0_1** Bypassed

CLKout0 LVDS 122.88 MHz

CLKout1 LVDS 122.88 MHz

Clockout0 and Clockout1 are the same configurations.
(frequency=122.88MHz, format=LVDS)

Phase Noise & RMS Jitter results of CLKout0/1



Clockout0 and Clockout1 are the same configurations.

But the results are different.

Why is that ?

Is this because models of additive jitter are different every output ? or is it a bug?