
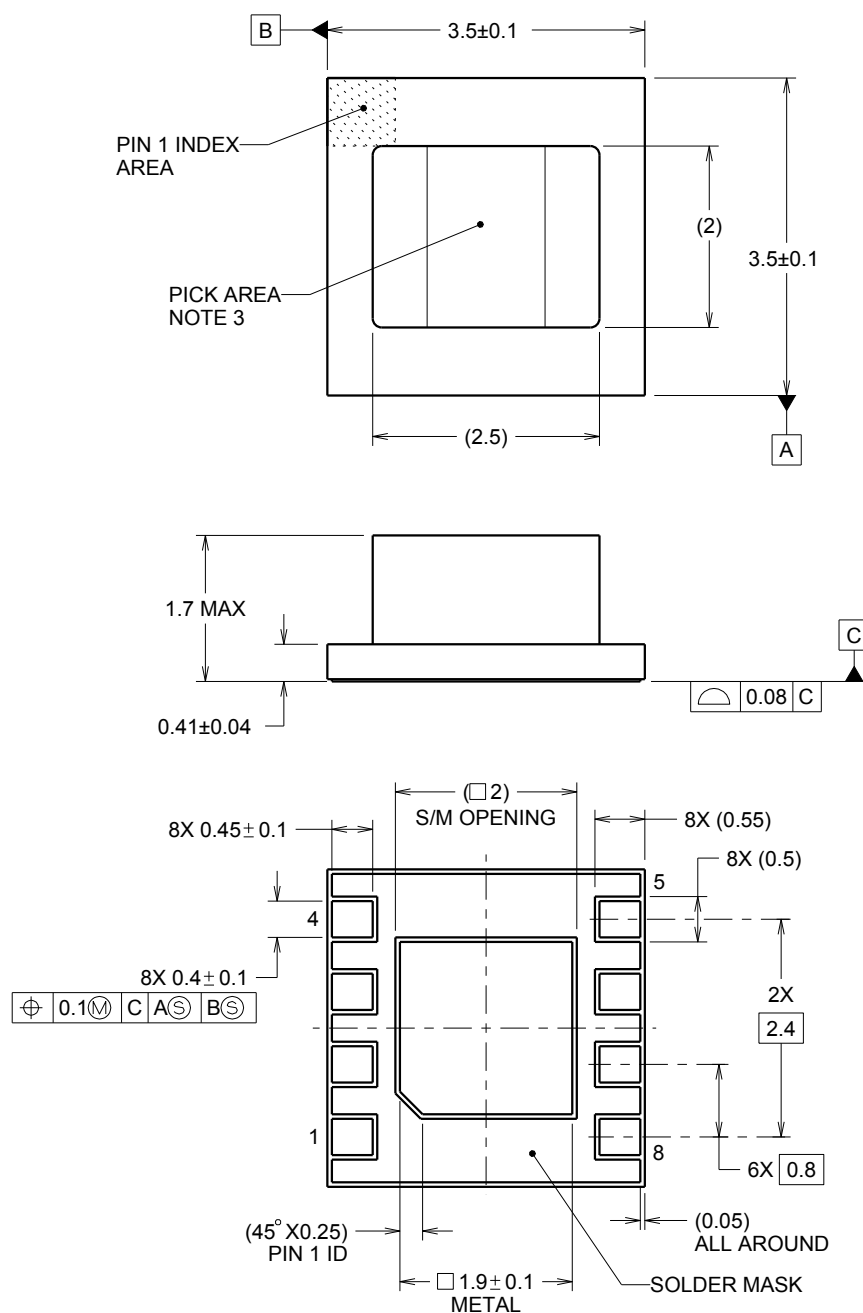
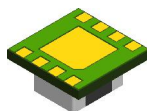


DATA BOOK  
PACKAGE OUTLINE

SUBSTRATE DRAWING
6576631

DRAFTER:	T. LEQUANG	DATE:	10/09/2013	DIMENSIONS IN MILLIMETERS	
DESIGNER:		DATE:		 <b>TEXAS INSTRUMENTS</b> SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
CHECKER:	K. SINCERBOX	DATE:	10/09/2013		
ENGINEER:	D. LEWIS	DATE:	10/09/2013		
APPROVED:	E. REY	DATE:	10/09/2013		
RELEASED:	WDM	DATE:	10/2013		
TEMPLATE INFO:	EDGE# 4218519 REV A	DATE:	03/20/2013	SCALE	SIZE
					A
				4221020	REV A
					PAGE 1 OF 5

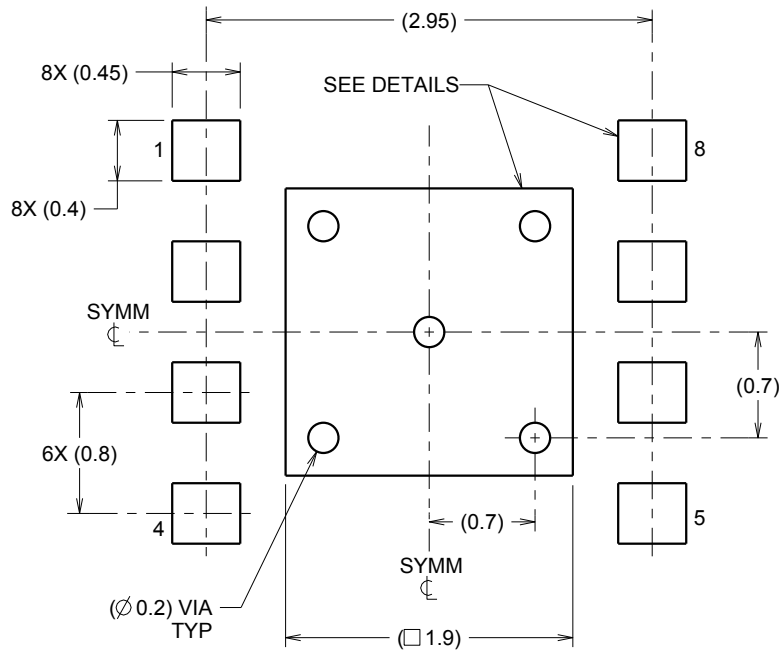
ePOD, SIL0008B / MicroSiP™,  
8 PIN, 0.8 MM PITCH



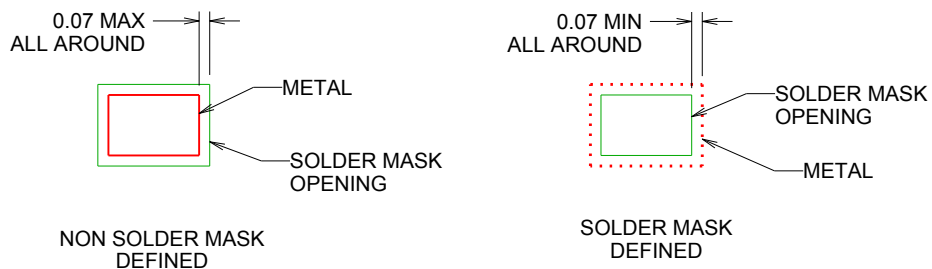
4221020/A 10/2013

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle  $\varnothing 1.3$  mm or smaller recommended.



**LAND PATTERN EXAMPLE**  
1:1 RATIO WITH PACKAGE SOLDER PADS  
SCALE:20X



**SOLDER MASK DETAILS**  
NOT TO SCALE

4221020/A 10/2013

NOTES: (continued)

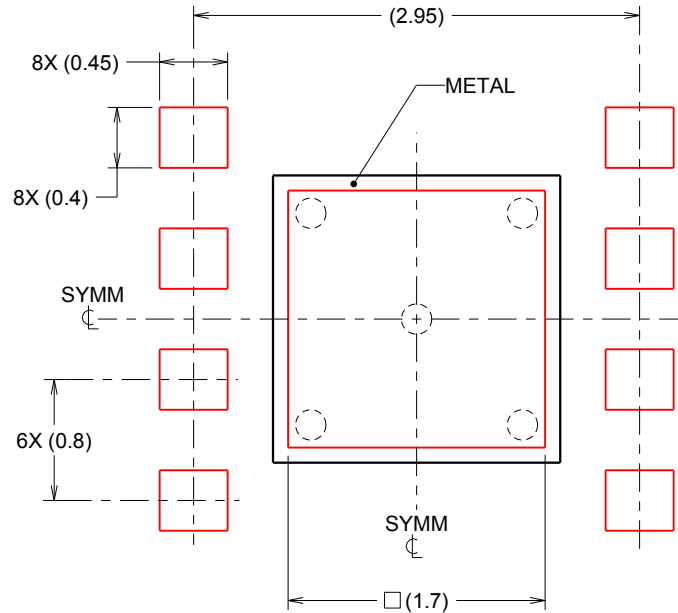
- This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

SIL0008B

MicroSiP™ - 1.7 mm max height

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4221020/A 10/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2136833	10/09/2013	D. LEWIS / T. LEQUANG