National Semiconductor

LM49155

Boomer® Audio Power Amplifier Series

PRELIMINARY

July 26, 2010

Uplink Noise Suppression & Downlink SNR Enhancement Analog Audio Subsystem

General Description

The LM49155 is a fully integrated audio subsystem designed for portable handheld applications such as cellular phones. The LM49155 combines a Noise Suppression microphone amplifier, a 1.35W mono class D amplifier with ALC, class AB earpiece driver with AGC, a high efficiency, stereo, ground referenced headphone amplifier with click pop suppression and I²C modes select and volume control.

The LM49155 features analog fully differential input, and differential output microphone amplifier designed to reduce background acoustic noise, while delivering superb speech clarity in voice communication applications. Downlink SNR enhancement utilizes an advanced acoustic AGC technology to adjust output levels.

The LM49155 speaker amplifier features National's unique output limiter that provides both a no-clip feature and speaker protection. The E²S class D amplifier features a patented, ultra low EMI PWM architecture that significantly reduces RF emissions while preserving audio quality and efficiency. The headphone drivers feature National's ground referenced architecture that creates a ground-referenced output from a single, low-voltage supply.

The LM49155 is available in an ultra-small 36-bump micro SMD package.

Key Specifications

- Uplink Far Field Noise Suppression
  - Electrical $FFNS_E$ at f = 1kHz — 34dB (typ)
- Downlink SNR Enhancement Earpiece Amplifier
  - Near-Field SNR Enhancement — 6 to 18dB (typ)
  - Downlink $SNRI_E$ — 16dB (typ)
- Class D Loudspeaker Amplifier R_L = 15µH+8Ω+15µH
  - P_{OUT}, THD+N ≤ 1%, V_{DD} = 3.6V — 680mW (typ)
  - P_{OUT}, THD+N ≤ 1%, V_{DD} = 5.0V — 1.35W (typ)
  - Efficiency — 88% (typ)
- Headphone Amplifier R_L = 32Ω
  - P_{OUT}, THD+N ≤ 1%, HPV_{DD} = 1.8V — 19mW (typ)

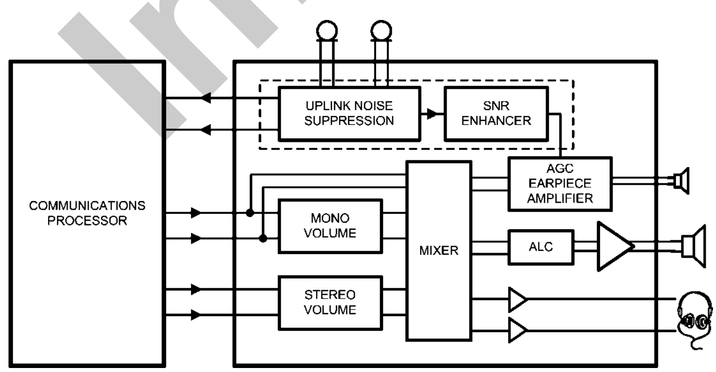
Features

- Noise cancellation for uplink and downlink without DSP-type artifacts, distortions or delays
- Adapting AGC on ambient noise level & downlink signal strength for earpiece
- Downlink adjustable noise-reducing high pass filter
- E²S Class D Amplifier with ALC
- Ground Referenced Headphone Outputs with Advanced Click Pop Suppression
- I²C Volume and Mode Control
- Micro-power shutdown

Applications

- Mobile Phones
- Portable Electronic Devices

Simplified Block Diagram



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Typical Application

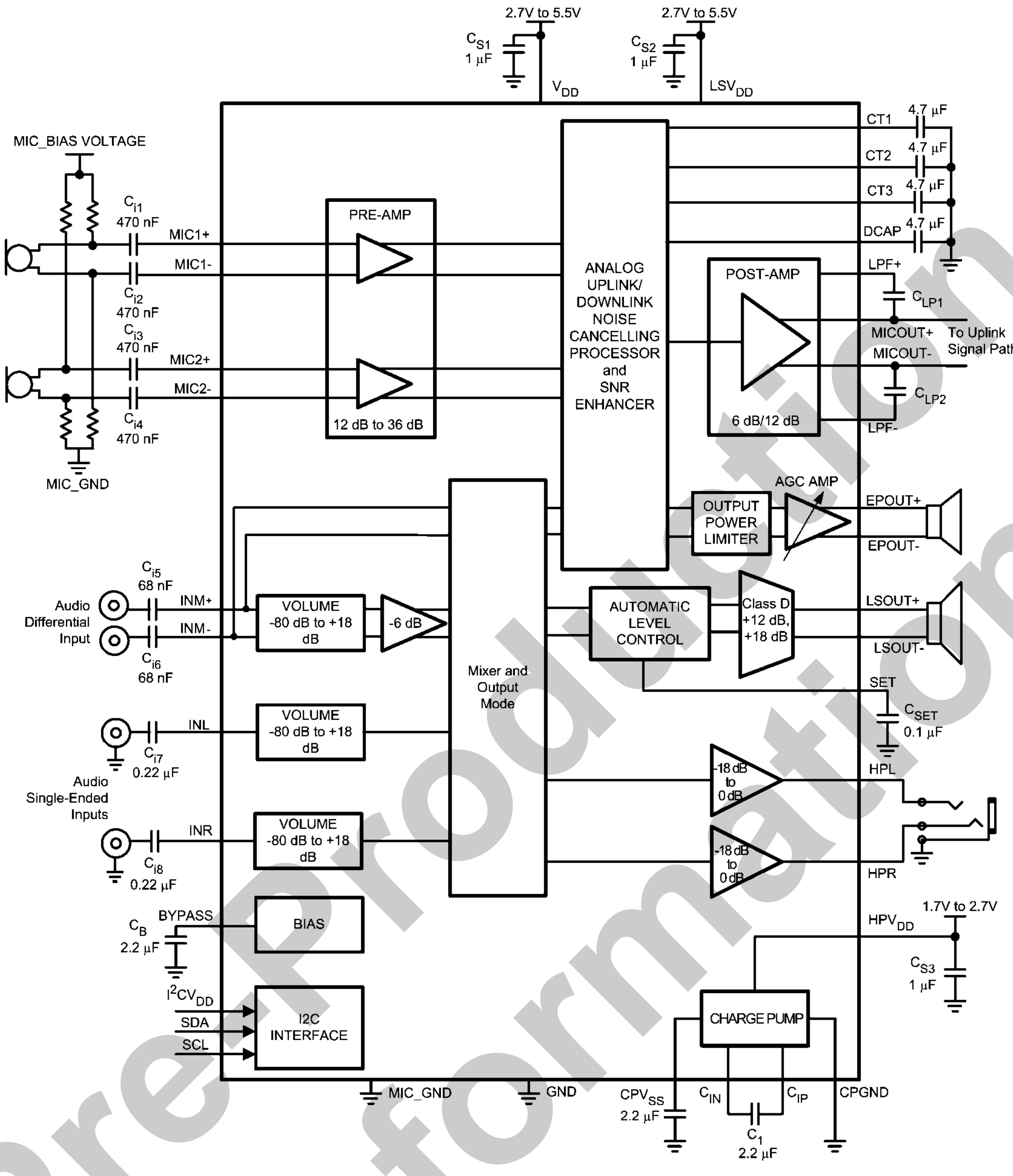
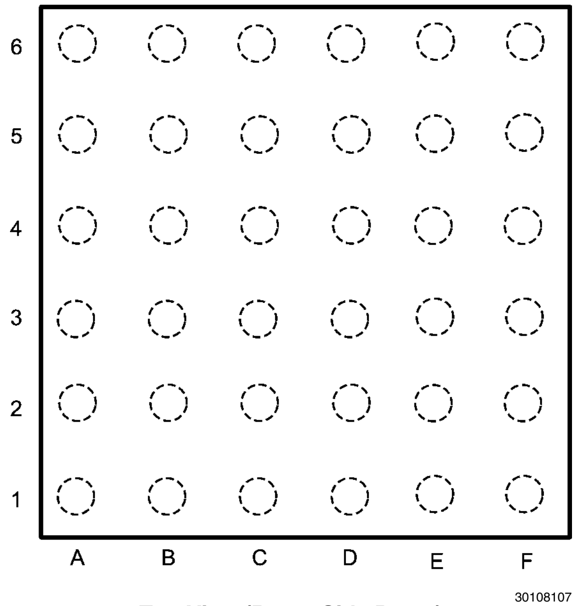


FIGURE 1. Typical Application Circuit

Connection Diagrams

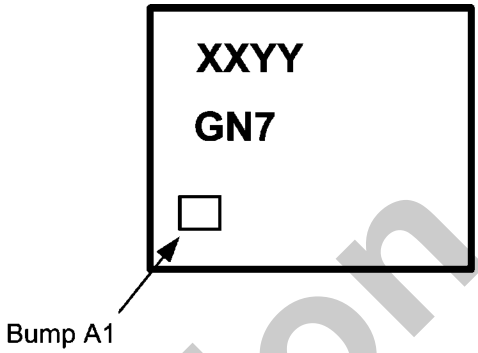
TL Package
(3.434mm x 3.459mm x 0.6mm)

Top View



Top View (Bump Side Down)
Order Number LM49155TL
See NS Package Number TLA36STA

36 Bump micro SMD Marking



Top View
XX — Date Code
YY — Die Traceability
G — Boomer
N7 — LM49155TL

Ordering Information

Order Number	Package	Package DWG #	Transport Media	MSL Level	Green Status
LM49155TL	36 Bump microSMD	TLA36STA	250 units on tape and reel	1	NOPB
LM49155TLX	36 Bump microSMD	TLA36STA	3000 units on tape and reel	1	NOPB

TABLE 1. Bump Description

BUMP	NAME	DESCRIPTION
A1	SDA	I2C serial data input
A2	SCL	I2C serial clock input
A3	CT1	Control timing capacitor
A4	V_{DD}	Main power supply
A5	DCAP	Voice signal detection capacitor
A6	MIC_GND	Microphone ground
B1	LPF-	Low pass filter for negative uplink output
B2	LPF+	Low pass filter for positive uplink output
B3	CT2	Control timing capacitor
B4	CT3	Control timing capacitor
B5	MIC1-	Microphone 1 inverting input
B6	MIC1+	Microphone 1 non-inverting input
C1	MICOUT-	Microphone inverting output
C2	MICOUT+	Microphone non-inverting output
C3	INM+	Mono channel inverting input
C4	INM-	Mono channel non-inverting input
C5	MIC2-	Microphone 2 inverting input
C6	MIC2+	Microphone 2 non-inverting input
D1	I^2CV_{DD}	I2C power supply
D2	SET	ALC timing set
D3	EPOUT+	Earpiece non-inverting output
D4	INR	Right channel input
D5	INL	Left channel input
D6	CPV_{SS}	Charge pump output
E1	LSV_{DD}	Loudspeaker/Earpiece power supply
E2	BYPASS	Mid-Rail bias bypass node
E3	EPOUT-	Earpiece inverting output
E4	C_{1P}	Charge pump flying capacitor positive terminal
E5	C_{1N}	Charge pump flying capacitor negative terminal
E6	HPV_{DD}	Headphone power supply
F1	LSOUT+	Loudspeaker non-inverting output
F2	LSOUT-	Loudspeaker inverting output
F3	GND	Main Power supply ground
F4	CPGND	Charge pump ground
F5	HPR	Right channel headphone output
F6	HPL	Left channel headphone output

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{DD}, I^2CV_{DD} (Note 1)	6V
Supply Voltage	
HPV_{DD} (Note 1)	3V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3 V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Rating, Human Body Model (Note 4)	2000V
ESD Rating, Machine Model (Note 5)	150V
ESD Rating, Charge Device Model (Note 6)	750V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (TLA36STA)	64°C/W

Soldering Information

See Applications Note AN-1112 “Micro SMD Level Chip Scale Package”

Operating Ratings

Temperature Range	
$T_{MIN} < T_A < T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	
V_{DD} and LSV_{DD}	2.7V ≤ to ≤ 5.5V
HPV_{DD}	1.7V ≤ to ≤ 2.7V
I^2CV_{DD}	1.7V ≤ to ≤ 5.5V
	$I^2CV_{DD} \le V_{DD}$

Electrical Characteristics: $V_{DD} = LSV_{DD} = 3.6V$, $HPV_{DD} = 1.8V$ (Note 1, Note 2)

The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN = 12dB, HPGAIN = 0dB, EPGAIN = 0dB, R_L = 15µH +8Ω+15µH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 32Ω (Earpiece), MIC_PREGAIN = 20dB, MIC_POSTGAIN = 6dB, MIC Input = 18mV$_{P-P}$, C_{SET} = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 8)

Symbol	Parameter	Conditions	LM49155		Units (Limits)
			Typical (Note 7)	Limit (Note 8)	
DC CHARACTERISTICS (V_{IN} = 0, No Load)					
I_{DDQ}	Quiescent Power Supply Current ($LSV_{DD} + V_{DD}$)	GAMP_SD = 1			
		LS Mode, Mono mode 1	3	4	mA (max)
		HP Mode, mode 8	1.3	1.6	mA (max)
		MIC Pass Through mode	0.6	0.8	mA (max)
		LS + HP, Mode 5	3.1	4	mA (max)
		LS + HP, Mode 10	3.4	4.3	mA (max)
		GAMP_SD = 0			
		LS Mode, Mono mode 1	3.7	5	mA (max)
		HP Mode, mode 8	1.7	2.1	mA (max)
		EP Mode, SNR Enhancer Off	0.8	1.3	mA (max)
		EP Mode, SNR Enhancer On	3.8	4.5	mA (max)
		LS + HP, Mode 5, 10	3.8	5	mA (max)
$I_{DDQ(HP)}$	Quiescent Power Supply Current (HPV_{DD})	HP Mode, mode 8	3	4	mA (max)
I_{SD}	Total Shutdown Current		0.05	1	µA (max)
$I_{DDQ\ (I^2C)}$	Quiescent I²C Power Supply Current (I^2CV_{DD})		0.05		µA
LOUDSPEAKER AMPLIFIER (Note 9)					
η	Efficiency	THD+N = 1%	88		%
THD+N	Total Harmonic Distortion + Noise	Mono Input Signal, P_O = 250mW	0.015		%
P_O	Output Power	Mono Input Signal, THD+N = 1%			
		LSV_{DD} = 3.6V	680	620	mW (min)
		LSV_{DD} = 4.2V	940		mW
		LSV_{DD} = 5.0V	1.35		W

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Symbol	Parameter	Conditions	LM49155 Typical (Note 7)	LM49155 Limit (Note 8)	Units (Limits)
PSRR	Power Supply Rejection Ratio	f = 217Hz, V_{RIPPLE} = 200mV_{P-P}, All inputs terminated to AC GND, C_B = 2.2µF, Output Referred			
		LS Mode 1, Mono Input	72		dB
		LS Mode 2, Stereo Input	60		dB
		LS Mode 3, Mono + Stereo Input	60		dB
SNR	Signal To Noise Ratio	P_O = 680mW, A-weighted	94		dB
ϵ_{OS}	Output Noise	A-weighted, All inputs terminated to AC GND			
		LS Mode 1, Mono Input	46		µV
		LS Mode 2, Stereo Input	55		µV
		LS Mode 3, Mono + Stereo Input	60		µV
CMRR	Common Mode Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f_{RIPPLE} = 217Hz, Mono Input Signal	55		dB
V_{OS}	Output Offset Voltage	LS Mode 1, Mono Input	10	40	mV (max)
		LS Mode 2, Stereo Input	10		mV
		LS Mode 3, Mono + Stereo Input	10		mV
Z_{IN}	Input Impedance	Maximum Gain Setting (MONO input) Minimum Gain Setting (MONO input)	12.5 99		kΩ kΩ
HEADPHONE AMPLIFIER					
THD+N	Total Harmonic Distortion + Noise	Stereo Input Signal, P_O = 12mW	0.01		%
P_O	Output Power	Stereo Input Signal, THD+N = 1%			
		R_L = 16Ω R_L = 32Ω	19 19	 15	mW mW (min)
PSRR	Power Supply Rejection Ration	f = 217Hz, V_{RIPPLE} = 200mV_{P-P}, All inputs terminated to AC GND, C_B = 2.2µF			
		Ripple on HPV_{DD} HP Mode 4, Mono Input HP Mode 8, Stereo Input HP Mode 12, Mono + Stereo Input	 94 90 90		 dB dB dB
		Ripple on V_{DD} HP Mode 4, Mono Input HP Mode 8, Stereo Input HP Mode 12, Mono + Stereo Input	 94 78 78		 dB dB dB
SNR	Signal-to-Noise Ratio	P_O = 20mW, A-weighted	95		dB
ϵ_{OS}	Output Noise	A-weighted, All inputs terminated to AC GND			
		HP Mode 4, Mono Input HP Mode 8, Stereo Input HP Mode 12, Mono + Stereo Input	9 10 12		µV µV µV
X_{TALK}	Crosstalk	P_O = 12mW	85		dB
V_{OS}	Output Offset Voltage	HP Mode 4, Mono Input HP Mode 8, Stereo Input HP Mode 12, Mono + Stereo Input	1.2 1. 2 1.5		mV mV mV
T_{WU}	Turn-On Time	HP Mode 8, C_B = 2.2µF Normal turn on time Fast turn on time	 27 15		 ms ms
VOLUME AND GAIN CONTROL					

Symbol	Parameter	Conditions	LM49155		Units (Limits)
			Typical (Note 7)	Limit (Note 8)	
A_{VOL}	Volume Control	Minimum Gain Setting (MONO input)	–80		dB dB
		Maximum Gain Setting (MONO input)	18		dB dB
		Minimum Gain Setting (Stereo input)	–80		dB dB
		Maximum Gain Setting (Stereo input)	18		dB dB
	Volume Control Gain Error		±0.5		dB
A_V	Gain	LS Mode Gain 0 Gain 1	 12 18		 dB dB
		HP Mode Gain 0 Gain 1 Gain 2 Gain 3 Gain 4 Gain 5 Gain 6 Gain 7	0 –1.5 –3 –6 –9 –12 –15 –18		dB dB dB dB dB dB dB dB
A_M	Microphone Pre Amplifier Gain Range	Minimum setting Maximum setting	12 36		dB dB
A_{MR}	Microphone Pre Amplifier Gain Resolution		2	1.7 2.3	dB (min) dB (max)
A_P	Post Amplifier Gain Range	Minimum setting Maximum setting	6 12		dB dB
A_{PR}	Post Amplifier Gain Resolution		6	5.5 6.5	dB (min) dB (max)
AUTOMATIC LEVEL CONTROL (ALC)					
t_A	Attack Time	ATTACK_TIME = 00	0.75		ms
t_R	Release Time	RELEASE_TIME = 00	1		s
V_{LIMIT}	Output Voltage Limit	LS Mode, THD+N ≤1%, Note 10			
		VOLTAGE_LEVEL = 001	4		V_{P-P}
		VOLTAGE_LEVEL = 010	4.8		V_{P-P}
		VOLTAGE_LEVEL = 011	5.6		V_{P-P}
		VOLTAGE_LEVEL = 100	6.4		V_{P-P}
UPLINK SPECIFICATIONS (Mic Pass Through mode)					
$FFNSE_{ADC}$	Far Field Noise Suppression (Electrical)	f = 1kHz (See Test Methods)	34	26	dB (min)
		f = 300Hz (See Test Methods)	42		dB (min)
$SNRI_E$	Signal-to-Noise Ratio Improvement (Electrical)	f = 1kHz (See Test Methods)	26	18	dB (min)
		f = 300Hz (See Test Methods)	33		dB (min)
V_{IN}	Maximum Input Signal	THD+N < 1%, Pre Amp Gain = 12dB		440	mV_{P-P} (max)
V_{OUT}	Maximum AC Output Voltage	Differential Output, f = 1kHz, THD+N < 1%	1.2	1.1	V_{RMS} (min)
	DC Level at Outputs	V_{IN} = GND	820		mV
THD+N	Total Harmonic Distortion + Noise	Differential Output	0.1	0.2	% (max)
SNR	Signal-to-Noise Ratio	$V_{IN} = 18mV_{P-P}$	63		dB
		$V_{IN} = 18mV_{P-P}$, A-Weighted	65		dB

Symbol	Parameter	Conditions	LM49155 Typical (Note 7)	LM49155 Limit (Note 8)	Units (Limits)
e_N	Input Referred Noise level	A-Weighted	5		μV_{RMS}
Z_{IN}	Input Impedance		142	103 220	kΩ (min) kΩ (max)
Z_{OUT}	Output Impedance		200		Ω
Z_{LOAD}	Allowable Load Impedance	R_{LOAD} C_{LOAD}		10 100	kΩ (min) pF (max)
PSRR	Power Supply Rejection Ratio	Input Referred, Input AC Grounded (470nF)			
		f = 217Hz, V_{RIPPLE} = 200mV_{P-P}	99	85	dB (min)
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}	95	80	dB (min)
CMRR	Common Mode Rejection Ratio	Input referred	57		dB
DOWNLINK SPECIFICATIONS (SNR Enhancer Off)					
$V_{IN(DV)}$	Maximum Input Signal (Differential)	THD+N < 1%, AGC_{AV} = 0dB	4.5	4.2	$V_{PP(DIFF)}$ (min)
V_{OS}	Output Offset Voltage	$V_{IN(DV)}$ = 0V, R_L = 32Ω	0.8	5	mV (max)
e_N	Output Noise level	A-Weighted, $V_{IN(DV)}$ = 0V, AGC_{AV} = 0dB	10		μV_{RMS}
SNR	Downlink Signal-to-Noise Ratio	P_O = 70mW P_O= 70mW, A-Weighted	99 105		dB dB
P_{OUT}	Output Power	THD+N < 1%, f = 1kHz, R_L = 32Ω	80	70	mW (min)
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, P_O = 50mW, R_L = 32Ω	0.04		% (max)
PSRR	Power Supply Rejection Ratio	Input AC Grounded (68nF)			
		f = 217Hz, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω	95	80	dB (min)
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω	92		dB (min)
CMRR	Common Mode Rejection Ratio	V_{IN} = 200mV_{P-P}, f = 217Hz, R_L = 32Ω	55		dB
		V_{IN} = 200mV_{P-P}, f = 1kHz, R_L = 32Ω	55		dB
$Z_{IN(DL)}$	Downlink Input Impedance	EP_INPUT_IMPEDANCE = 00 EP_INPUT_IMPEDANCE = 01 EP_INPUT_IMPEDANCE = 10, 11	40 8.3 5.7		kΩ kΩ kΩ
SNR ENHANCEMENT SPECIFICATIONS					
AGC_{AV}	Automatic Gain Control Range	Minimum setting Maximum setting	0 18		dB dB
ΔAGC_{AV}	0dB Gain Accuracy	AGC_{AV} = 0dB, f = 1kHz, V_{DV} = 1V, Ambient Noise = 0V	±0.5		dB
$SNRI_E$	Signal-to-Noise Ratio Improvement	f = 300Hz			
		V_{DV} = 100mV_{P-P}, MIC1 = MIC2 = 0.8mV_{P-P}	6		dB
		V_{DV} = 100mV_{P-P}, MIC1 = MIC2 = 2mV_{P-P}	16		dB
		f = 1kHz			
		V_{DV} = 100mV_{P-P}, MIC1 = MIC2 = 1.4mV_{P-P}	12		dB
		V_{DV} = 100mV_{P-P}, MIC1 = MIC2 = 2mV_{P-P}	16		dB

Note 1: *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Charge Device Model, applicable std. JESD22-C101-C.

Note 7: Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

Note 8: Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Note 9: Loudspeaker R_L is a resistive load in series with two inductors to simulate an actual speaker load. For R_L = 8Ω, the load is 15µH + 8Ω +15µH. For R_L = 4Ω, the load is 15µH + 4Ω + 15µH.

Note 10: The LM49155 ALC limits the output power to which ever is lower, the supply voltage or output power limit.

I²C Interface Characteristics 1.7V ≤ I^2CV_{DD} ≤ 5.5V

(Note 1, Note 2) The following specifications apply for LS and HP VOLUMEGAIN = 0dB, LSGAIN =12dB, HPGAIN = 0dB, EPGAIN = 0dB, R_L = 15µH+8Ω+15µH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 32Ω (Earpiece), C_{SET} = 0.1µF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 8).

Symbol	Parameter	Conditions	LM49155 Typical	LM49155 Limit (Note 8)	Units (Limits)
	SCL Frequency		400		kHz (max)
1	Hold Time (repeated) START Condition			0.6	µs (min)
2	Clock Low Time			1.3	µs (min)
3	Clock High Time			600	ns (min)
4	Setup Time (repeated) START Condition			600	ns (min)
5	Data Hold Time			900	ns (max)
6	Data Setup Time			250	ns (min)
7	Rise Time of SDA and SCL			$20+0.1C_B$ 300	ns (min) ns (max)
8	Fall Time of SDA and SCL			$20+0.1C_B$ 300	ns (min) ns (max)
9	Setup Time for STOP Condition			600	ns (min)
10	Bus Free Time Between a STOP and START Condition			1.3	µs (min)
C_B	Bus Capacitance			200	pF (max)
V_{IH}	Input High Voltage			$0.7*I^2CV_{DD}$	V (min)
V_{IL}	Input Low Voltage			$0.3*I^2CV_{DD}$	V (max)

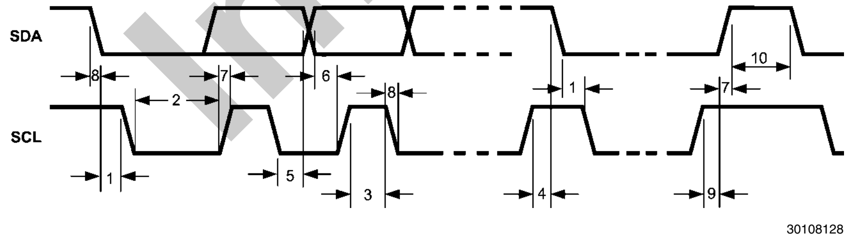
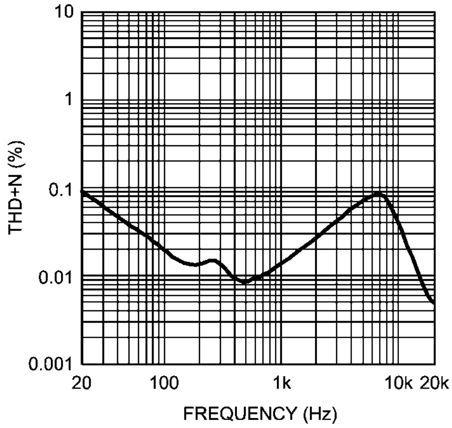


FIGURE 2. I²C Timing Diagram

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 3.6V, R_L = 15μH+8Ω+15μH, P_{OUT} = 250mW
Speaker Mode 1



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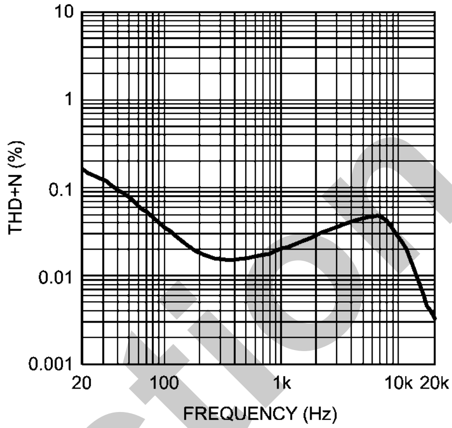
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 16Ω, P_{OUT} = 20mW
Headphone Mode 8



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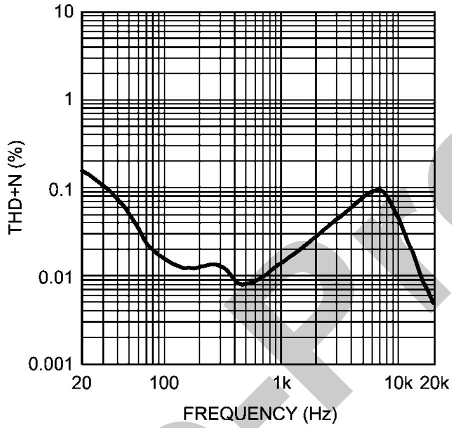
THD+N vs Frequency
V_{DD} = 4.2V, R_L = 15μH+8Ω+15μH, P_{OUT} = 300mW
Speaker Mode 1



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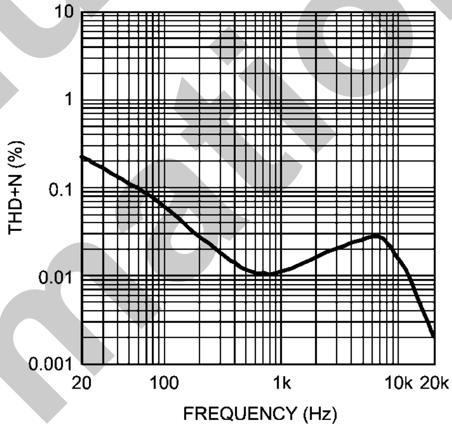
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω, P_{OUT} = 12mW
Headphone Mode 8



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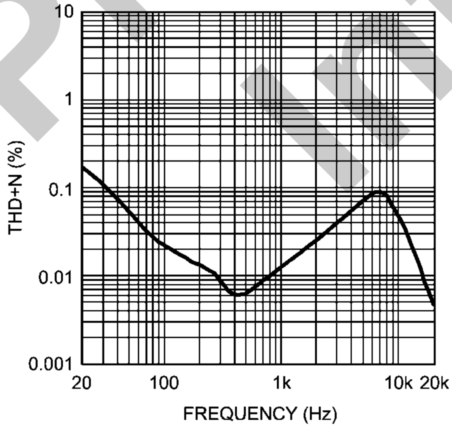
THD+N vs Frequency
V_{DD} = 5V, R_L = 15μH+8Ω+15μH, P_{OUT} = 600mW
Speaker Mode 1



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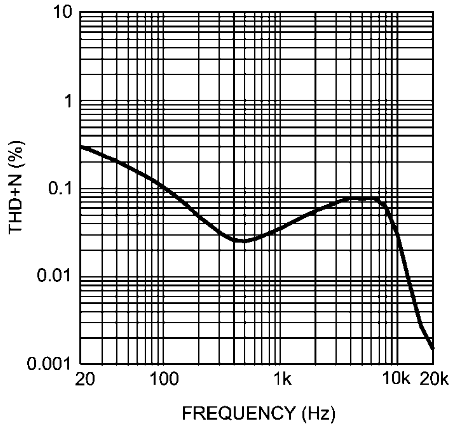
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω, P_{OUT} = 20mW
EP Mode



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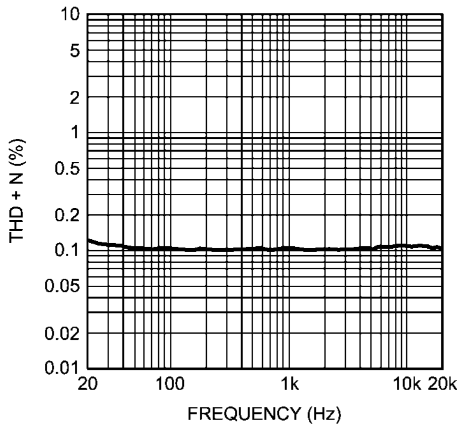
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF
Mic 1 Pass Through Mode



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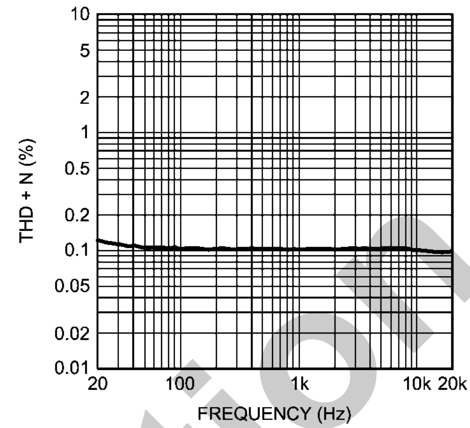
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF
Mic 2 Pass Through Mode



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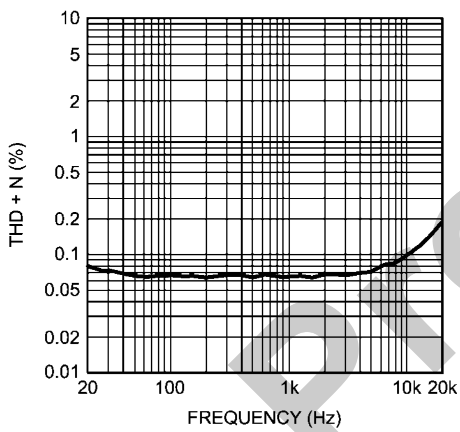
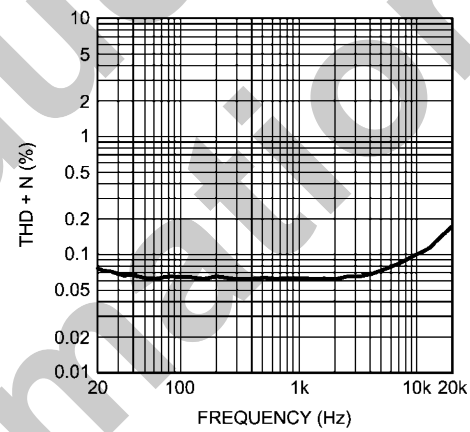
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF
Mic2 = AC GND, Mic1 = 18mV$_{P-P}$
Noise Cancelling Mode



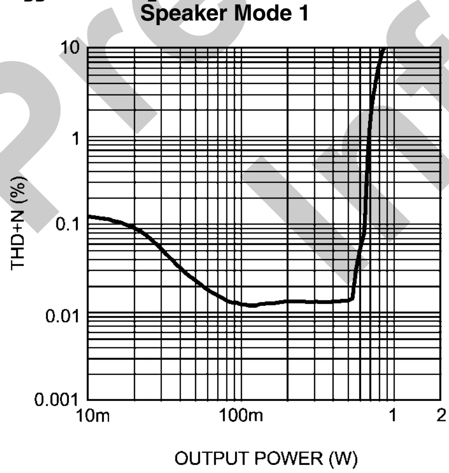
30108189

THD+N vs Frequency
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF
Mic1 = AC GND, Mic2 = 18mV$_{P-P}$
Noise Cancelling Mode



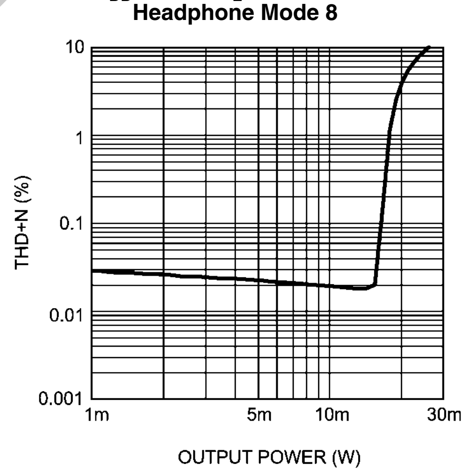
30108190

THD+N vs Output Power
V_{DD} = 3.6V, R_L = 15μH+8Ω+15μH, f = 1kHz
Speaker Mode 1



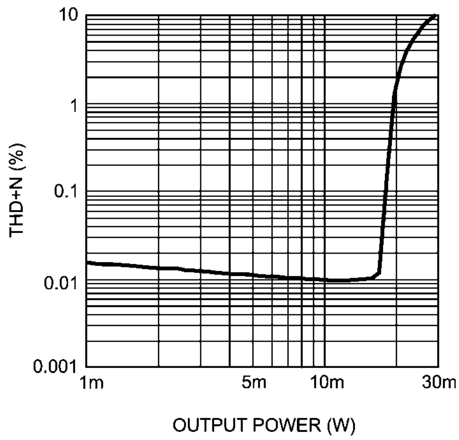
30108196

THD+N vs Output Power
HPV_{DD} = 1.8V, R_L = 16Ω, f = 1kHz
Headphone Mode 8



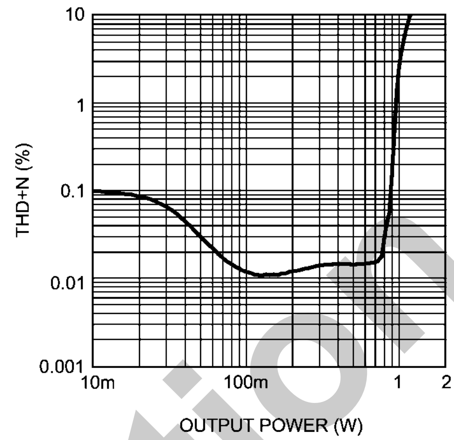
30108197

THD+N vs Output Power
HPV_{DD} = 1.8V, R_L = 32Ω, f = 1kHz
Headphone Mode 8



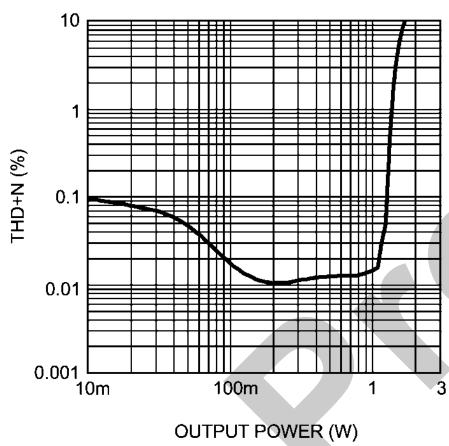
30108199

THD+N vs Output Power
V_{DD} = 4.2V, R_L = 15μH+8Ω+15μH, f = 1kHz
Speaker Mode 1



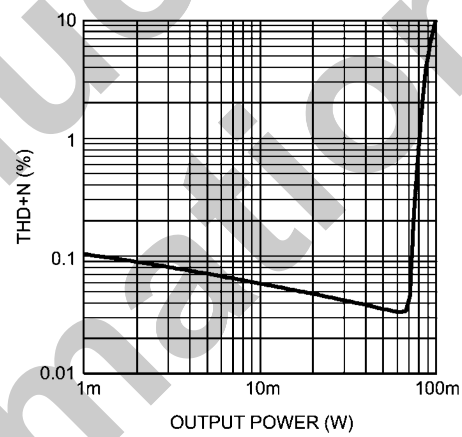
301081a0

THD+N vs Output Power
V_{DD} = 5V, R_L = 15μH+8Ω+15μH, f = 1kHz
Speaker Mode 1



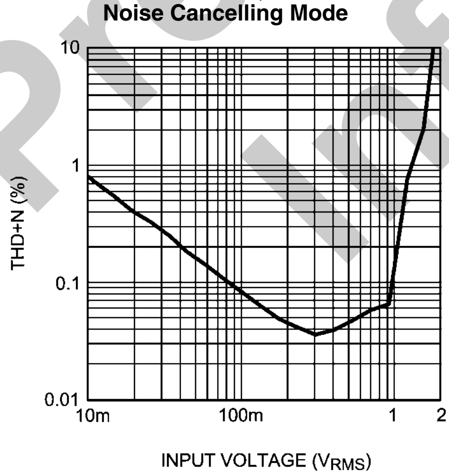
301081a1

THD+N vs Output Power
V_{DD} = 3.6V, R_L = 32Ω, f = 1kHz
EP Mode



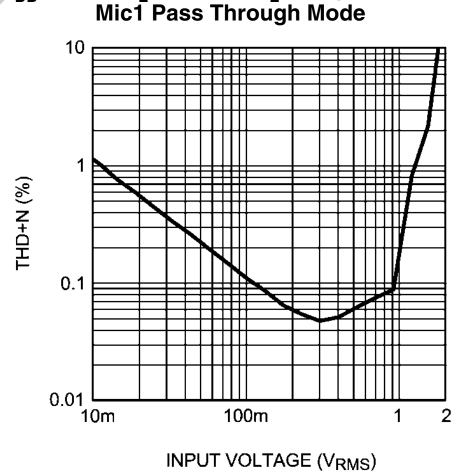
30108103

THD+N vs Mic Input Voltage
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF
Mic1 = AC GND, f = 1kHz
Noise Cancelling Mode



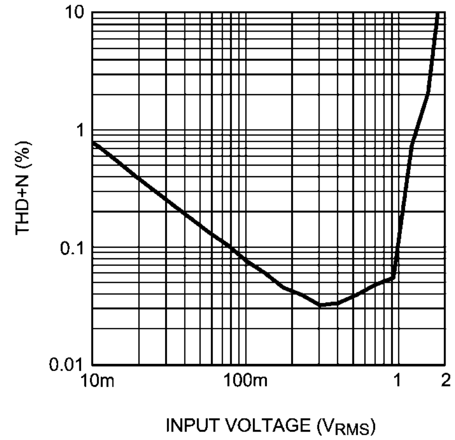
301081a5

THD+N vs Mic Input Voltage
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF, f = 1kHz
Mic1 Pass Through Mode



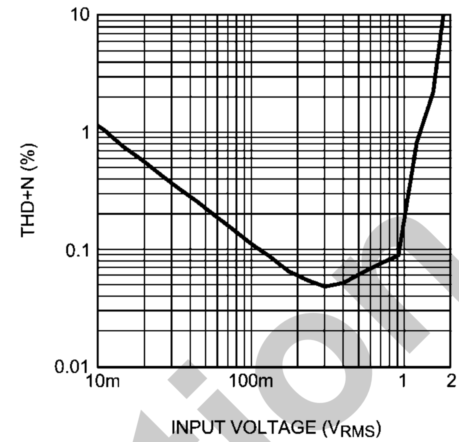
301081a6

THD+N vs Mic Input Voltage
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF
Mic2 = AC GND, f = 1kHz
Noise Cancelling Mode



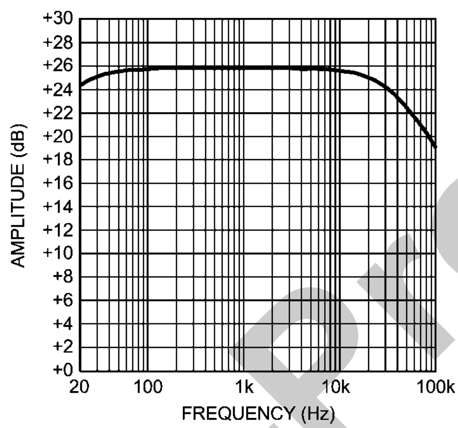
301081a7

THD+N vs Mic Input Voltage
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF, f = 1kHz
Mic2 Pass Through Mode



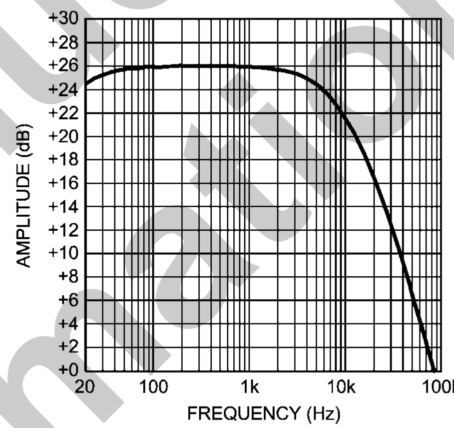
301081a8

Frequency Response
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF
Mic1 and 2 Pass Through Mode



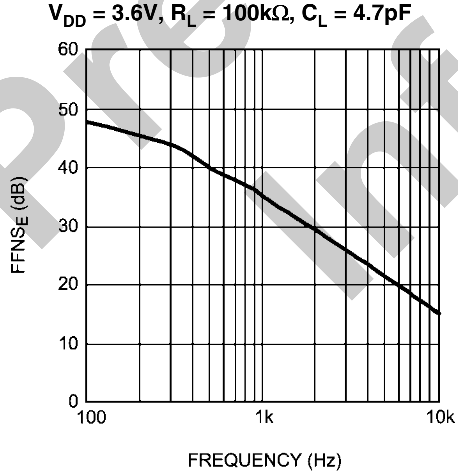
30108185

Frequency Response
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF
Noise Cancelling Mode



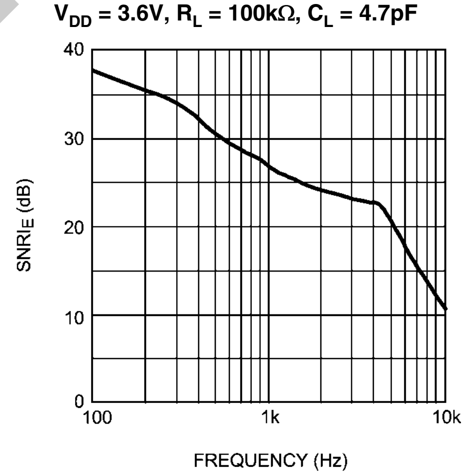
30108186

Far Field Noise Suppression Electrical vs Frequency
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF

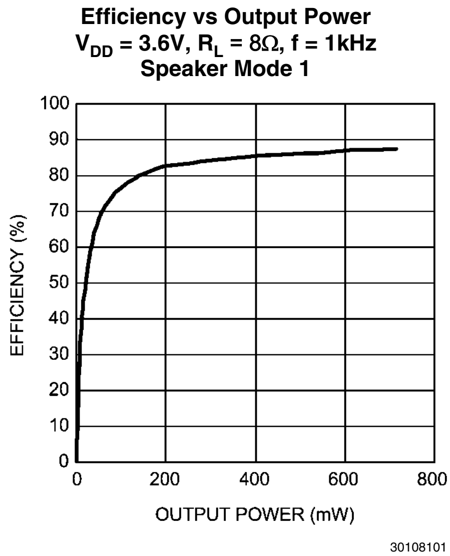


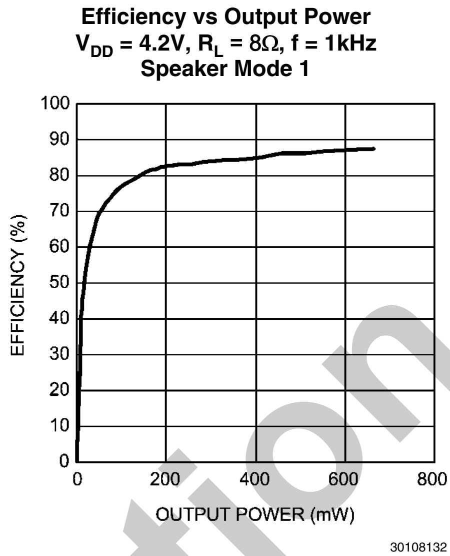
301081a3

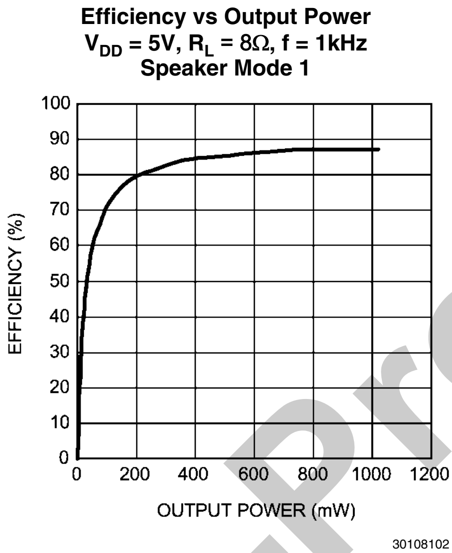
Signal-to-Noise Electrical vs Frequency
V_{DD} = 3.6V, R_L = 100kΩ, C_L = 4.7pF

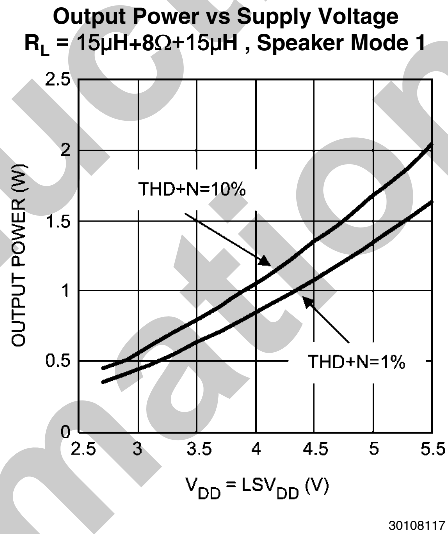


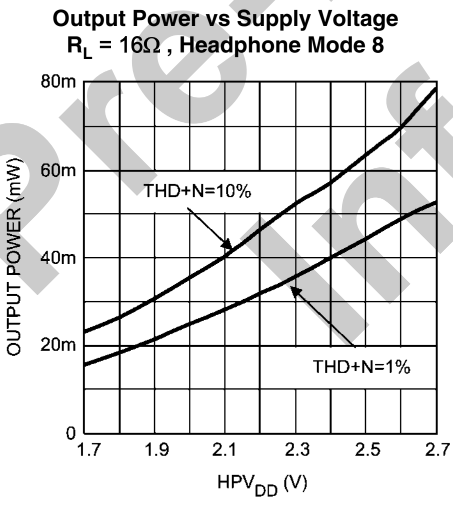
301081a4

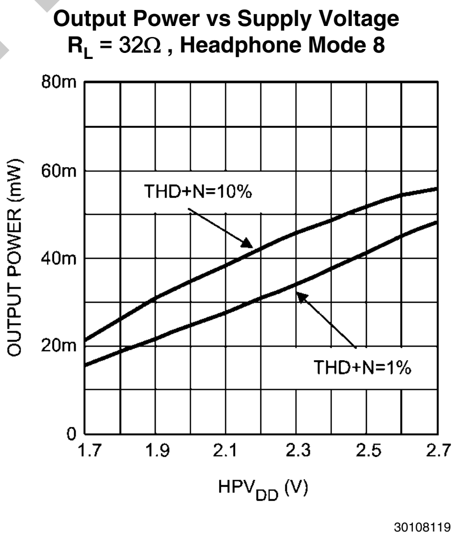

Efficiency vs Output Power
VDD = 3.6V, RL = 8Ω, f = 1kHz
Speaker Mode 1
EFFICIENCY (%)
OUTPUT POWER (mW)
30108101


Efficiency vs Output Power
VDD = 4.2V, RL = 8Ω, f = 1kHz
Speaker Mode 1
EFFICIENCY (%)
OUTPUT POWER (mW)
30108132

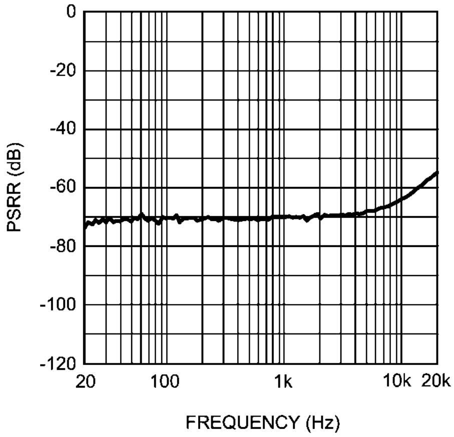

Efficiency vs Output Power
VDD = 5V, RL = 8Ω, f = 1kHz
Speaker Mode 1
EFFICIENCY (%)
OUTPUT POWER (mW)
30108102


Output Power vs Supply Voltage
RL = 15μH+8Ω+15μH , Speaker Mode 1
THD+N=10%
THD+N=1%
OUTPUT POWER (W)
VDD = LSVDD (V)
30108117


Output Power vs Supply Voltage
RL = 16Ω , Headphone Mode 8
THD+N=10%
THD+N=1%
OUTPUT POWER (mW)
HPVDD (V)
30108118

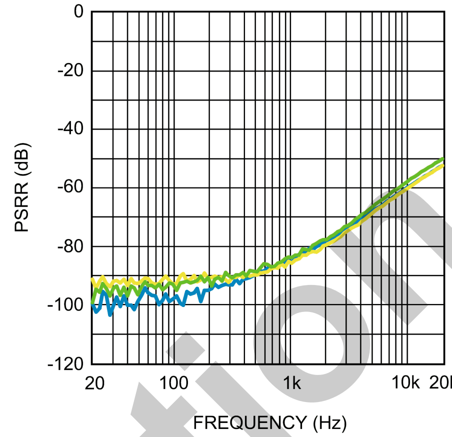

Output Power vs Supply Voltage
RL = 32Ω , Headphone Mode 8
THD+N=10%
THD+N=1%
OUTPUT POWER (mW)
HPVDD (V)
30108119

PSRR vs Frequency
$LSV_{DD} = V_{DD} = 3.6V + V_{RIPPLE} = 200mV_{P-P}$
R_L = 15µH+8Ω+15µH, Speaker Mode 1



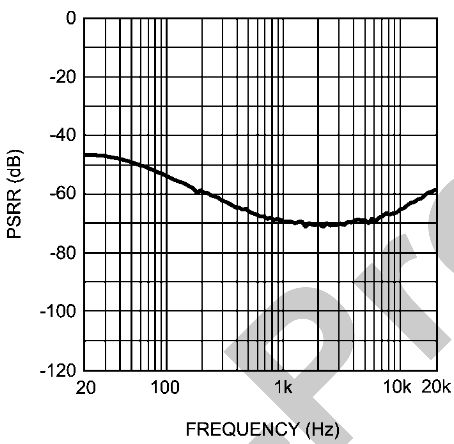
30108106

PSRR vs Frequency
$LSV_{DD} = V_{DD} = 3.6V + V_{RIPPLE} = 200mV_{P-P}$
R_L = 32Ω, HPV_{DD} = 1.8V, Headphone Mode
Yellow = Mode 4, Geen = Mode 8, Blue = Mode12



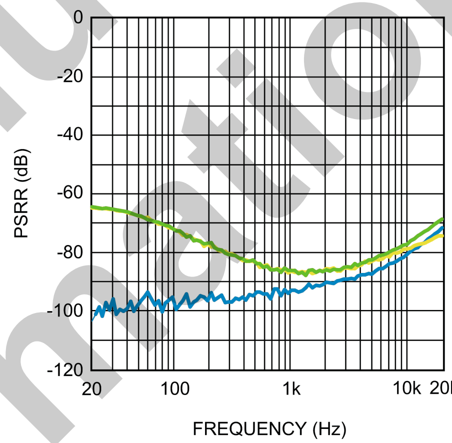
30108105

PSRR vs Frequency
$LS_{DD} = V_{DD} = 3.6V + V_{RIPPLE} = 200mV_{P-P}$
R_L = 15µH+8Ω+15µH, Speaker Mode 2



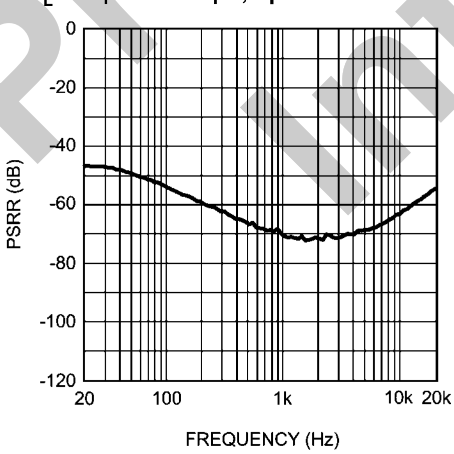
30108110

PSRR vs Frequency
$HPV_{DD} = V_{DD} = 1.8\ V_{RIPPLE} = 200mV_{P-P}$
$LSV_{DD} = V_{DD} = 3.6V$, R_L = 32Ω, Headphone Mode
Yellow = Mode 4, Geen = Mode 8, Blue = Mode12



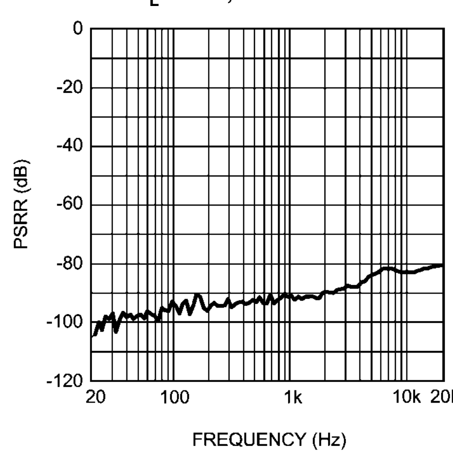
30108113

PSRR vs Frequency
$LS_{DD} = V_{DD} = 3.6V + V_{RIPPLE} = 200mV_{P-P}$
R_L = 15µH+8Ω+15µH, Speaker Mode 3



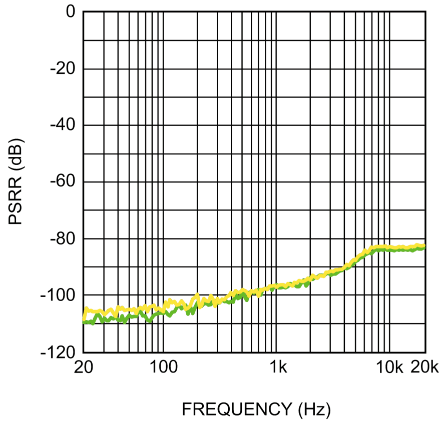
30108111

PSRR vs Frequency
$LS_{DD} = V_{DD} = 3.6V + V_{RIPPLE} = 200mV_{P-P}$
R_L = 32Ω, EP Mode



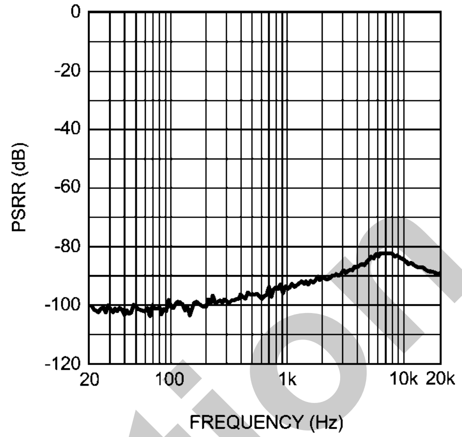
30108116

PSRR vs Frequency
$LS_{DD} = V_{DD} = 3.6V + V_{RIPPLE} = 200mV_{P-P}$
Input Referred
Yellow = Mic1 Pass through Mode
Green = Mic2 Pass through Mode



30108114

PSRR vs Frequency
$LS_{DD} = V_{DD} = 3.6V + V_{RIPPLE} = 200mV_{P-P}$
Input Referred, Noise Cancelling Mode



30108115

Test Methods

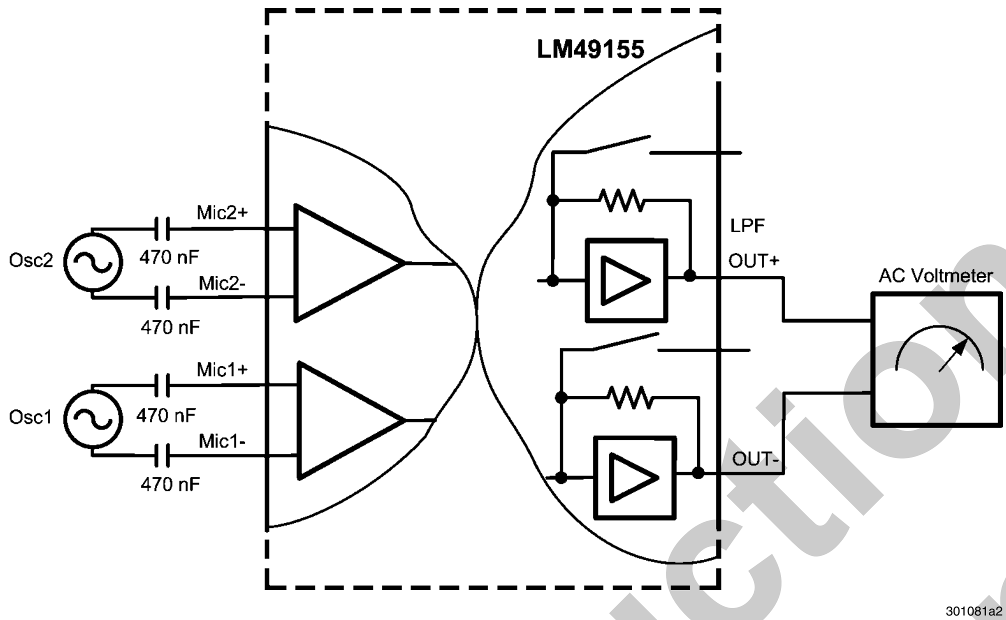


FIGURE 3. $FFNS_E$, $NFSL_E$, $SNRI_E$ Test Circuit

FAR FIELD NOISE SUPPRESSION ($FFNS_E$)

For optimum noise suppression the far field noise should be in a broadside array configuration from the two microphones (see *Figure 16*). Which means the far field sound source is equidistance from the two microphones. This configuration allows the amplitude of the far field signal to be equal at the two microphone inputs, however a slight phase difference may still exist. To simulate a real world application a slight phase delay was added to the $FFNS_E$ test. The block diagram from Figure 3 is used with the following procedure to measure the $FFNS_E$.

1. A 1kHz sine wave with equal frequency and amplitude ($25mV_{P-P}$) is applied to Mic1 and Mic2. Using a signal generator, the phase of Mic 2 is delayed by 1.1° when compared with Mic1. For 300Hz sine wave, use phase delay of .33°.
2. Measure the output level in dBV (X)
3. Mute the signal from Mic2
4. Measure the output level in dBV (Y)
5. $FFNS_E$ = Y - X dB

NEAR FIELD SPEECH LOSS ($NFSL_E$)

For optimum near field speech preservation, the sound source should be in an endfire array configuration from the two microphones (see *Figure 17*). In this configuration the speech signal at the microphone closest to the sound source will have greater amplitude than the microphone further away. Additionally the signal at microphone further away will experience a phase lag when compared with the closer microphone. To simulate this, phase delay as well as amplitude shift was added to the $NFSL_E$ test. The schematic from Figure 3 is used with the following procedure to measure the $NFSL_E$.

1. A $25mV_{P-P}$ and $17.25mV_{P-P}$ ($0.69*25mV_{P-P}$) 1kHz sine wave is applied to Mic1 and Mic2 respectively. Once again, a signal generator is used to delay the phase of Mic2 by 15.9° when compared with Mic1. For 300Hz sine wave, use phase delay of 4.76°.
2. Measure the output level in dBV (X)
3. Mute the signal from Mic2
4. Measure the output level in dBV (Y)
5. $NFSL_E$ = Y - X dB

SIGNAL TO NOISE RATIO IMPROVEMENT ELECTRICAL ($SNRI_E$)

The $SNRI_E$ is the ratio of $FFNS_E$ to $NFSL_E$ and is defined as:

$$SNRI_E = FFNS_E - NFSL_E$$

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System Control

I²C SIGNALS

In I²C mode the LM49155 pin SCL is used for the I²C clock SCL and the pin SDA is used for the I²C data signal SDA. Both of these signals need a pull-up resistor according to I²C specification. The 7-bits I²C slave address for LM49155 is 1111100.

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

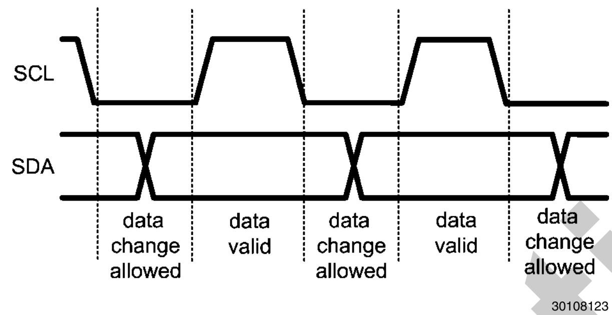

FIGURE 4. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

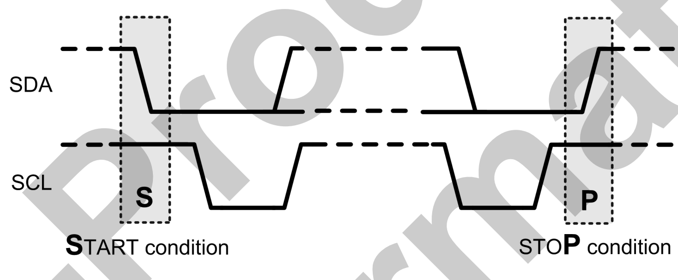

FIGURE 5. I²C Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received. After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eight bit which is a data direction bit (R/W). The LM49155 address is TBD. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

MSB							LSB
ADR6 Bit7	ADR5 bit6	ADR4 bit5	ADR3 bit4	ADR2 bit3	ADR1 bit2	ADR0 bit1	R/W bit0

I^2C SLAVE address (chip address)

30108125

FIGURE 6. I²C Chip Address

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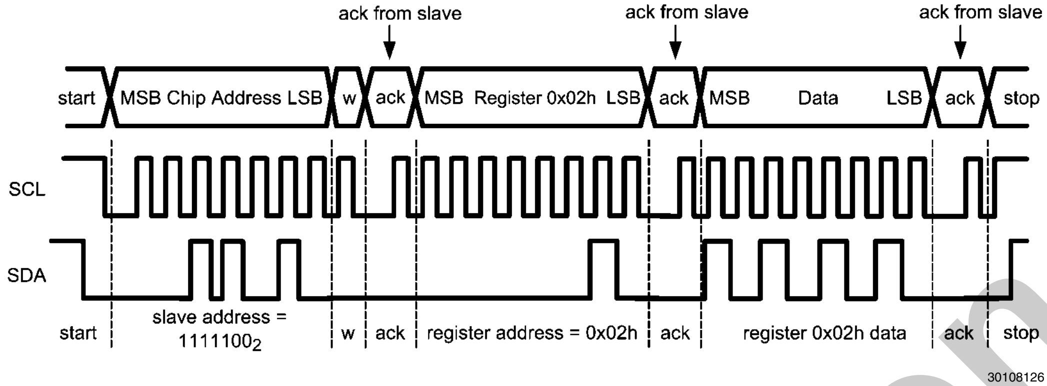
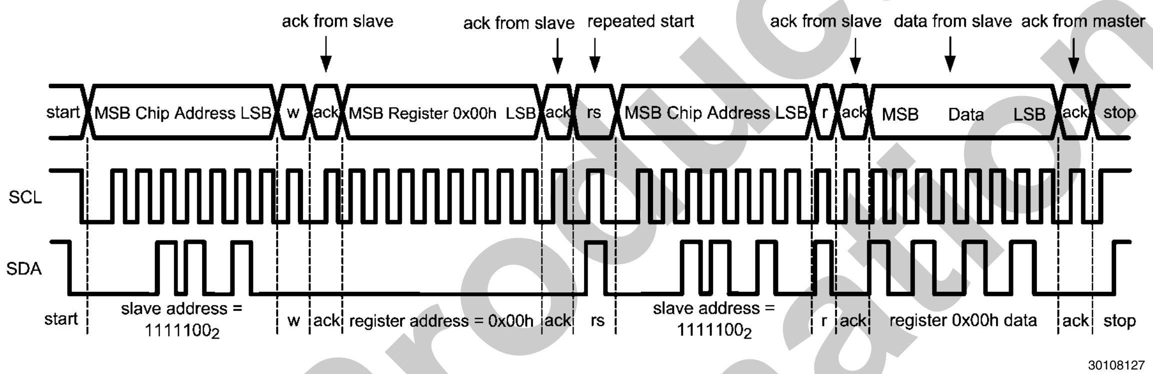


FIGURE 7. Example I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by slave)
rs = repeated start

FIGURE 8. Example I²C Read Cycle

Device Register Map

TABLE 2. Device Register Map

<table>
<tr><th>Address</th><th>Register</th><th>B7</th><th>B6</th><th>B5</th><th>B4</th><th>B3</th><th>B2</th><th>B1</th><th>B0</th></tr>
<tr><td>0x00h</td><td>SHUTDOWN</td><td>1</td><td>0</td><td>TURN_ON_TIME</td><td>AGC_ON</td><td>GAMP_SD</td><td>HPR_SD</td><td>I2C_VDD_SD</td><td>PWR_ON</td></tr>
<tr><td>0x01h</td><td>MIC</td><td>0</td><td>0</td><td colspan="2">MIC_SELECT</td><td>MIC2_ENB</td><td>MIC1_ENB</td><td>MIC2_MUTE</td><td>MIC1_MUTE</td></tr>
<tr><td>0x02h</td><td>MODE</td><td>1</td><td>AGC_MODE</td><td>EP_BYPASS_AGC</td><td>EP_ENB</td><td colspan="4">MODE_CONTROL</td></tr>
<tr><td>0x03h</td><td>VOLTAGE LIMITER</td><td>0</td><td>0</td><td>0</td><td colspan="2">ATTACK_TIME</td><td colspan="3">VOLTAGE_LEVEL</td></tr>
<tr><td>0x04h</td><td>NO CLIP</td><td>0</td><td>0</td><td>0</td><td colspan="2">RELEASE_TIME</td><td colspan="3">OUTPUT_CLIP_CONTROL</td></tr>
<tr><td>0x05h</td><td>GAIN</td><td>0</td><td>0</td><td>0</td><td>INPUT_MUTE</td><td>LS_GAIN</td><td colspan="3">HP_GAIN</td></tr>
<tr><td>0x06h</td><td>MONO VOLUME</td><td>0</td><td>0</td><td>0</td><td colspan="5">MONO_VOL</td></tr>
<tr><td>0x07h</td><td>STEREO VOLUME</td><td>0</td><td>0</td><td>0</td><td colspan="5">STEREO_VOL</td></tr>
<tr><td>0x08h</td><td>MIC GAIN</td><td>0</td><td>0</td><td>0</td><td>MIC_POSTGAIN</td><td colspan="4">MIC_PREGAIN</td></tr>
<tr><td>0x09h</td><td>EP</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>EP_LEVEL</td><td colspan="2">EP_INPUT_IMPEDANCE</td></tr>
<tr><td>0x0A</td><td>SS</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>ERC</td><td>SS_ENB</td></tr>
</table>

Shutdown Control Register

This register is used to control basic power management setup.

TABLE 3. Shutdown Control Register (0x00h)

<table>
<tr><th>Bit</th><th>Field</th><th colspan="2">Description</th></tr>
<tr><td rowspan="4">B0</td><td rowspan="4">PWR_ON</td><td colspan="2">This enables or disables the device.</td></tr>
<tr><td>PWR_ON</td><td>Status</td></tr>
<tr><td>0</td><td>Device disabled</td></tr>
<tr><td>1</td><td>Device enabled</td></tr>
<tr><td rowspan="4">B1</td><td rowspan="4">I^2CV_{DD}_SD</td><td colspan="2">If B2 = 0, I^2CV_{DD} acts as an active low reset input. If I^2CV_{DD} drops below 1.1V, the device resets and the I^2C registers are restored to their default state. By setting the bit I^2CV_{DD} does not reset the device</td></tr>
<tr><td>I^2CV_{DD}_SD</td><td>Status</td></tr>
<tr><td>0</td><td>Reset register if I^2CV_{DD} drops below 1.1V</td></tr>
<tr><td>1</td><td>Normal Operation</td></tr>
<tr><td rowspan="4">B2</td><td rowspan="4">HPR_SD</td><td colspan="2">This disables the right headphone output.</td></tr>
<tr><td>HPR_SD</td><td>Status</td></tr>
<tr><td>0</td><td>Normal operation</td></tr>
<tr><td>1</td><td>Headphone right disabled</td></tr>
<tr><td rowspan="4">B3</td><td rowspan="4">GAMP_SD</td><td colspan="2">This disables the gain amplifiers that are not in use to minimize I_{DD}. This setting is recommended for output modes 1, 2, 4, 5, 8, 10.</td></tr>
<tr><td>GAMP_SD</td><td>Status</td></tr>
<tr><td>0</td><td>Normal operation</td></tr>
<tr><td>1</td><td>Disable the unused gain amplifiers</td></tr>
<tr><td rowspan="4">B4</td><td rowspan="4">AGC_ON</td><td colspan="2">This enables or disables the AGC.</td></tr>
<tr><td>AGC_ON</td><td>Status</td></tr>
<tr><td>0</td><td>Enable of AGC function will depend on the AGC_MODE bit.</td></tr>
<tr><td>1</td><td>AGC is always turn on irrespective of the AGC_MODE bit.</td></tr>
<tr><td rowspan="4">B5</td><td rowspan="4">TURN_ON_TIME</td><td colspan="2">This control the turn on time of the device.</td></tr>
<tr><td>TURN_ON_TIME</td><td>Status</td></tr>
<tr><td>0</td><td>Normal turn on time (27ms)</td></tr>
<tr><td>1</td><td>Fast turn on time (15ms)</td></tr>
<tr><td>B6</td><td>NOT USED</td><td colspan="2">This bit is not used and should be 0.</td></tr>
<tr><td>B7</td><td>1</td><td colspan="2">This bit should be 1 when powering on the device in shutdown control register.</td></tr>
</table>

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MIC Control Register

This register is used to control basic microphones input setup.

TABLE 4. MIC Control Register (0x01h)

Bit	Field	Description	
B0	MIC1_MUTE	This mute the Microphone 1 input path.	
		MIC1_MUTE	Status
		0	MIC 1 is not in Mute
		1	MIC 1 is in Mute
B1	MIC2_MUTE	This mute the Microphone 2 input path.	
		MIC1_MUTE	Status
		0	MIC 2 is not in Mute
		1	MIC 2 is in Mute
B2	MIC1_ENB	This enables or disable the microphone 1 input path.	
		MIC1_ENB	Status
		0	Disable MIC 1
		1	Enable MIC 1
B3	MIC2_ENB	This enables or disable the microphone 2 input path.	
		MIC1_ENB	Status
		0	Disable MIC 2
		1	Enable MIC 2
B5:B4	MIC_SELECT	This selects the following microphone modes.	
		MIC_SELECT	Status
		00	Noise cancelling mode
		01	Only Mic 1 enabled (pass through)
		10	Only Mic 2 enabled (pass through)
		11	Mic1 + Mic2

Mode Control Register

This register is used to control the different mixer modes LM49155 supports:

TABLE 5. Output Mode Selection (see legend below) (0x02h)

Bits	Field	Description				
B3:B0	MODE _CONTROL	This sets the different mixers output modes.				
		MODE_ CONTROL	Mode	Loudspeaker	Headphone Left	Headphone Right
		0000	0	SD	SD	SD
		0001	1	GM x M	SD	SD
		0010	2	2 x (GL x L + GR x R)	SD	SD
		0011	3	2 x (GL x L + GR x R) + GM x M	SD	SD
		0100	4	SD	GM x M/2	GM x M/2
		0101	5	GM x M	GM x M/2	GM x M/2
		0110	6	2 x (GL x L + GR x R)	GM x M/2	GM x M/2
		0111	7	2 x (GL x L + GR x R) + GM x M	GM x M/2	GM x M/2
		1000	8	SD	GR x R	GL x L
		1001	9	GM x M	GR x R	GL x L
		1010	10	2 x (GL x L + GR x R)	GR x R	GL x L
		1011	11	2 x (GL x L + GR x R) + GM x M	GR x R	GL x L
		1100	12	SD	GR x R + GM x M/2	GL x L + GM x M/2
		1101	13	GM x M	GR x R + GM x M/2	GL x L + GM x M/2
		1110	14	2 x (GL x L + GR x R)	GR x R + GM x M/2	GL x L + GM x M/2
		1111	15	2 x (GL x L + GR x R) + GM x M	GR x R + GM x M/2	GL x L + GM x M/2
B4	EP_BYPASS	This makes the loudspeaker and headphone amplifiers into shutdown mode and enables receiver bypass path.				
		0	Normal output mode operation			
		1	Enable the receiver bypass path			
B5	EP_BYPASS _AGC	This enables the bypass path for earpiece output when AGC is on.				
		0	If AGC on, earpiece gain depends on AGC.			
		1	If AGC on, earpiece path bypass the AGC and has 0dB gain.			
B6	AGC_MODE	This enables or disables the AGC function.				
		0	Disable AGC function			
		1	Enable AGC function			
B7	1	This bit should be 1 when SNR Enhancer is enabled.				

M: Mono differential input
R: Right channel stereo input
L: Left channel stereo input
SD: Shutdown
GM: Differential input gain path
GR: Right channel input gain path
GL: Left Channel input gain path

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Voltage Limiter Control Register

This register is used to control output voltage limiter settings and attack time of automatic level circuit.

TABLE 6. Voltage Limit Control (0x03h)

Bits	Field	Description	
B2:B0	VOLTAGE _LEVEL	This sets the output voltage limit level.	
		000	Voltage limit disabled
		001	$V_{TH(VLIM)} = 4V_{P-P}$
		010	$V_{TH(VLIM)} = 4.8V_{P-P}$
		011	$V_{TH(VLIM)} = 5.6V_{P-P}$
		100	$V_{TH(VLIM)} = 6.4V_{P-P}$
		101	$V_{TH(VLIM)} = 7.2V_{P-P}$
		110	$V_{TH(VLIM)} = 8V_{P-P}$
		111	Voltage Limit disabled
B4:B3	ATTACK_TIME	This sets the attack time of automatic level control circuit. It is based on characterization data and C_{SET} = 0.1µF (see ATTACK TIME section).	
		00	0.75ms
		01	1ms
		10	1.5ms
		11	2ms

No Clip Control Register

This register is used to control output clip limit level settings and release time of automatic level circuit.

TABLE 7. No Clip Control (0x04h)

Bits	Field	Description	
B2:B0	OUTPUT_CLIP _LIMIT	This sets the output clip limit level.	
		000	No Clip disabled, output clip control disabled
		010	No Clip enabled
		011	Low
		100	Med
		101	High
B4:B3	RELEASE_TIME	This sets the release time of automatic level control circuit. It is based on characterization data and C_{SET} = 0.1µF (see RELEASE TIME section).	
		00	1s
		01	0.8s
		10	0.65s
		11	0.4s

Gain Control Register

This register is used to control gain level on the outputs and mute all the input into low power mode.

TABLE 8. Gain Control (0x05h)

Bits	Field	Description	
B2:B0	HP_GAIN	This sets the headphone output gain level.	
		HP_GAIN	Level (dB)
		000	0
		001	-1.5
		010	-3
		011	-6
		100	-9
		101	-12
		110	-15
		111	-18
B3	LS_GAIN	This sets the loudspeaker output gain level.	
		LS_GAIN	Level (dB)
		0	12dB
		1	18dB
B4	INPUT_MUTE	This enables all the inputs into low power mute mode.	
		0	Enabled
		1	Disabled

Volume Control Register

These registers are used to control input volume control levels for mono and stereo inputs.

TABLE 9. Mono and Stereo Volume (0x06h and 0x07h)

Bits	Field	Description	
B4:B0	MONO_VOL STEREO_VOL	This programs the mono and stereo inputs volume gain.	
		VOL	Level (dB)
		00000	MUTE
		00001	-46.5
		00010	-40.5
		00011	-34.5
		00100	-30
		00101	-27
		00110	-24
		00111	-21
		01000	-18
		01001	-15
		01010	-13.5
		01011	-12
		01100	-10.5
		01101	-9
		01110	-7.5
		01111	-6
		10000	-4.5
		10001	-3
		10010	1.5
		10011	0
		10100	1.5
		10101	3
		10110	4.5
		10111	6
		11000	7.5
		11001	9
		11010	10.5
		11011	12
		11100	13.5
		11101	15
		11110	16.5
		11111	18

MIC Gain Control Register

This register is used to control microphone pre-gain and post-gain levels.

TABLE 10. MIC Gain Control (0x08h)

Bits	Field	Description	
B3:B0	MIC_PREGAIN	This sets microphones pre-gain.	
		MIC_PREGAIN	Level (dB)
		0000	12
		0001	12
		0010	12
		0011	12
		0100	14
		0101	16
		0110	18
		0111	20
		1000	22
		1001	24
		1010	26
		1011	28
		1100	30
		1101	32
		1110	34
		1111	36
B4	MIC_POSTGAIN	This sets microphone post-gain in dB.	
		MIC_POSTGAIN	Level (dB)
		0	6
		1	12

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EP Control Register

This register is used to set earpiece input impedances and power levels.

TABLE 11. EP Control Register (0x09h)

Bits	Field	Description	
B1:B0	EP_INPUT _IMPEDANCE	This sets the earpiece input impedances.	
		00	40kΩ
		01	8.3kΩ
		10	5.7kΩ
B3	EP_PLEVEL	This sets the earpiece output power level.	
		0	50mW
		1	70mW

Spread Spectrum Control Register

This register controls the spread spectrum mode of the class D amplifier

TABLE 12. SS Control Register (0x0Ah)

Bits	Field	Description	
B0	SS_ENB	This sets the spread spectrum mode of the Class D amplifier.	
		0	Spread Spectrum Disabled
		1	Spread Spectrum Enabled
B1	ERC	This sets the edge rate control of class D amplifier.	
		0	Disabled
		1	Enabled

Application Information

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM49155 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM49155 can be used without input coupling capacitors when configured with a differential input signal.

INPUT MIXER/MULTIPLEXER

The LM49155 includes a comprehensive mixer multiplexer controlled through the I²C interface. The mixer/multiplexer allows any input combination to appear on any output of LM49155. Multiple input paths can be selected simultaneously. Under these conditions, the selected inputs are mixed together and output on the selected channel. Table 5 (MODE CONTROL) shows how the input signals are mixed together for each possible input selection.

SHUTDOWN FUNCTION

The LM49155 features the following shutdown controls: Bit B4 (GAMP_SD) of the SHUTDOWN CONTROL register controls the gain amplifiers. When GAMP_SD = 1, it disables the gain amplifiers that are not in use. For example, in Modes 1, 4 and 5, the Mono inputs are in use, so the Left and Right input gain amplifiers are disabled, causing the I_{DD} to be minimized. Bit B0 (PWR_ON) of the SHUTDOWN CONTROL register is the global shutdown control for the entire device. Set PWR_ON = 0 for normal operation. PWR_ON = 1 overrides any other shutdown control bit.

CLASS D AMPLIFIER

The LM49155 features a mono class D audio power amplifier with a filterless modulation scheme that reduces external component count, conserving board space and reducing system cost. With no signal applied, the outputs (LSOUT+ and LSOUT-) switch between VDD and GND with 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

With an input signal applied, the duty cycle (pulse width) of the class D output changes. For increasing output voltage, the duty cycle of LSOUT+ increases, while the duty cycle of LSOUT- decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yields the differential output voltage.

ENHANCED EMISSIONS SUPPRESSION (E²S)

The LM49155 class D amplifier features National's patent-pending E²S system that reduces EMI, while maintaining high quality audio reproduction and efficiency. The E²S system features selectable spread spectrum and advanced edge rate control (ERC). The LM49155 class D ERC greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduces RF emissions, while maximizing THD+N and efficiency performance.

FIXED FREQUENCY

The LM49155 class D amplifier features two modulation schemes, a fixed frequency mode and a spread spectrum mode. Select the fixed frequency mode by setting bit B0 (SS_EN) of the SS Control register to 0. In fixed frequency mode, the loudspeaker outputs switch at a constant 300kHz. The output spectrum consists of the 300kHz fundamental and its associated harmonics.

SPREAD SPECTRUM

The selectable spread spectrum mode minimizes the need for output filters, ferrite beads or chokes. In spread spectrum mode, the switching frequency varies randomly by 30% about a 300kHz center frequency, reducing the wideband spectral content, improving EMI emission radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR. Set bit B0 (SS_EN) of the SS Control register to 1 to enable spread spectrum mode.

GROUND REFERENCED HEADPHONE AMPLIFIER

The LM49155 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the headphone outputs to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two small ceramic charge pump capacitors, saving board space and cost. Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor from a high-pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM49155 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components. In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM49155 headphone amplifiers when compared to a traditional headphone amplifier operating from the same supply voltage.

AUTOMATIC LIMITER CONTROL (ALC)

When enabled, the ALC continuously monitors and adjusts the gain of the loudspeaker amplifier signal path if necessary. The ALC serves two functions: voltage limiter/speaker protection and output clip prevention (No-Clip) with three clip controls levels. The voltage limiter/speaker protection prevents an output overload condition by maintaining the loudspeaker output signal below a preset amplitude (See voltage Limiter section). The No Clip feature monitors the output signal and maintains audio quality by preventing the loudspeaker output from exceeding the amplifier's headroom (see No Clip/ Output Clip Control section). The voltage limiter thresholds, clip control levels, attack and release times are configured through the I²C interface.

VOLTAGE LIMITER

The voltage limiter function of the ALC monitors and prevents the audio signal from exceeding the voltage limit threshold (*Figure 9*). The voltage limit threshold ($V_{TH(VLIM)}$) is set by bits B2:B0 in the Voltage Limit Threshold Register (see table 6). Although the ALC reduces the gain of the speaker path to maintain the audio signal below the voltage limit threshold, it is still possible to overdrive the speaker output in which case loudspeaker output will exceed the voltage limit threshold and cause clipping on the output, and speaker damage is possible. Please see the ALC headroom section for further details.

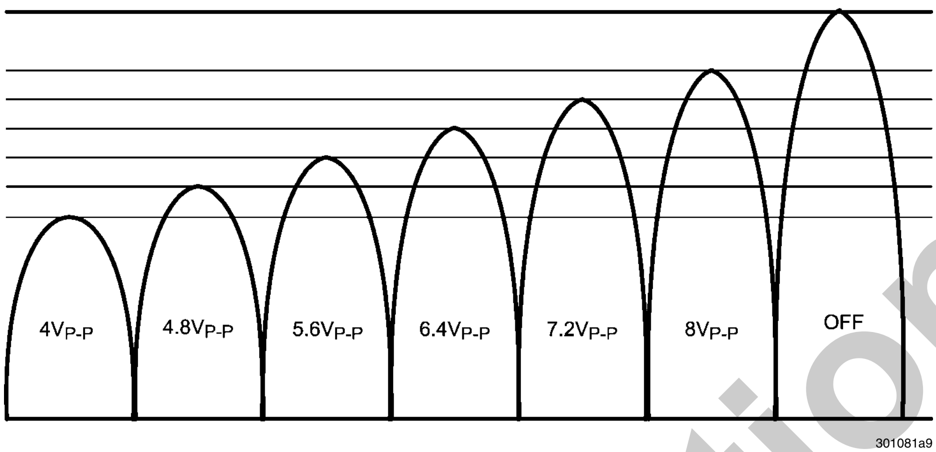

FIGURE 9. Voltage Limit Output Level

NO CLIP/OUTPUT CLIP CONTROL

The LM49155 No Clip circuitry detects when the loudspeaker output is near clipping and reduces the signal gain to prevent output clipping and preserve audio quality (Figure 6). Although the ALC reduces the gain of the speaker path to prevent output clipping, it is still possible to overdrive the speaker output. Please see the ALC headroom section for further details.

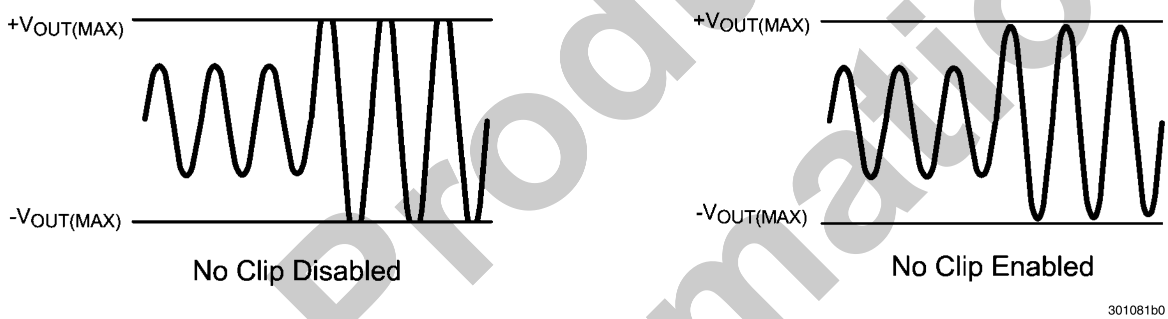

FIGURE 10. No Clip Function

The LM49155 also features an output clip control that allows a certain amount of clipping at the output in order to increase the loudspeaker output power. The clip level is set by B2:B0 in the No Clip Control Register (see Table 7). The clip control works by allowing the output to enter clipping before the ALC turns on and maintains the output level. The clip control has three levels: low, medium, and high. The low and max clip level control settings give the lowest distortion and highest distortion respectively on the output (see *Figure 11*). The actual output level of the device will depend upon the supply voltage, and the output power will depend upon the load impedance.

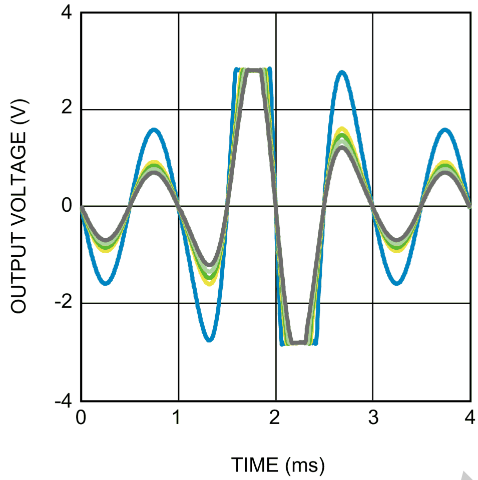

FIGURE 11. Clip Control Levels
V_{DD} = 3.3V, V_{IN} = 8V_{PP} Shaped Burst, 1kHz
Blue = No Clip Disabled, Gray = Low, Light Green = Medium
Green = High, Yellow = Max

ALC HEADROOM

When either voltage limiter or no clip is enabled, it is still possible to drive LM49155 into clipping by over driving the input volume stage of the signal path beyond its output dynamic range. In this case, clipping occurs at the input volume stage, and although ALC is active, the gain reduction will have no effect on the output clipping. The maximum input that can safely pass through the input volume stage can be calculated by following formula:

$$V_{IN} \leq \frac{V_{DD}}{Av\ (\text{volume gain})} \quad (1)$$

So in the case of 0 dB volume gain, audio input has to be less than V_{DD} for both voltage limiter or No clip settings.

When voltage limiter is enabled, ALC can reach its max attenuation for lower voltage limit levels as shown in *Figure 12*. Typically, after the ALC started working, with 6 dB of audio input change ALC is well within its regulation. Voltage limiter Input headroom can be increased by switching to the LS_GAIN to 18dB in the Gain Control Register (see *Table 8*).

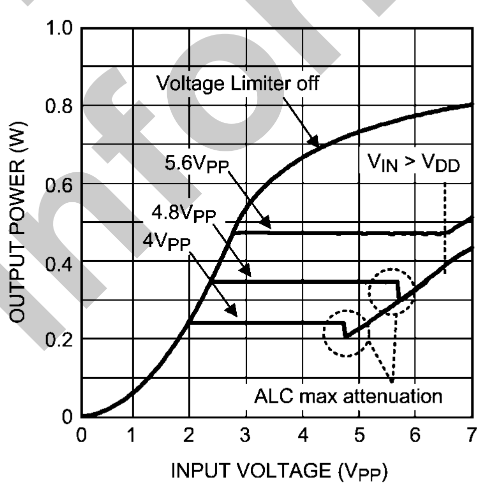

FIGURE 12. Voltage Limiter Function
V_{DD} = 3.3V, R_L = 15µH+8Ω+15µH
f_{IN} = 1kHz, LS_GAIN = 0

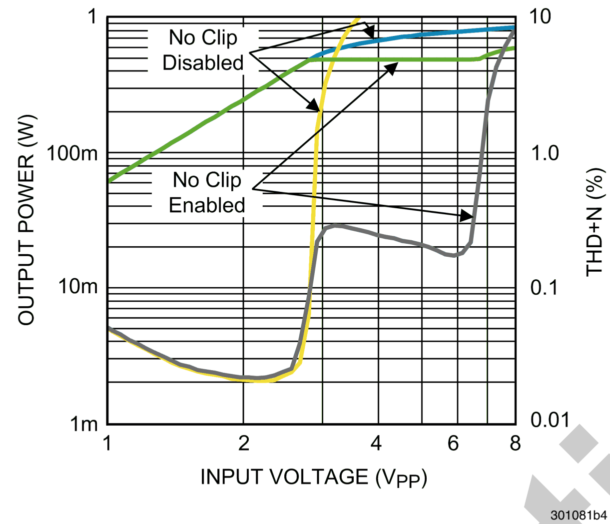

FIGURE 13. No Clip Function
V_{DD} = 3.3V, R_L = 15μH+8Ω+15μH
f_{IN} = 1kHz, LS_GAIN = 0
Blue, Green = Output Power vs Input Voltage
Gray, Yellow = THD+N vs Input Voltage

When No Clip is enabled, class D speaker output reduces when it's about to enter clipping region and power stay constant as long as V_{IN} is less than V_{DD} for 0 dB volume gain (see figure 9). For example, in the case of V_{DD} = 3.3V, there is a 6 dB of headroom for the change in input. Please see the ALC typical performance curves for additional plots relating to different supply voltages and LS_GAIN settings for specific application parameters.

ATTACK TIME

Attack time (t_{ATK}) is the time it takes for the gain to be reduced by 6dB (LS_GAIN=0) once the audio signal exceeds the ALC threshold. Fast attack times allow the ALC to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the ALC cycles quickly. Slower attack times cause the ALC to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function, and possible output overload conditions in the case of the Voltage limiter. The attack time is set by a combination of the value of C_{SET} and the attack time coefficient as given by equation (2):

$$t_{ATK} = 20k\Omega C_{SET} / \alpha_{ATK} \quad (s) \qquad (2)$$

Where α_{ATK} is the attack time coefficient (*Table 13*) set by bits B4:B3 in the Voltage Limit Control Register (see *Table 6*). The attack time coefficient allows the user to set a nominal attack time. The internal 20kΩ resistor is subject to temperature change, and it has tolerance between -11% to +20%.

TABLE 13. Attack Time Coefficient

B4	B3	α_{ATK}
0	0	2.667
0	1	2
1	0	1.333
1	1	1

RELEASE TIME

Release time (t_{RL}) is the time it takes for the gain to return from 6dB (LS_GAIN=0) to its normal level once the audio signal returns below the ALC threshold. A fast release time allows the ALC to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. The release time is set by a combination of the value of C_{SET} and release time coefficient as given by equation (3):

$$t_{RL} = 20M\Omega C_{SET} / \alpha_{RL} \quad (s) \qquad (3)$$

where α_{RL} is the release time coefficient (*Table 14*) set by bits B4:B3 in the No Clip Control Register. The release time coefficient allows the user to set a nominal release time. The internal 20MΩ is subject to temperature change, and it has tolerance between -11% to +20%.

TABLE 14. Release Time Coefficient

B4	B3	α_{RL}
0	0	2
0	1	2.5
1	0	3
1	1	5

UPLINK FAR-FIELD NOISE REDUCTION OVERVIEW

The uplink portion of the LM49155 is a fully analog solution to reduce the far field noise picked up by microphones in a communication system. A simplified block diagram is provided in *Figure 14*.

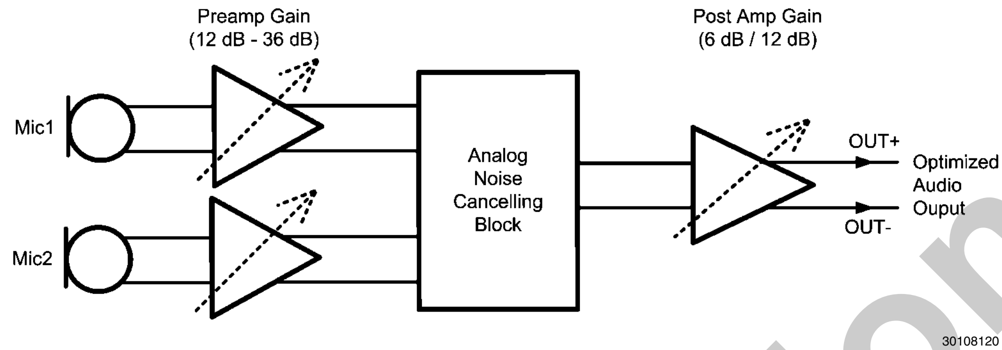

FIGURE 14. Simplified Block Diagram of the LM49155 Uplink path

The output signal of the microphones is amplified by a preamplifier with adjustable gain between 12dB and 36dB. The matched signals are then routed through the Analog Noise Cancelling block which suppresses the far-field signal. The output of the analog noise cancelling processor is amplified in the post amplifier with selectable gain, 6dB or 12dB. For optimum noise and EMI immunity, the microphones have a differential connection to the LM49155 and the uplink output is also differential. The adjustable gain functions can be controlled via I²C.

GAIN BALANCE AND GAIN BUDGET

In systems where input signals have a high dynamic range, critical noise levels or where the dynamic range of the output voltage is also limited, careful gain balancing is essential for the best performance. Too low of a gain setting in the preamplifier can result in higher noise levels, while too high of a gain setting in the preamplifier will result in saturation of the noise cancelling processor and output stages.

The gain ranges and maximum signal levels for the different functional blocks are shown in *Figure 15*. Two examples are given as a guideline on how to select proper gain settings.

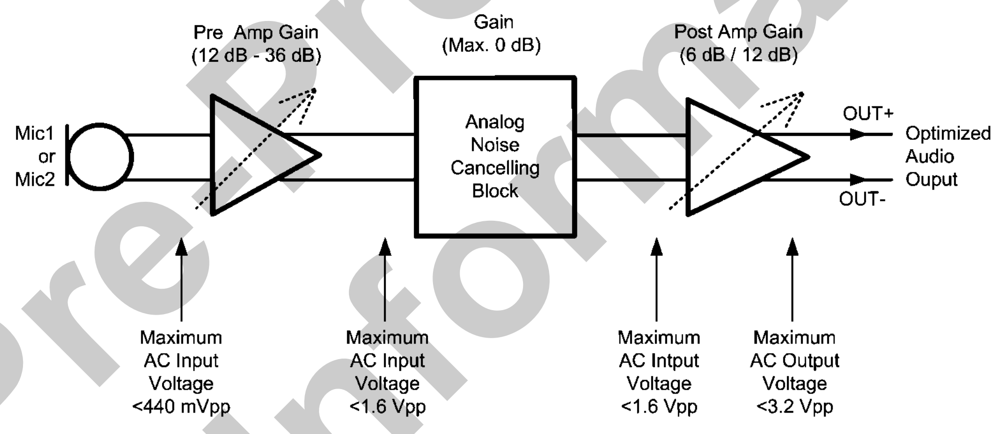

FIGURE 15. Maximum Signal Levels

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Example 1:

An application using microphones with $50mV_{P-P}$ maximum output voltage, and a baseband chip after the LM49155 with $1.5V_{P-P}$ maximum input voltage.

For optimum noise performance, the gain of the input stage should be set to the maximum.

1. $50mV_{P-P} + 36dB = 3.1V_{P-P}$.
2. $3.1V_{P-P}$ is higher than the maximum $1.5V_{P-P}$ allowed for the Noise Cancelling Block (NCB). This means a gain lower than 29.5dB should be selected.
3. Select the nearest lower gain from the gain settings shown in *Table 10*, 28dB is selected. This will prevent the Noise Cancelling block from being overloaded by the microphone. With this setting, the resulting output level of the Pre Amplifier will be $1.26V_{P-P}$.
4. The NCB has a gain of 0dB which will result in $1.26V_{P-P}$ at the output of the LM49155. This level is less than the maximum level that is allowed at the input of the post amp of the LM49155.
5. The baseband chip limits the maximum output voltage to $1.5V_{P-P}$ with the minimum of 6dB post amp gain, this results in requiring a lower level at the input of the post amp of $0.75V_{P-P}$. Now calculating this for a maximum preamp gain, the output of the preamp must be no more than $0.75mV_{P-P}$.
6. Calculating the new gain for the preamp will result in <23.5dB gain.
7. The nearest lower gain will be 22dB.

So using preamp gain = 22dB and postamp gain = 6dB is the optimum for this application.

Example 2:

An application using microphones with $10mV_{P-P}$ maximum output voltage, and a baseband chip after the LM49155 with $3.3V_{P-P}$ maximum input voltage.

For optimum noise performance we would like to have the maximum gain at the input stage.

1. $10mV_{P-P} + 36dB = 631mV_{P-P}$.
2. This is lower than the maximum $1.5V_{P-P}$, so this is OK.
3. The Noise Cancelling block has a gain of 0dB which will result in $1.5V_{P-P}$ at the output of the LM49155. This level is lower than the maximum level that is allowed at the input of the Post Amp of the LM49155.
4. With a Post Amp gain setting of 6dB the output of the Post Amp will be $3V_{P-P}$ which is OK for the baseband.
5. The nearest lower Post Amp gain will be 6dB.

So using preamp gain = 36dB and postamp gain = 6dB is optimum for this application.

MICROPHONE MODE CONTROL

The LM49155 features 4 Microphone modes, Noise Cancellation Mode, Mic 1 pass through, Mic 2 pass through, and (Mic1+Mic2)/2. When in Noise Cancellation mode, it is imperative that Mic 1 and Mic 2 are NOT muted. If the mute function for either microphone path is enabled, the noise cancellation circuitry will be disabled. In mic1/mic2 pass through mode the noise canceling block is bypassed, and the LM49155 is simply used as a microphone amplifier where the microphone signal passes through the pre and post amplifier gain stages. The last mode provides an average of the two microphone pass through signals (noise cancelling block is bypassed).

The microphone input paths can be muted individually via I²C (Mic control register B1:B0). To enable the mute function, set bit B2 of the microphone mode control register to 1. If B2 is set to 0, the mute function will not activate.

SIGNAL-TO-NOISE RATIO (SNR) ENHANCER

The SNR Enhancer in the LM49155 is designed to provide excellent voice intelligibility in noisy environments. The control signal for the output gain adjustment is dependent on both the level and the type of ambient noise, compared with the signal energy of the downlink voice. The system was designed to operate transparently to the user, such that the gain changes are not evident but provide excellent voice intelligibility.

SNR ENHANCER BYPASS (EP_BYPASS_AGC)

The SNR enhancer can be bypassed by setting B5 of the Mode Control Register to 1. When the SNR enhancer is bypassed, the earpiece amplifier has a fixed 0dB gain.

EP_RI (INPUT IMPEDANCE)

The earpiece input of the LM49155 features three input impedance options, this impedance in conjunction with the input capacitor creates a high-pass filter. The three options provide various cutoff frequencies for the high-pass filter. *Table 15* shows the respective cutoff frequencies for each of the input impedance options when using a 68nF input capacitor.

TABLE 15. Input Impedance options

Input Impedance	f_C
40kΩ	59Hz
8.3kΩ	282Hz
5.7kΩ	411Hz

MICROPHONE PLACEMENT

Because the LM49155 is a microphone array Far Field Noise Reduction solution, proper microphone placement is critical for optimum performance. Two things need to be considered: The spacing between the two microphones and the position of the two microphones relative to near field source

If the spacing between the two microphones is too small near field speech will be canceled along with the far field noise. Conversely, if the spacing between the two microphones is large, the far field noise reduction performance will be degraded. The optimum spacing between mic1 and mic2 is 1.5-2.5cm. This range provides a balance of minimal near field speech loss and maximum far field noise reduction. The microphones should be in line with the desired sound source 'near speech' and configured in an endfire array (see *Figure 17*) orientation from the sound source. If the 'near speech' (desired sound source) is equidistant to the source like a broadside array (see *Figure 16*) the result will be a great deal of near field speech loss.

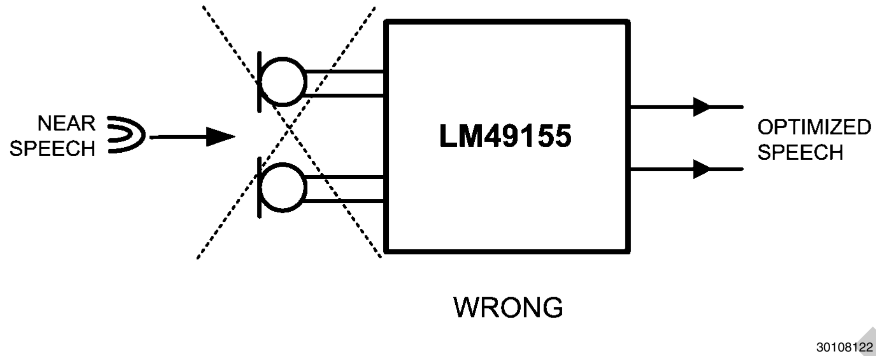


FIGURE 16. Broadside Array (WRONG)

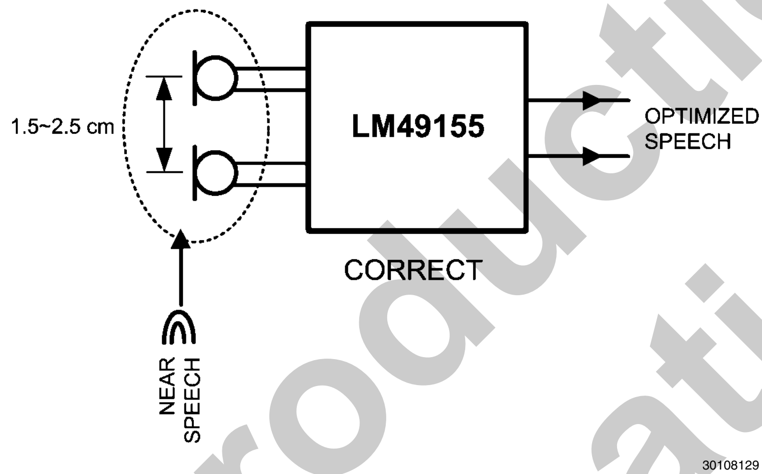


FIGURE 17. Endfire Array (CORRECT)

LOW-PASS FILTER AT THE OUTPUT

At the output of the LM49155 there is a provision to create a 1st order low-pass filter (only enabled in 'Noise Cancelling' mode). This low-pass filter can be used to compensate for the change in frequency response that results from the noise cancellation process. The change in frequency response resembles a first-order high-pass filter, and for many of the applications it can be compensated by a first-order low-pass filter with cutoff frequency between 1.5kHz and 2.5kHz.

The transfer function of the low-pass filter is derived as:

$$H(s) = \frac{\text{Post Amplifier gain}}{sR_fC_f+1}$$

This low-pass filter is created by connecting a capacitor between the LPF pin and the OUT pin of the LM49155. The value of this capacitor also depends on the selected output gain. For different gains the feedback resistance in the low-pass filter network changes as shown in *Table 16*.

This will result in the following values for a cutoff frequency of 2000 Hz:

TABLE 16. Low-Pass Filter Capacitor For 2kHz

Post Amplifier Gain Setting (dB)	R_f (kΩ)	C_f (nF)
6	20	3.9
9	29	2.7
12	40	2.0
15	57	1.3
181	80	1.0

A-WEIGHTED FILTER

The human ear is sensitive for acoustic signals within a frequency range from about 20Hz to 20kHz. Within this range the sensitivity of the human ear is not equal for each frequency. To approach the hearing response, weighting filters are introduced. One of those filters is the A-weighted filter.

The A-weighted filter is used in signal to noise measurements, where the wanted audio signal is compared to device noise and distortion.

The use of this filter improves the correlation of the measured values to the way these ratios are perceived by the human ear.

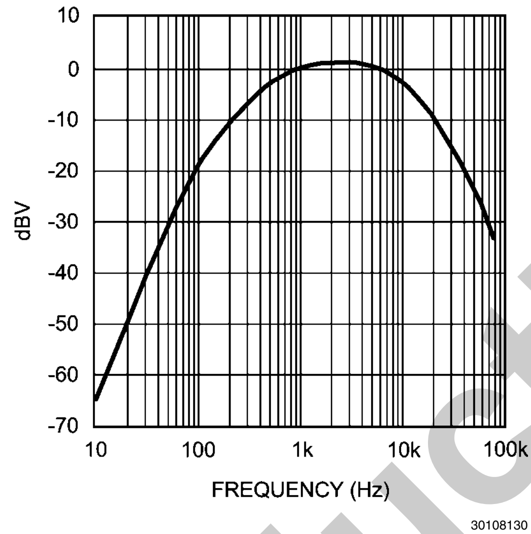


FIGURE 18. A-Weighted Filter

PROPER SELECTION OF EXTERNAL COMPONENTS

ALC Timing (C_{SET}) Capacitor Selection

The recommended range value of C_{SET} is between .01µF to 1µF. Lowering the value below .01µF can increase the attack time but LM49155 ALC ability to regulate its output can be disrupted and approaches the hard limiter circuit. This in turn increases the THD+N and audio quality will be severely affected.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C_1)

The flying capacitor (C_1), see Figure 1, affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the RDS(ON) of the charge pump switches and the ESR of C1 and CPV_{SS} dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Charge Pump Hold Capacitor (CPV_{SS})

The value and ESR of the hold capacitor (CPV_{SS}) directly affects the ripple on CPV_{SS}. (see figure 1) Increasing the value of CPV_{SS} reduces output ripple. Decreasing the ESR of CPV_{SS} reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49155. The input capacitors create a high-pass filter with the input resistors RIN. The -3dB point of the high-pass filter is found using Equation (4) below.

$$f = 1/\,2\pi R_{IN}C_{IN} \quad \text{(Hz)} \tag{4}$$

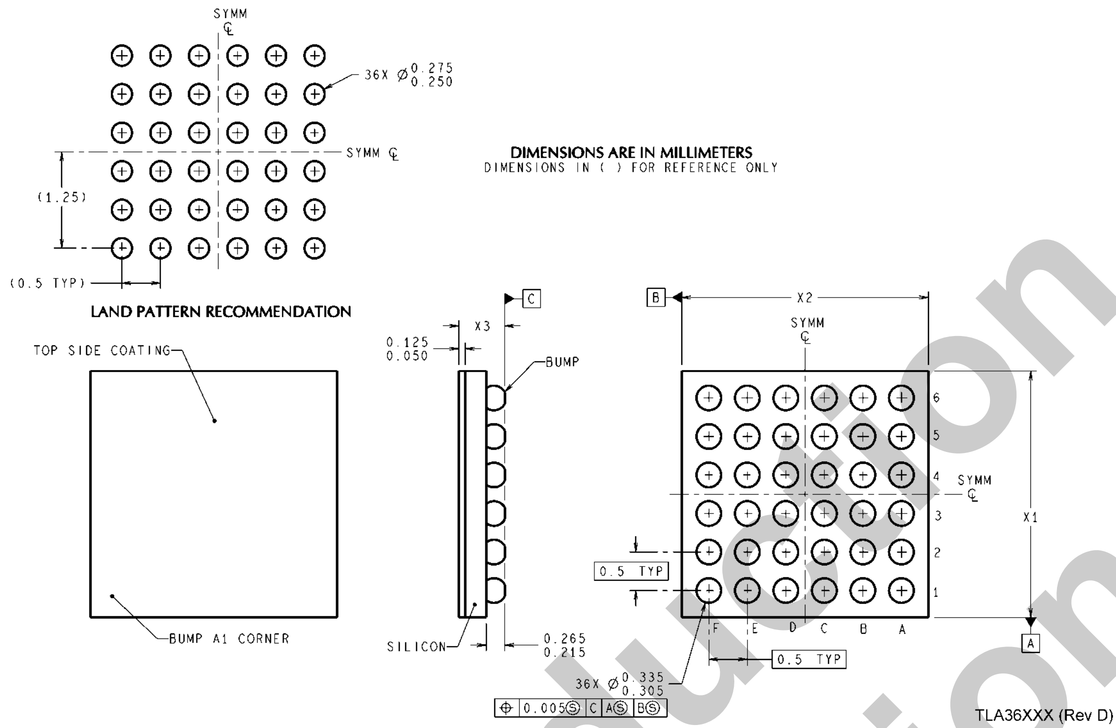
Where the value of R_{IN} is given in the Electrical Characteristics Table.

High-pass filtering the audio signal helps protect the speakers. When the LM49155 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

Revision History

Rev	Date	Description
0.01	11/10/09	Initial PDF.
0.02	01/22/10	Text edits.
0.03	02/04/10	Added he Top Marking instructions and input text edits.
0.04	02/17/10	Text edits.
0.05	03/04/10	Text edits.
0.06	03/24/10	Text edits.
0.07	05/24/10	Text edits.
0.08	05/28/10	Input text edits.
0.09	06/01/10	Deleted the Limit values on Vos (Headphone Amplifier) section in the EC table.
0.10	06/03/10	Input text edits.
0.11	06/07/10	Added the Efficiency vs Output Power graphs.
0.12	06/09/10	Input text edits.
0.13	06/11/10	Added the PSRR vs Freq curves.
0.14	06/16/10	Added more curves, PSRR vs Frequency.
0.15	06/28/10	Input edits on Input Voltage (under Absolute Maximum Ratings.
0.16	07/01/10	Input text edits on Table 7 (No Clip Control).
0.17	07/09/10	Text edits.
0.18	07/22/10	Input major text edits.
0.19	07/26/10	Input text edits.

Physical Dimensions inches (millimeters) unless otherwise noted



micro SMD–36 Package
Order Number LM49155TL
NS Package Number TLA36STA
X_1 = 3.343mm, X_2 = 3.459mm, X_3= 0.600mm,

Notes

Notes

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