TAS5538 Register Map

Please refer to TAS5538 data sheet for the detailed setting.

*R : Read, W : Write, SB : Sticky Bits(Write Zero Only), N/A : Not Available

*If you need to write unused bits, you must write default values to them.

Sub-address	Total Bytes	Register Name	Default	Permission
0x00	1	Clock Control Register (48K,MCK=256)	0x6C	R/W
0x01	1	General Status Register	0x03	R
0x02	1	Error Status Register	0x00	R/SB
0x03	1	System Control Reg1	0xB0	R/W
0x04	1	System Control Reg2	0x03	R/W
0x05	1	Channel Config Reg1	0xE0	R/W
0x06	1	Channel Config Reg2	0xE0	R/W
0x07	1	Channel Config Reg3	0xE0	R/W
0x08	1	Channel Config Reg4	0xE0	R/W
0x09	1	Channel Config Reg5	0xE0	R/W
0x0A	1	Channel Config Reg6	0xE0	R/W
0x0B	1	Channel Config Reg7	0xE0	R/W
0x0C	1	Channel Config Reg8	0xE0	R/W
0x0D	1	Headphone Config Reg	0x00	R/W
0x0E	1	Serial Data Interface Reg	0x55	R/W
0x0F	1	Soft Mute Reg	0x00	R/W
0x10	1	EMO Status Register	0x0A	R/SB
0x11	1	Reserved	-	N/A
0x12	1	OSC_TRIM	0x82	R/W
0x13	1	Reserved	-	N/A
0x14	1	Automute Control	0x44	R/W
0x15	1	Automute PWM Threshold & Backend Reset Period	0x02	R/W
0x16	1	Modulation Limit Reg(ch1 & 2)	0x77	R/W
0x17	1	Modulation Limit Reg(ch3 & 4)	0x77	R/W
0x18	1	Modulation Limit Reg(ch5 & 6)	0x77	R/W
0x19	1	Modulation Limit Reg(ch7 & 8)	0x77	R/W
0x1B	1	IC Delay Channel 0	0x80	R/W
0x1C	1	IC Delay Channel 1	0x00	R/W
0x1D	1	IC Delay Channel 2	0xC0	R/W

0x1E	1	IC Delay Channel 3	0x40	R/W
0x1F	1	IC Delay Channel 4	0xA0	R/W
0x20	1	IC Delay Channel 5	0x20	R/W
0x21	1	IC Delay Channel 6	0xE0	R/W
0x22	1	IC Delay Channel 7	0x60	R/W
0x23	1	IC Offset	0x00	R/W
0x24	1	PWM sequence timing	0x0F	R/W
0x25	1	PWM and EMO Control Register	0x80	R/W
0x26	1	Reserved	-	N/A
0x27	1	Individual Channel Shutdown	0x00	R/W
0x28	1	Reserved	-	N/A
0x29	1	Reserved	-	N/A
0x2A	1	Reserved	-	N/A
0x2B	1	Reserved	-	N/A
0x2C	1	Reserved	-	N/A
0x2D	1	Reserved	-	N/A
0x2E	1	Reserved	-	N/A
0x2F	1	Reserved	-	N/A
0x30	1	Input_Mux_ch1&2	0x01	R/W
0x31	1	Input_Mux_ch3&4	0x23	R/W
0x32	1	Input_Mux_ch5&6	0x45	R/W
0x33	1	Input_Mux_ch7&8	0x67	R/W
0x34	1	PWM_mux_ch1&2	0x01	R/W
0x35	1	PWM_mux_ch3&4	0x23	R/W
0x36	1	PWM_mux_ch5&6	0x45	R/W
0x37	1	PWM_mux_ch7&8	0x67	R/W
0x38	1	IC Delay Channel 0(BD)	0x80	R/W
0x39	1	IC Delay Channel 1(BD)	0x00	R/W
0x3A	1	IC Delay Channel 2(BD)	0xC0	R/W
0x3B	1	IC Delay Channel 3(BD)	0x40	R/W
0x3C	1	IC Delay Channel 4(BD)	0xA0	R/W
0x3D	1	IC Delay Channel 5(BD)	0x20	R/W
0x3E	1	IC Delay Channel 6(BD)	0xE0	R/W
0x3F	1	IC Delay Channel 7(BD)	0x60	R/W
0x40	4	Bank-switching Command Register	0000 0000	R/W
0x41	32	Input Mixer Register Ch1 – Ch8 A_to_ipmix[1]	0080 0000	R/W

		B_to_ipmix[1]	0000 0000	
		C_to_ipmix[1]	0000 0000	
		D_to_ipmix[1]	0000 0000	
		E_to_ipmix[1]	0000 0000	
		F_to_ipmix[1]	0000 0000	
		G_to_ipmix[1]	0000 0000	
		H_to_ipmix[1]	0000 0000	
0x42	32	Input Mixer Register Ch1 – Ch8		R/W
		A_to_ipmix[2]	0000 0000	
		B_to_ipmix[2]	0080 0000	
		C_to_ipmix[2]	0000 0000	
		D_to_ipmix[2]	0000 0000	
		E_to_ipmix[2]	0000 0000	
		F_to_ipmix[2]	0000 0000	
		G_to_ipmix[2]	0000 0000	
		H_to_ipmix[2]	0000 0000	
0x43	32	Input Mixer Register Ch1 – Ch8		R/W
		A_to_ipmix[3]	0000 0000	
		B_to_ipmix[3]	0000 0000	
		C_to_ipmix[3]	0080 0000	
		D_to_ipmix[3]	0000 0000	
		E_to_ipmix[3]	0000 0000	
		F_to_ipmix[3]	0000 0000	
		G_to_ipmix[3]	0000 0000	
		H_to_ipmix[3]	0000 0000	
0x44	32	Input Mixer Register Ch1 – Ch8		R/W
		A_to_ipmix[4]	0000 0000	
		B_to_ipmix[4]	0000 0000	
		C_to_ipmix[4]	0000 0000	
		D_to_ipmix[4]	0080 0000	
		E_to_ipmix[4]	0000 0000	
		F_to_ipmix[4]	0000 0000	
		G_to_ipmix[4]	0000 0000	
		H_to_ipmix[4]	0000 0000	
0x45	32	Input Mixer Register Ch1 – Ch8		R/W
		A_to_ipmix[5]	0000 0000	
		B_to_ipmix[5]	0000 0000	
		C_to_ipmix[5]	0000 0000	

		D_to_ipmix[5]	0000 0000	
		E_to_ipmix[5]	0080 0000	
		F_to_ipmix[5]	0000 0000	
		G_to_ipmix[5]	0000 0000	
		H_to_ipmix[5]	0000 0000	
0x46	32	Input Mixer Register Ch1 – Ch8		R/W
		A_to_ipmix[6]	0000 0000	
		B_to_ipmix[6]	0000 0000	
		C_to_ipmix[6]	0000 0000	
		D_to_ipmix[6]	0000 0000	
		E_to_ipmix[6]	0000 0000	
		F_to_ipmix[6]	0080 0000	
		G_to_ipmix[6]	0000 0000	
		H_to_ipmix[6]	0000 0000	
0x47	32	Input Mixer Register Ch1 – Ch8		R/W
		A_to_ipmix[7]	0000 0000	
		B_to_ipmix[7]	0000 0000	
		C_to_ipmix[7]	0000 0000	
		D_to_ipmix[7]	0000 0000	
		E_to_ipmix[7]	0000 0000	
		F_to_ipmix[7]	0000 0000	
		G_to_ipmix[7]	0080 0000	
		H_to_ipmix[7]	0000 0000	
0x48	32	Input Mixer Register Ch1 – Ch8		R/W
		A_to_ipmix[8]	0000 0000	
		B_to_ipmix[8]	0000 0000	
		C_to_ipmix[8]	0000 0000	
		D_to_ipmix[8]	0000 0000	
		E_to_ipmix[8]	0000 0000	
		F_to_ipmix[8]	0000 0000	
		G_to_ipmix[8]	0000 0000	
		H_to_ipmix[8]	0080 0000	
0x49	4	r_ipmix_1_to_ch8	0000 0000	R/W
0x4A	4	r_ipmix_2_to_ch8	0000 0000	R/W
0x4B	4	r_ipmix_7_to_ch2	0000 0000	R/W
0x4C	4	r_ch7_bp_bq2	0000 0000	R/W
0x4D	4	r_ch7_bq2	0080 0000	R/W
0x4E	4	r_ipmix_8_to_ch1,2	0000 0000	R/W

0x4F	4	r_ch8_bp_bq2	0000 0000	R/W
0x50	4	Biquad filter register r_ch8_bq2	0080 0000	R/W
0x51 – 0x57	20/Register	Biquad filter register Ch1_bq[1:7]		R/W
		b_0 coefficient	0080 0000	
		b_1 coefficient	0000 0000	
		b_2 coefficient	0000 0000	
		a_1 coefficient	0000 0000	
		a_2 coefficient	0000 0000	
0x58 – 0x5E	20/Register	Biquad filter register Ch2_bq[1:7]		R/W
		b_0 coefficient	0080 0000	
		b_1 coefficient	0000 0000	
		b_2 coefficient	0000 0000	
		a_1 coefficient	0000 0000	
		a_2 coefficient	0000 0000	
0x5F – 0x65	20/Register	Biquad filter register Ch3_bq[1:7]		R/W
		b_0 coefficient	0080 0000	
		b_1 coefficient	0000 0000	
		b_2 coefficient	0000 0000	
		a_1 coefficient	0000 0000	
		a_2 coefficient	0000 0000	
0x66 – 0x6C	20/Register	Biquad filter register Ch4_bq[1:7]		R/W
		b_0 coefficient	0080 0000	
		b_1 coefficient	0000 0000	
		b_2 coefficient	0000 0000	
		a_1 coefficient	0000 0000	
		a_2 coefficient	0000 0000	
0x6D – 0x73	20/Register	Biquad filter register Ch5_bq[1:7]		R/W
		b_0 coefficient	0080 0000	
		b_1 coefficient	0000 0000	
		b_2 coefficient	0000 0000	
		a_1 coefficient	0000 0000	
		a_2 coefficient	0000 0000	
0x74 – 0x7A	20/Register	Biquad filter register Ch6_bq[1:7]		R/W
		b_0 coefficient	0080 0000	
		b_1 coefficient	0000 0000	
		b_2 coefficient	0000 0000	
		a_1 coefficient	0000 0000	
		a_2 coefficient	0000 0000	

0x7B – 0x81	20/Register	Biquad filter register Ch7_bq[1:7]		R/W
		b_0 coefficient	0080 0000	
		b_1 coefficient	0000 0000	
		b_2 coefficient	0000 0000	
		a_1 coefficient	0000 0000	
		a_2 coefficient	0000 0000	
0x82 – 0x88	20/Register	Biquad filter register Ch8_bq[1:7]		R/W
		b_0 coefficient	0080 0000	
		b_1 coefficient	0000 0000	
		b_2 coefficient	0000 0000	
		a_1 coefficient	0000 0000	
		a_2 coefficient	0000 0000	
0x89	8	Bass and Treble Bypass Register, Channels 1		R/W
		Channel bass and treble bypass	0080 0000	
		Channel bass and treble inline	0000 0000	
0x8A	8	Bass and Treble Bypass Register, Channels 2		R/W
		Channel bass and treble bypass	0080 0000	
		Channel bass and treble inline	0000 0000	
0x8B	8	Bass and Treble Bypass Register, Channels 3		R/W
		Channel bass and treble bypass	0080 0000	
		Channel bass and treble inline	0000 0000	
0x8C	8	Bass and Treble Bypass Register, Channels 4		R/W
		Channel bass and treble bypass	0080 0000	
		Channel bass and treble inline	0000 0000	
0x8D	8	Bass and Treble Bypass Register, Channels 5		R/W
		Channel bass and treble bypass	0080 0000	
		Channel bass and treble inline	0000 0000	
0x8E	8	Bass and Treble Bypass Register, Channels 6		R/W
		Channel bass and treble bypass	0080 0000	
		Channel bass and treble inline	0000 0000	
0x8F	8	Bass and Treble Bypass Register, Channels 7		R/W
		Channel bass and treble bypass	0080 0000	
		Channel bass and treble inline	0000 0000	
0x90	8	Bass and Treble Bypass Register, Channels 8		R/W
		Channel bass and treble bypass	0080 0000	
		Channel bass and treble inline	0000 0000	
0x91	4	Loudness Log2 gain (LG)	0FC0 0000	R/W
0x92	4	Loudness Log2 offset (LO)	0000 0000	R/W

0x93	4	Loudness gain (G)	0000 0000	R/W
0x94	4	Loudness offset lower 32 bits (O)	0000 0000	R/W
0x95	20	Loudness Biquad coefficient b_0 Loudness Biquad coefficient b_1 Loudness Biquad coefficient b_2 Loudness Biquad coefficient a_0 Loudness Biquad coefficient a_2	00FE 5045 0F81 AA27 0000 D513 0000 0000 0FFF 2AED	R/W
0x96	4	DRC1 Control Register Ch1-7	0000 0000	R/W
0x97	4	DRC2 Control Register Ch8	0000 0000	R/W
0x98	8	DRC1 energy Ch 1,2,3,4,5,6,7 DRC1 (1-energy) Ch 1,2,3,4,5,6,7	0000 883F 007F 77C0	R/W
0x99	8	DRC1 threshold T1 Ch 1,2,3,4,5,6,7 DRC1 threshold T2 Ch 1,2,3,4,5,6,7	0B20 E2B2 06F9 DE58	R/W
0x9A	12	DRC1 slope Ch 1,2,3,4,5,6,7 k0 DRC1 slope Ch 1,2,3,4,5,6,7 k1 DRC1 slope Ch 1,2,3,4,5,6,7 k2	0040 0000 0FC0 0000 0F90 0000	R/W
0x9B	8	DRC1 offset 1 Ch 1,2,3,4,5,6,7 DRC1 offset 2 Ch 1,2,3,4,5,6,7	FF82 3098 0195 B2C0	R/W
0x9C	16	DRC1 attack Ch 1,2,3,4,5,6,7 DRC1 attack (1-attack) Ch 1,2,3,4,5,6,7 DRC1 decay Ch 1,2,3,4,5,6,7 DRC1 decay (1-decay) Ch 1,2,3,4,5,6,7	0000 883F 007F 77C0 0000 0056 003F FFA8	R/W
0x9D	8	DRC2 energy Ch 8 DRC2 (1-energy) Ch8	0000 883F 007F 77C0	R/W
0x9E	8	DRC2 threshold T1 Ch 8 DRC2 threshold T2 Ch 8	0B20 E2B2 06F9 DE58	R/W
0x9F	12	DRC2 slope Ch 8 k0 DRC2 slope Ch 8 k1 DRC2 slope Ch 8 k2	0040 0000 0FC0 0000 0F90 0000	R/W
0xA0	8	DRC2 offset 1 Ch 8 DRC2 offset 2 Ch 8	FF82 3098 0195 B2C0	R/W
0xA1	16	DRC2 attack Ch 8 DRC2 attack (1-attack) Ch 8 DRC2 decay Ch 8 DRC2 decay (1-decay) Ch 8	0000 883F 007F 77C0 0000 0056 003F FFA8	R/W
0xA2	8	DRC bypass 1 DRC Inline 1	0080 0000 0000 0000	R/W
0xA3	8	DRC bypass 2	0080 0000	R/W

		DRC Inline 2	0000 0000	
0xA4	8	DRC bypass 3 DRC Inline 3	0080 0000 0000 0000	R/W
0xA5	8	DRC bypass 4 DRC Inline 4	0080 0000 0000 0000	R/W
0xA6	8	DRC bypass 5 DRC Inline 5	0080 0000 0000 0000	R/W
0xA7	8	DRC bypass 6 DRC Inline 6	0080 0000 0000 0000	R/W
0xA8	8	DRC bypass 7 DRC Inline 7	0080 0000 0000 0000	R/W
0xA9	8	DRC bypass 8 DRC Inline 8	0080 0000 0000 0000	R/W
0xAA	8	sel op1-8 and mix to PWM1	0080 0000 0000 0000	R/W
0xAB	8	sel op1-8 and mix to PWM2	1080 0000 0000 0000	R/W
0xAC	8	sel op1-8 and mix to PWM3	2080 0000 0000 0000	R/W
0xAD	8	sel op1-8 and mix to PWM4	3080 0000 0000 0000	R/W
0xAE	8	sel op1-8 and mix to PWM5	4080 0000 0000 0000	R/W
0xAF	8	sel op1-8 and mix to PWM6	5080 0000 0000 0000	R/W
0xB0	12	sel op1-8 and mix to PWM7	6080 0000 0000 0000 0000 0000	R/W
0xB1	12	sel op1-8 and mix to PWM8	7080 0000 0000 0000 0000 0000	R/W
0xB2	16	Energy Manager Averaging coefficients (Two 28 bit bit coefficients for satellite and sub-woofer)	0000 0000 0000 0000 0000 0000 0000 0000	R/W
0xB3	4	Energy Manager Weighting co-efficients (28-bit coefficient for channel1)	0000 0000	R/W
0xB4	4	Energy Manager Weighting co-efficients	0000 0000	R/W

		(28-bit coefficient for channel2)		
0xB5	4	Energy Manager Weighting co-efficients (28-bit coefficient for channel3)	0000 0000	R/W
0xB6	4	Energy Manager Weighting co-efficients (28-bit coefficient for channel4)	0000 0000	R/W
0xB7	4	Energy Manager Weighting co-efficients (28-bit coefficient for channel5)	0000 0000	R/W
0xB8	4	Energy Manager Weighting co-efficients (28-bit coefficient for channel6)	0000 0000	R/W
0xB9	4	Energy Manager Weighting co-efficients (28-bit coefficient for channel7)	0000 0000	R/W
0xBA	4	Energy Manager Weighting co-efficients (28-bit coefficient for channel8)	0000 0000	R/W
0xBB	4	Energy Manager high threshold for satellite	0000 0000	R/W
0xBC	4	Energy Manager low threshold for satellite	0000 0000	R/W
0xBD	4	Energy Manager high threshold for sub-woofer	0000 0000	R/W
0xBE	4	Energy Manager low threshold for sub-woofer	0000 0000	R/W
0xBF	4	Reserved	-	N/A
0xC0	4	Reserved	-	N/A
0xC1	4	Reserved	-	N/A
0xC2	4	Reserved	-	N/A
0xC3	4	Reserved	-	N/A
0xC4	4	Reserved	-	N/A
0xC5	4	Reserved	-	N/A
0xC6	4	Reserved	-	N/A
0xC7	4	Reserved	-	N/A
0xC8	4	Reserved	-	N/A
0xC9	4	Reserved	-	N/A
0xCA	4	Reserved	-	N/A
0xCB	4	Reserved	-	N/A
0xCC	4	Reserved	-	N/A
0xCD	4	Reserved	-	N/A
0xCE	4	Reserved	-	N/A
0xCF	20	PSVC Volume Biquad	0080 0000 0000 0000 0000 0000 0000 0000	R/W

			0000 0000	
0xD0	4	Volume, treble, and bass slew rates register	0000 043F	R/W
0xD1	4	Ch1 volume	0000 0048	R/W
0xD2	4	Ch2 volume	0000 0048	R/W
0xD3	4	Ch3 volume	0000 0048	R/W
0xD4	4	Ch4 volume	0000 0048	R/W
0xD5	4	Ch5 volume	0000 0048	R/W
0xD6	4	Ch6 volume	0000 0048	R/W
0xD7	4	Ch7 volume	0000 0048	R/W
0xD8	4	Ch8 volume	0000 0048	R/W
0xD9	4	Master volume	0000 0245	R/W
0xDA	4	Bass filter set register (all channels)	0303 0303	R/W
0xDB	4	Bass filter index register (all channels)	1212 1212	R/W
0xDC	4	Treble filter set register (all channels)	0303 0303	R/W
0xDD	4	Treble filter index register (all channels)	1212 1212	R/W
0xDE	4	AM mode register	0000 0000	R/W
0xDF	4	PSVC range register	0000 0002	R/W
0xE0	4	General control register	0000 0000	R/W
0xE1	4	Reserved	-	N/A
0xE2	4	Reserved	-	N/A
0xE3	4	r_dolby_COEFLR	0029 0333	R/W
0xE4	4	r_dolby_COEFC	001C FEEF	R/W
0xE5	4	r_dolby_COEFLSP	001C FEEF	R/W
0xE6	4	r_dolby_COEFRSP	001C FEEF	R/W
0xE7	4	r_dolby_COEFLSM	0FE3 0111	R/W
0xE8	4	r_dolby_COEFRSM	0FE3 0111	R/W
0xE9	4	Reserved	-	N/A
0xEA	4	Reserved	-	N/A
0xEB	4	Reserved	-	N/A
0xEC	4	Reserved	-	N/A
0xED	4	Reserved	-	N/A
0xEE	4	Reserved	-	N/A
0xEF	4	Reserved	-	N/A
0xF0	4	Reserved	-	N/A
0xF1	4	Reserved	-	N/A
0xF2	4	Reserved	-	N/A
0xF3	4	Reserved	-	N/A

0xF4	4	Reserved	-	N/A
0xF5	4	Reserved	-	N/A
0xF6	4	Reserved	-	N/A
0xF7	4	Reserved	-	N/A
0xF8	4	Reserved	-	N/A
0xF9	4	Reserved	-	N/A
0xFA	4	Reserved	-	N/A
0xFB	4	Reserved	-	N/A
0xFC	4	Reserved	-	N/A
0xFD	4	Reserved	-	N/A
0xFE	4(min)	Multiple_byte write-append register	-	
0xFF	4	Reserved	-	N/A