DRR Configuration for C6657

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The ROM code creates a table of DDR configuration parameters in the local L2 at a fixed address and initializes it to zero. While the ROM boot loader is active, the contents of the table are checked after every boot table section is complete. If the boot ROM finds that the enable bitmap is non-zero the DDR is configured. This allows a single boot table record to configure the DDR table, which can be followed by boot sections that reside in DDR.

|  |  |  |
| --- | --- | --- |
| DDR Configuration | | |
| Byte offset | Name | Description |
| 0 | Enable bitmap MSW | Bits 31:0 of the PLL/EMIF enable bitmap. Bit 0 corresponds to the PLL config, Bit 1 to the SDRAM config register. There are 24 valid bits in this field (with the MSB corresponding to Rw/exc thresh) |
| 4 | Enable bitmap SLSW | Bits 31:0 of the chip level register enable bit map. Bit 0 corresponds to chip level config register 0 |
| 8 | Enbale bitmap LSW | Bits 60:32 of the chip level register enable bit map. Bit 0 corresponds to chip level config register 32 |
| 12 | PLL config | See PLL configuratiopn table below |
| 16 | Config | SDRAM Config Register |
| 20 | config 2 | SDRAM Config 2 Register |
| 24 | Refresh ctl | SDRAM Refresh Control Register |
| 28 | Timing 1 | SDRAM Timing 1 Register |
| 32 | Timing 2 | SDRAM Timing 2 Register |
| 36 | Timing 3 | SDRAM Timing 3 Register |
| 40 | Nvm timing | LPDDR2-NVM Timing Register |
| 44 | Pwr management | Power Management Control Register |
| 48 | IODFT\_TLGC | IODFT Test Logic Global Control Register |
| 52 | Perf ctl cfg | Performance Counter Config Register |
| 56 | Perf ctl sel | Performance Counter Master Region Select Register |
| 60 | Read idle ctl | Read Idle Control Register |
| 64 | Irq enable | System VBUSM Interrupt Enable Set Register |
| 68 | Zq config | SDRAM Output Impedance Calibration Config Register |
| 72 | Temp alert cfg | Temperature Alert Config Register |
| 76 | Phy ctrl 1 | DDR PHY Control 1 Register |
| 80 | Phy ctrl 2 | DDR PHY Control 2 Register |
| 84 | Pri cos map | Priority to Class of Service Mapping Register |
| 88 | Mst id cos map 1 | Master ID to Class of Service 1 Mapping Register |
| 92 | Mst id cos map 2 | Master ID to Class of Service 2 Mapping Register |
| 96 | Ecc ctrl | ECC Control Register |
| 100 | Ecc addr rng 1 | ECC Address Range 1 Register |
| 104 | Ecc addr rng 2 | ECC Address Range 2 Register |
| 108 | Rw/exc thresh | Read Write Execution Threshold Register |
| 112 | DDR 3 Config 0 | Chip level config register 0 |
| 114 | DDR 3 Config 1 | Chip level config register 1 |
| 120 | DDR 3 Config 2 | Chip level config register 2 |
| 124 | DDR 3 Config 3 | Chip level config register 3 |
| 128 | DDR 3 Config 4 | Chip level config register 4 |
| 132 | DDR 3 Config 5 | Chip level config register 5 |
| 136 | DDR 3 Config 6 | Chip level config register 6 |
| 140 | DDR 3 Config 7 | Chip level config register 7 |
| 144 | DDR 3 Config 8 | Chip level config register 8 |
| 148 | DDR 3 Config 9 | Chip level config register 9 |
| 152 | DDR 3 Config 10 | Chip level config register 10 |
| 156 | DDR 3 Config 11 | Chip level config register 11 |
| 160 | DDR 3 Config 12 | Chip level config register 12 |
| 164 | DDR 3 Config 13 | Chip level config register 13 |
| 168 | DDR 3 Config 14 | Chip level config register 14 |
| 172 | DDR 3 Config 15 | Chip level config register 15 |
| 176 | DDR 3 Config 16 | Chip level config register 16 |
| 180 | DDR 3 Config 17 | Chip level config register 17 |
| 184 | DDR 3 Config 18 | Chip level config register 18 |
| 188 | DDR 3 Config 19 | Chip level config register 19 |
| 192 | DDR 3 Config 20 | Chip level config register 20 |
| 196 | DDR 3 Config 21 | Chip level config register 21 |
| 200 | DDR 3 Config 22 | Chip level config register 22 |
| 204 | DDR 3 Config 23 | Chip level config register 23 |
| 208 | DDR 3 Config 24 | Chip level config register 24 |
| 212 | DDR 3 Config 25 | Chip level config register 25 |
| 216 | DDR 3 Config 26 | Chip level config register 26 |
| 220 | DDR 3 Config 27 | Chip level config register 27 |
| 224 | DDR 3 Config 28 | Chip level config register 28 |
| 228 | DDR 3 Config 29 | Chip level config register 29 |
| 232 | DDR 3 Config 30 | Chip level config register 30 |
| 236 | DDR 3 Config 31 | Chip level config register 31 |
| 240 | DDR 3 Config 32 | Chip level config register 32 |
| 244 | DDR 3 Config 33 | Chip level config register 33 |
| 248 | DDR 3 Config 34 | Chip level config register 34 |
| 252 | DDR 3 Config 35 | Chip level config register 35 |
| 256 | DDR 3 Config 36 | Chip level config register 36 |
| 260 | DDR 3 Config 37 | Chip level config register 37 |
| 264 | DDR 3 Config 38 | Chip level config register 38 |
| 268 | DDR 3 Config 39 | Chip level config register 39 |
| 272 | DDR 3 Config 40 | Chip level config register 40 |
| 276 | DDR 3 Config 41 | Chip level config register 41 |
| 280 | DDR 3 Config 42 | Chip level config register 42 |
| 284 | DDR 3 Config 43 | Chip level config register 43 |
| 288 | DDR 3 Config 44 | Chip level config register 44 |
| 292 | DDR 3 Config 45 | Chip level config register 45 |
| 296 | DDR 3 Config 46 | Chip level config register 46 |
| 300 | DDR 3 Config 47 | Chip level config register 47 |
| 304 | DDR 3 Config 48 | Chip level config register 48 |
| 308 | DDR 3 Config 49 | Chip level config register 49 |
| 312 | DDR 3 Config 50 | Chip level config register 50 |
| 316 | DDR 3 Config 51 | Chip level config register 51 |
| 320 | DDR 3 Config 52 | Chip level config register 52 |
| 324 | DDR 3 Config 53 | Chip level config register 53 |
| 328 | DDR 3 Config 54 | Chip level config register 54 |
| 332 | DDR 3 Config 55 | Chip level config register 55 |
| 336 | DDR 3 Config 56 | Chip level config register 56 |
| 338 | DDR 3 Config 57 | Chip level config register 57 |
| 342 | DDR 3 Config 58 | Chip level config register 58 |
| 346 | DDR 3 Config 59 | Chip level config register 59 |
| 350 | DDR 3 Config 60 | Chip level config register 60 |

DDR Configuration

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| DDR PLL Configuration Bit Fields | | | | | | | | | | |
| 31 | 30 | 29 |  | 16 | 15 |  | 8 | 7 |  | 0 |
| PLL Config Ctl | | PLL Multiplier | | | PLL Pre-Divider | | | PLL Post-divider | | |

DDR PLL Configuration Bit Fields

|  |  |  |
| --- | --- | --- |
| DDR PLL Configuration Field Description | | |
| Field | Value | Description |
| Pll Config Ctl | 0b00 | Pll is not configured |
| 0b01 | PLL is configured only if it is currently disabled or in bypass |
| 0b10 | PLL is configured |
| 0b11 | PLL is disabled and put into bypass |
| Pre-divider | 0-255 | Input clock division. The value 0 is treated as pre-divide by 1 |
| Multiplier | 0-16384 | Multiplier. The value is 0 treated as multiply by 1 |
| Post-divider | 0-255 | PLL output division. The value 0 is treated as post divide by 1 |

DDR PLL Configuration Field Descriptions

The DDR config table is in the reserved L2 area. For C6657 it is at 0x008F\_FD20 with size of 0x120.