

TI TMS320C6678 EVM Board Rev. 3A

DSPM-8301E

PCB PN : 19C2830103

PCB Rev. A104-1

Project Code :

PCB Thickness : 62 mils(1.6mm)
12 Layers

TOP	1.0 oz		
L2_GND	1.0 oz	3.6mils	p.p
		4mils	core
L3	0.5 oz	4.8mils	p.p
L4_PWR	1.0 oz	5mils	core
		4.5mils	p.p
L5	0.5 oz	4.5mils	p.p
L6_GND	1.0 oz	4mils	core
		4.5mils	p.p
L7_GND	1.0 oz	4.5mils	p.p
L8	0.5 oz	5mils	core
		4.8mils	p.p
L9_PWR	1.0 oz	4mils	core
L10	0.5 oz	3.6mils	p.p
L11_GND	1.0 oz		
BOT	1.0 oz		

DISCLAIMER: THIS CIRCUIT DESIGN IS PROVIDED AS REFERENCE ONLY, WITHOUT WARRANTY EXPRESSED OR IMPLIED. THE USER IS ENCOURAGED TO PERFORM ALL DUE DILIGENCE WITH RESPECT TO DESIGN AND ANALYSIS.

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TI Information - Selective Disclosure
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USA

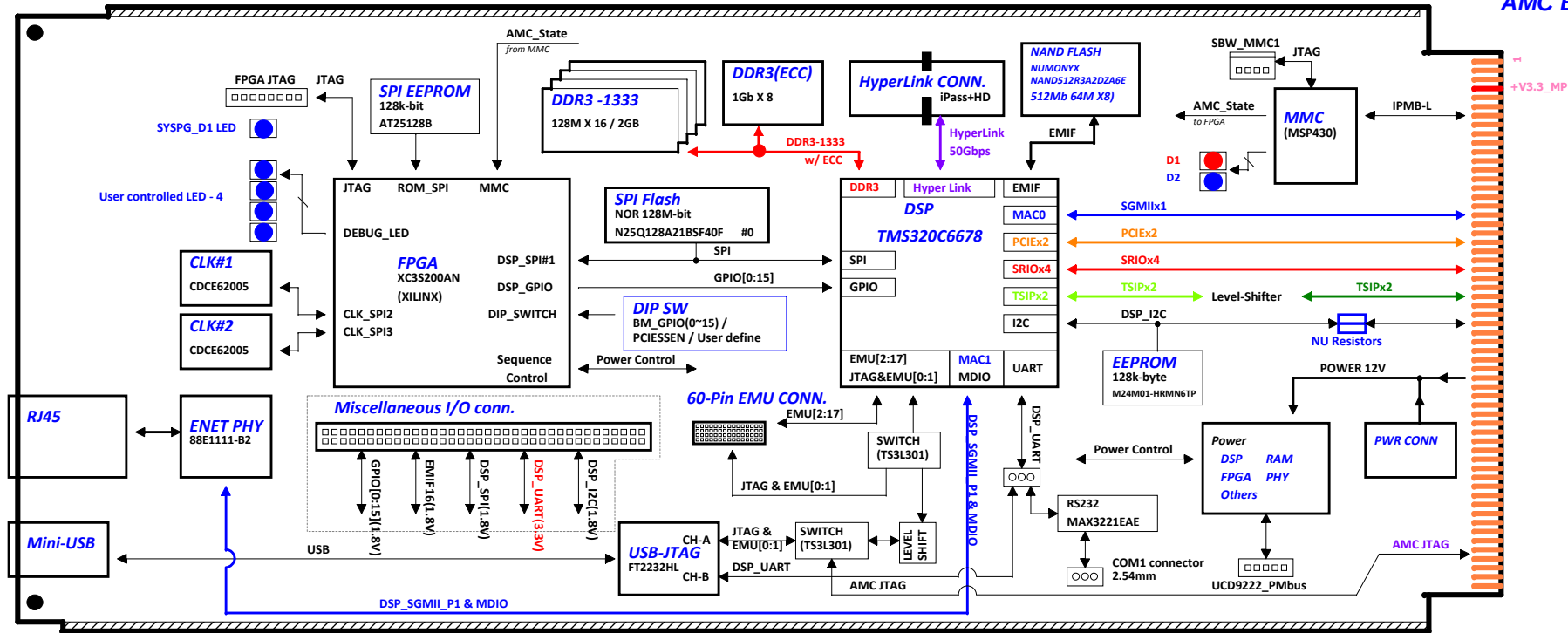
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BLOCK DIAGRAM_AMC

AMC Board

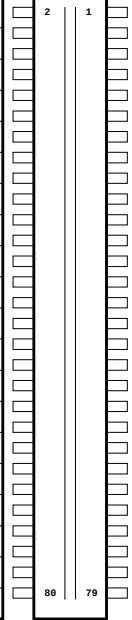


Miscellaneous I/O 80 Pin conn. Signal

AMC Port mapping

PIN	Port mapping
02	EMIFA00
04	EMIFA01
06	EMIFA02
08	EMIFA03
10	EMIFA04
12	EMIFA05
14	EMIFA06
16	EMIFA07
18	EMIFA08
20	EMIFA09
22	EMIFA10
24	EMIFA11
26	EMIFA12
28	EMIFA13
30	EMIFA14
32	EMIFA15
34	EMIFA16
36	EMIFA17
38	EMIFA18
40	EMIFA19

PIN	Port mapping
42	EMIFA20
44	EMIFA21
46	EMIFA22
48	EMIFA23
50	GPIO00
52	GPIO01
54	GPIO02
56	GPIO03
58	GPIO04
60	GPIO05
62	GPIO06
64	GPIO07
66	GPIO08
68	GPIO09
70	GPIO10
72	GPIO11
74	GPIO12
76	GPIO13
78	GPIO14
80	GPIO15



PIN	Port mapping
01	GND
03	SDA
05	SCL
07	EMIFD0
09	EMIFD1
11	EMIFD2
13	EMIFD3
15	EMIFD4
17	EMIFD5
19	EMIFD6
21	EMIFD7
23	EMIFD8
25	EMIFD9
27	EMIFD10
29	EMIFD11
31	EMIFD12
33	EMIFD13
35	EMIFD14
37	EMIFD15
39	EMIFCE1Z

PIN	Port mapping
41	EMIFCE2Z
43	EMIFBE0z
45	EMIFBE1z
47	EMIFOEz
49	EMIFWEz
51	EMIFRnW
53	EMIFWAIT1
55	TIM0
57	TIM00
59	TIM1
61	TIM01
63	SSPMISO
65	SSPMOSI
67	SSPCS1
69	SSPCK
71	UARTTXD
73	UARTRXD
75	UARTRTS
77	UARTCTS
79	GND

PIN	Port mapping
TCLKA	TSIP_CLK0
TCLKB	TSIP_CLK1
FCLKA	100MHz
00	SGMII
01	
02	
03	
04	PCI-E_1
05	PCI-E_2
06	
07	
08	SRIO_1
09	SRIO_2
10	SRIO_3

PIN	Port mapping
11	SRIO_4
12	TSIP0 [0..3]
13	TSIP1 [0..3]
14	
15	Alternate I2C link
16	
TCLKC	TSIP_FS0
TCLKD	TSIP_FS1
17	
18	
19	
20	
	AMC_JTAG

Power Sequence

Label	Time	Description
T0	1ms	S2 plane power stable to S3 enable signal assertion

VCC3V3_MP_AMC			
S0	MMC	VCC3V3_MP	
S1		VCC12	
S2	Other	FT2232H XC3S200AN	VCC3V3_AUX
S3		XC3S200AN	VCC1V8_AUX
S4	88E1111	XC3S200AN	VCC1V2
S5		PMBUS & UCD9222_ENA1	
S6	DSP TMS320C6678	CVDD	
S7		UCD9222_VID2 & UCD9222_ENA2	
S8	DSP TMS320C6678	VCC1V0	
S9		VCC1V8_EN	
S10	DSP TMS320C6678	VCC1V8	
S11		VCC1V5_EN	
S12	DDR3	DSP TMS320C6678	VCC1V5
S13		VCC0V75_EN	
S14	DDR3	DSP TMS320C6678	DDR3 Vref VCC0V75
S15		VCC2V5_EN	
S16	88E1111	VCC2V5	
S17		VCC5_EN	
S18	XDS560V2 Mazzenine Board	VCC5	

RESET# including peripherals.
POR#

RESETFULL#

RESETSTAT#

REFCLKP&N by REFCLK2_PD#
CLOCK2_PLL_LOCK

DORCLKP&N by REFCLK3_PD#
CLOCK3_PLL_LOCK

XILINX_XC3S200AN
1.2V_AUX (VCCINT)
1.8V_AUX (VCC1V8_AUX)
3.3V_AUX (VCC_AUX)

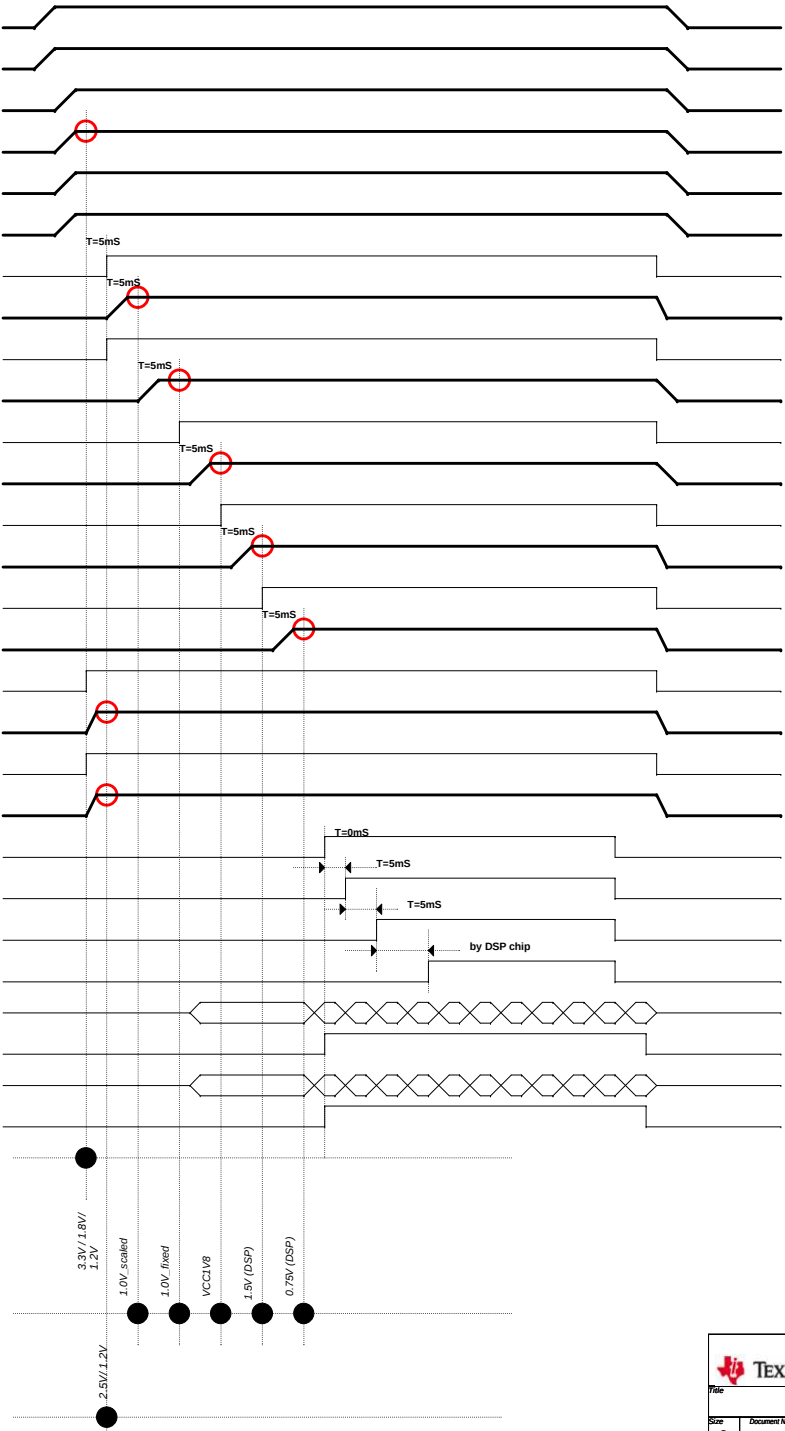
XILINX_XC3S200AN

DSP TMS320C6678
VCC1V0 Scaled/(CVDD)
VCC1V0 Fixed/(CVDD1)
VCC1V8/(DVDD18)
1.5V/(DDR3_IO)
0.75V/(DDR3_Vref)

DSP TMS320C6678

88E1111 (PHY)
2.5V
1.2V

88E1111

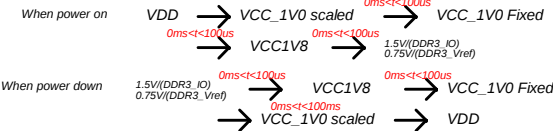


Power Sequence

Reset Sequence

CLK Sequence

There is no specific power-up nor power-down sequence.

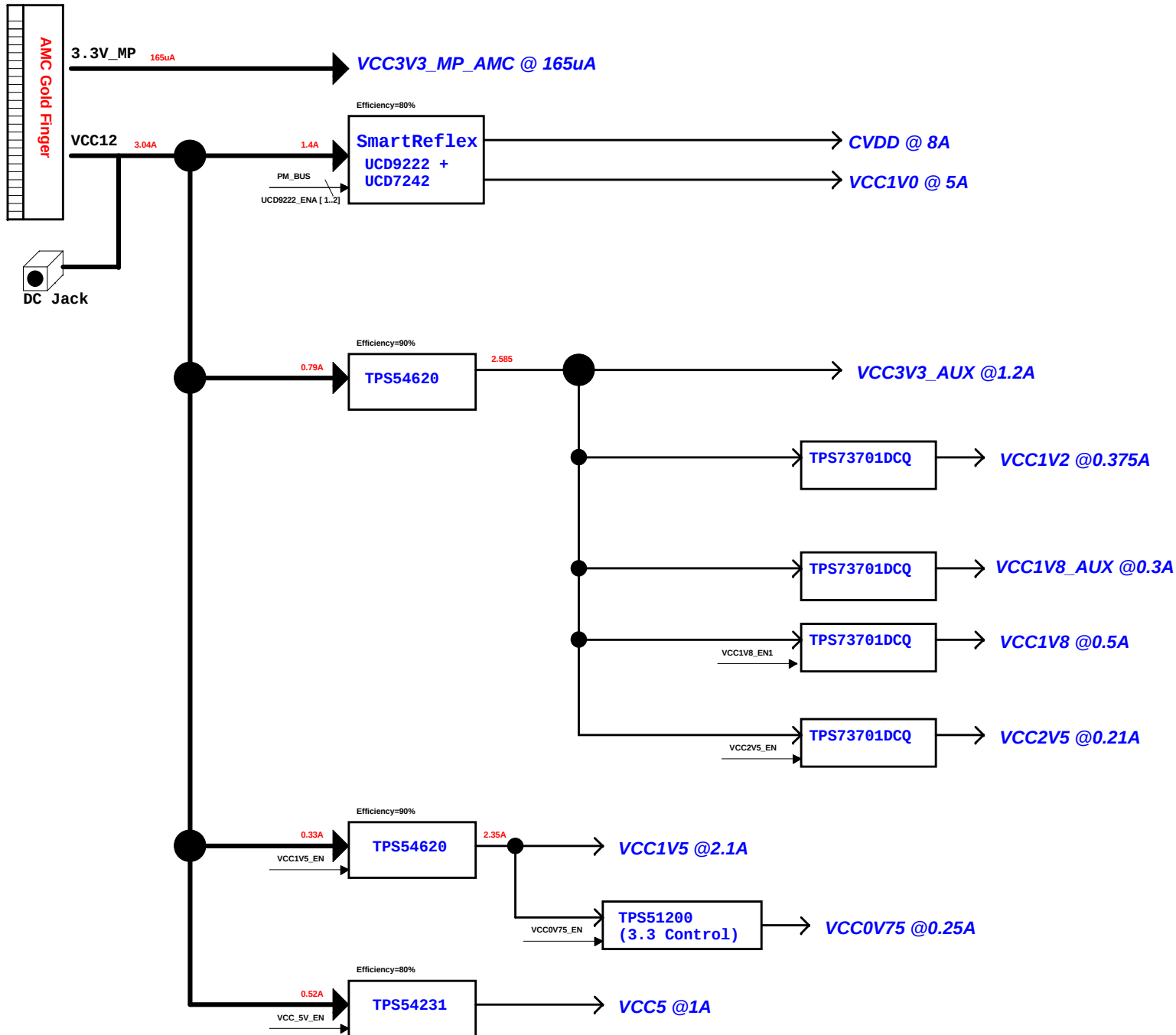


There is no specific power-up nor power-down sequence.

POWER CONSUMPTION

		V	I	Qty	Isub.	Efficiency	Max. Power Design			Operating (for Thermal)		Note
							Pd (W)	I12V	I3vsb	Utilization	Pd (W)	
	CVDD (12V-->1.0V)				8.000			0.741				UCD9222 + UCD7242
	TMS320C6678	1.00	8.000	1	8.000	90%	8.889	0.741	x	70%	6.222	
	VCC1V0 (12V-->1.0V)				5.000			0.463				
	TMS320C6678	1.00	5.000	1	5.000	90%	5.556	0.463	x	70%	3.889	
	VCC1V5 (12V-->1.5V)				2.300			0.319				TPS54620
	TMS320C6678	1.50	0.850	1	0.850	90%	1.417	0.118	x	70%	0.992	
	DDR3	1.50	0.240	5	1.200	90%	2.000	0.167	x	100%	2.000	
	VCC0V75 (VTT for DDR3) 1.5V-->0.75V							x				TPS51200
	DDR3	0.75	0.050	5	0.250	45%	0.417	0.035	x	70%	0.292	
	VCC3V3_AUX (12V-->3.3V_AUX)				2.484			0.748				TPS54620
	FPGA	3.30	0.024	1	0.024	85%	0.093	0.008	x	70%	0.065	
	XD5560V2 Mazzenine Board	3.30	0.300	1	0.300	85%	1.165	0.097	x	70%	0.815	
	FT2232H	3.30	0.210	1	0.210	85%	0.815	0.068	x	70%	0.571	
	Others	3.30	0.660	1	0.660	85%	2.562	0.214	x	70%	1.794	
	VCC1V8_AUX (3.3V_AUX-->1.8V_AUX)							x				TPS73701DCQ
	FPGA	1.80	0.200	1	0.200	46%	0.783	0.065	x	70%	0.548	
	Others	1.80	0.100	1	0.100	46%	0.391	0.033	x	70%	0.274	
	VCC1V8 (3.3V_AUX-->1.8V)							x				TPS73701DCQ
	TMS320C6678	1.80	0.330	1	0.330	46%	1.291	0.108	x	70%	0.904	
	FT2232H	1.80	0.075	1	0.075	46%	0.293	0.024	x	70%	0.205	
	VCC1V2_AUX (3.3V_AUX-->1.2V_AUX)							x				TPS73701DCQ
	FPGA	1.20	0.125	1	0.125	30%	0.500	0.042	x	70%	0.350	
	88E1111	1.00	0.250	1	0.250	90%	0.278	0.023	x	70%	0.194	
	VCC2V5 (3.3V_AUX-->2.5V)							x				TPS73701DCQ
	88E1111	2.50	0.210	1	0.210	65%	0.808	0.067	x	70%	0.565	
	VCC5 (12V-->5V)				1.000			0.490				TPS54231
	XD5560V2 Mazzenine Board	5.00	1.000	1	1.000	85%	5.882	0.490	x	70%	4.118	
	VCC3V3_MP_AMC (150mA)				0.048			x	0.048			
	MMC_MSP430	3.30	0.048	1	0.048	100%	0.158	x	0.048	70%	0.111	
	Total power consumption						Pmax.	I12V	I3VSB		Pop.	
							33.298	2.762	0.096		23.909	

POWER DISTRIBUTION



XILINX_XC3S200AN
1.2V_AUX / 0.125A (VCCINT)
3.3V_AUX / 0.024A (VCCAUX)

DSP TMS320C6678
VCC1V0 / 8A Scaled/(CVDD)
VCC1V0 / 5A Fixed/(CVDD1)
VCC1V8 / 0.33A (DVDD18)
1.5V / 0.85A (DDR3_IO)
0.75V/(DDR3_Vref)

DDR3
1.5V / 1.2A (DDR3_VDD)
0.75V / 0.25A (DDR3_Vref)

88E1111 (PHY)
2.5V / 0.21A
1.2V / 0.25A

FT2232H(USB-JTAG)
3.3V / 0.21A

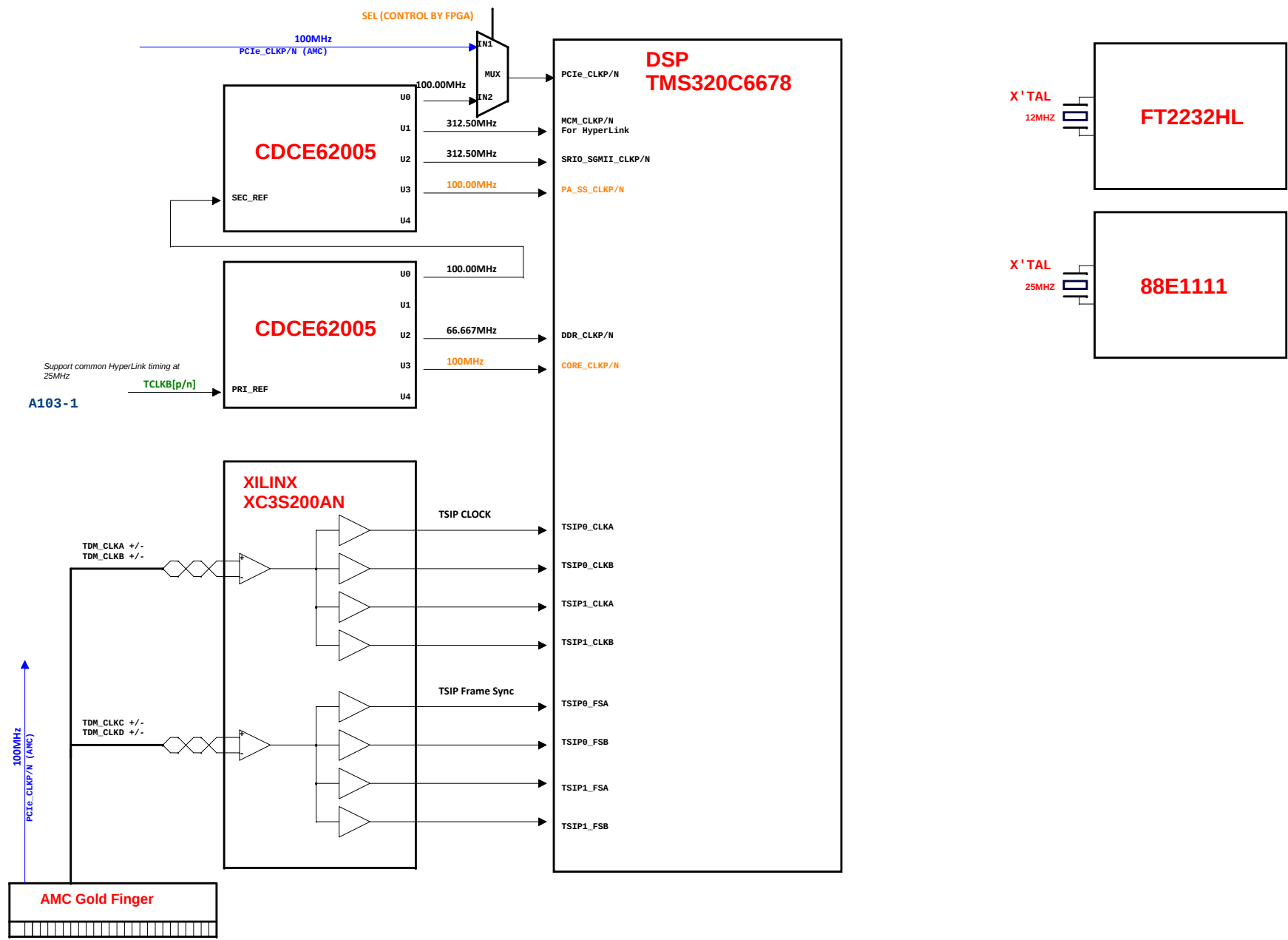
RS232
3.3V

FLASH
1.8V

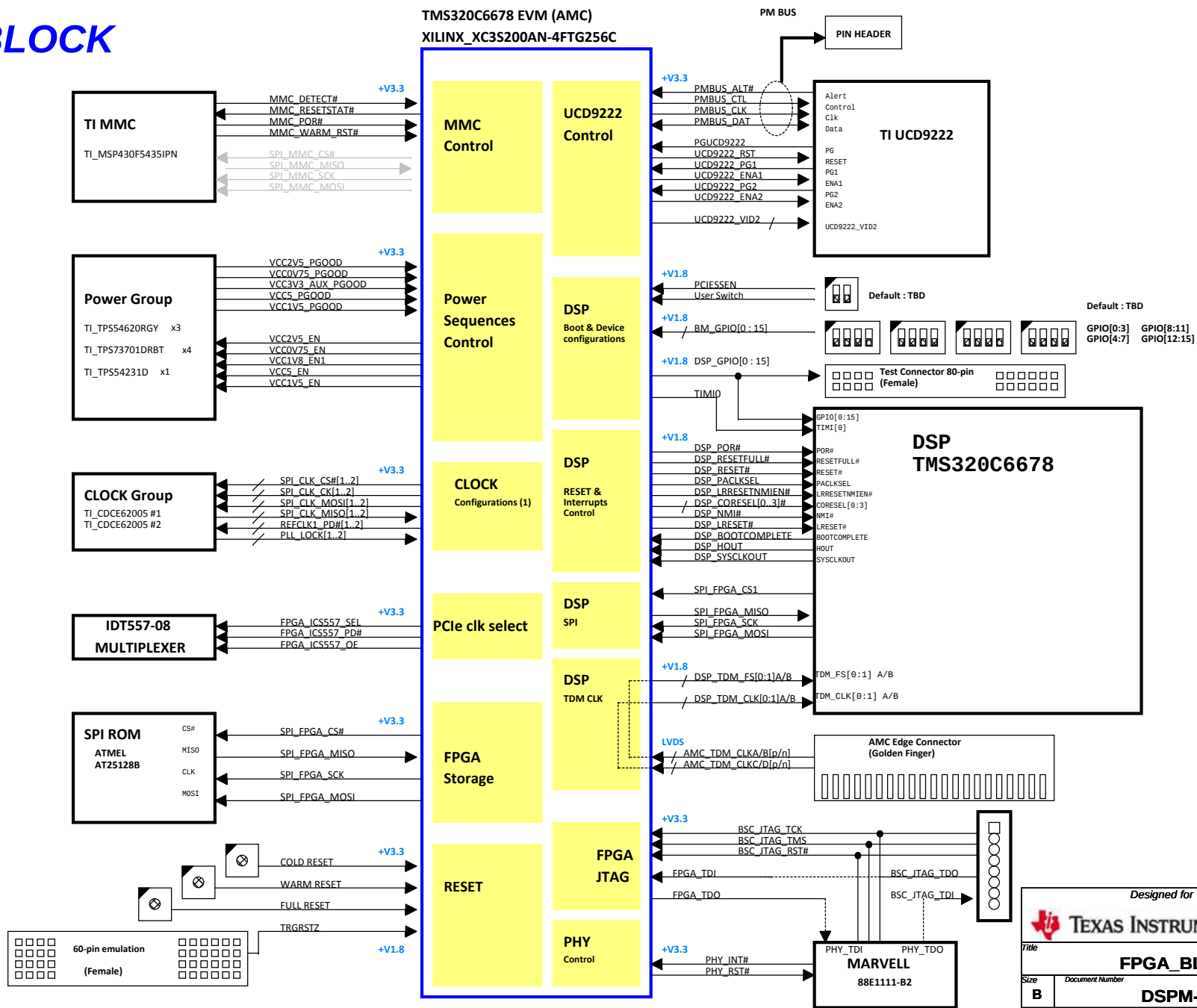
SPI NOR FLASH
1.8V

XDS560V2
Mazzenine Board
5.0V / 1A
3.3V / 0.3A

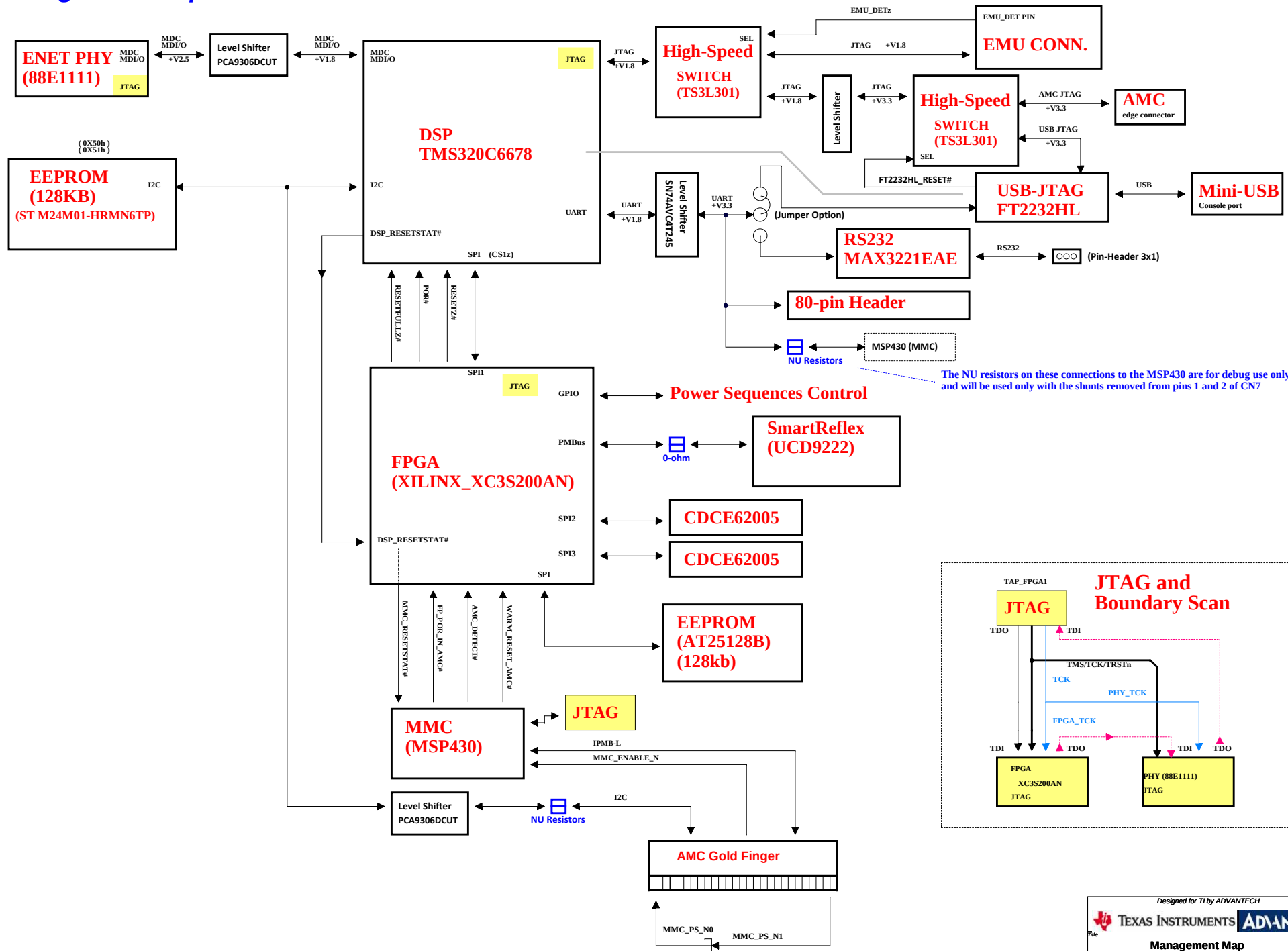
CLOCK DIAGRAM



FPGA_BLOCK

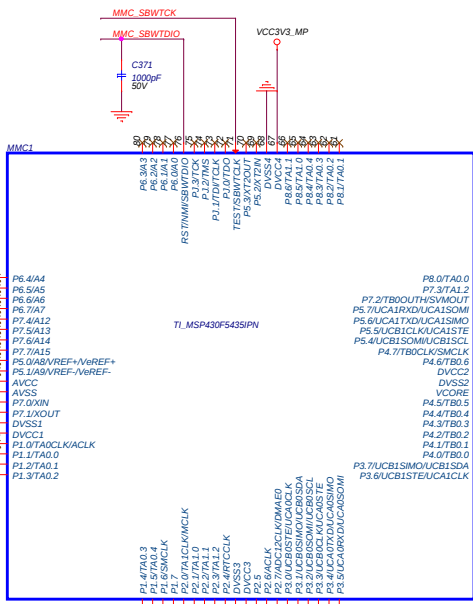
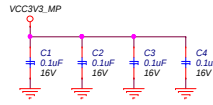
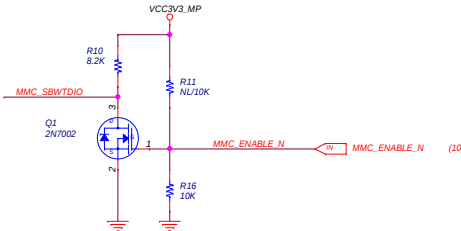
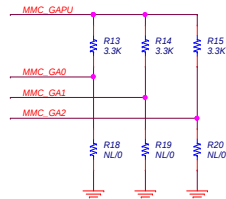
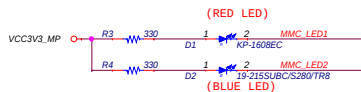
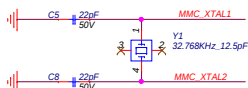
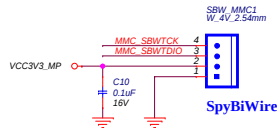
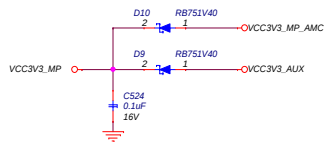


Management Map



The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of CN7

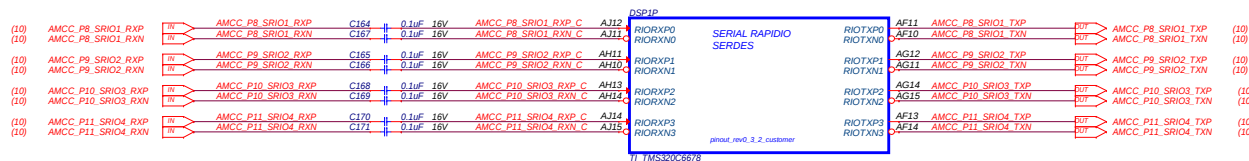
Power for MSP430



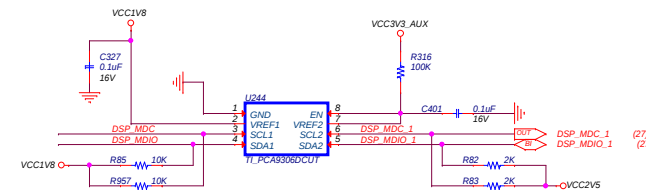
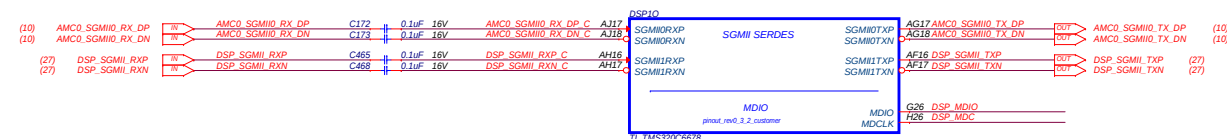
SPI I/F is for Advantech FPGA debugging.

The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of CN7

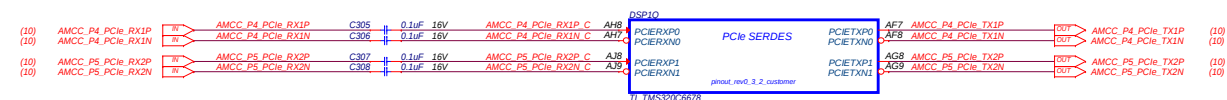
SRIO



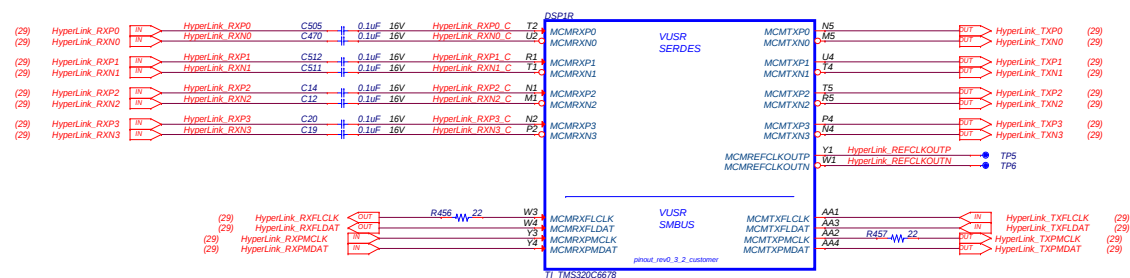
SGMII



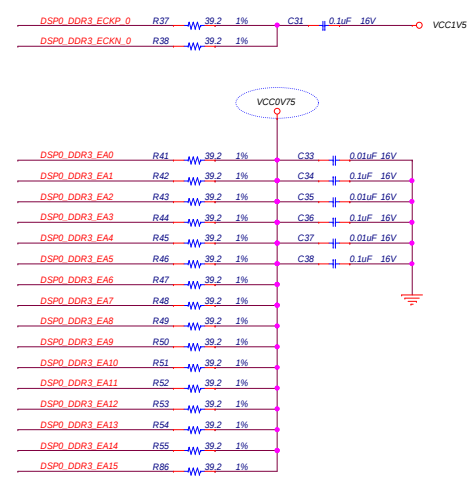
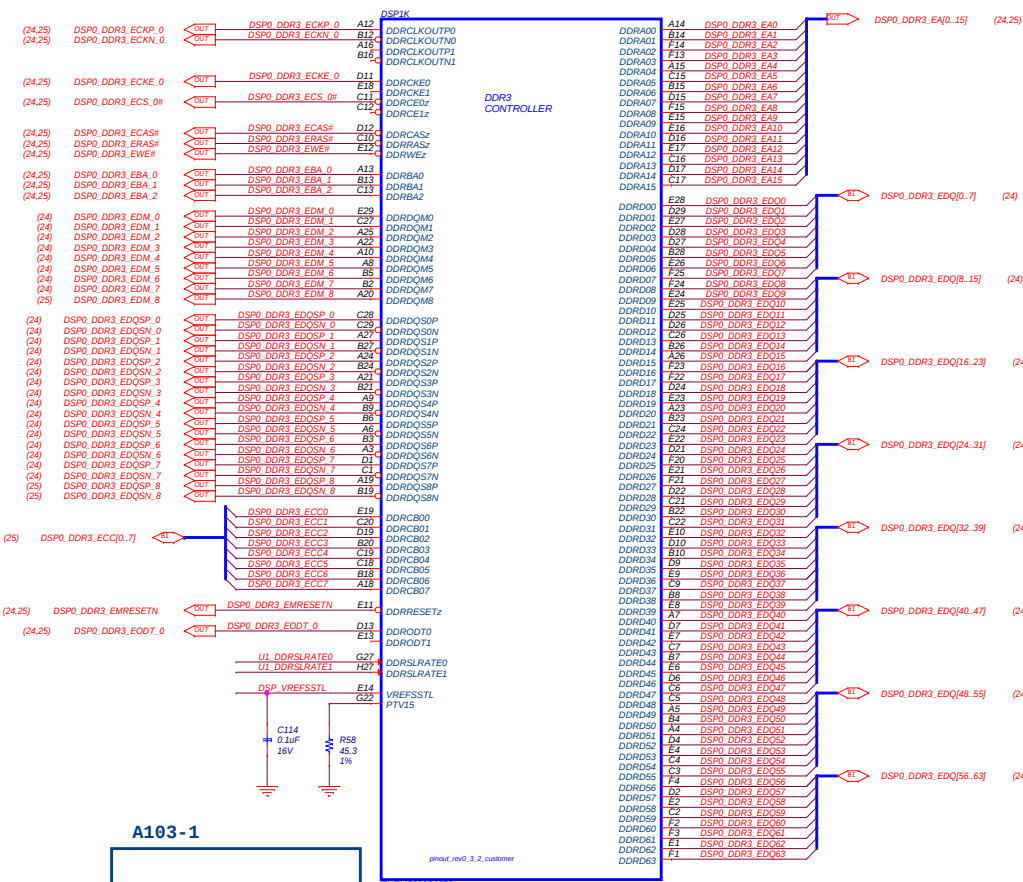
PCIE



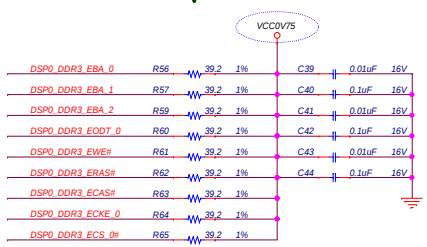
HyperLink



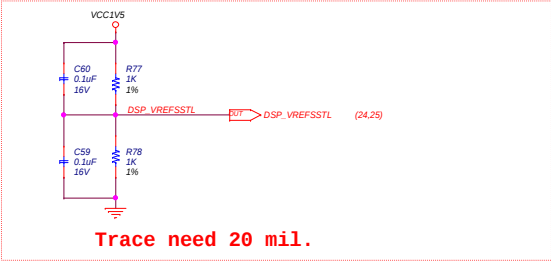
"The HyperLink routes must have a maximum of 2 vias and no via stubs – top layer routing recommended"



Place these resistors at the end of the trace.

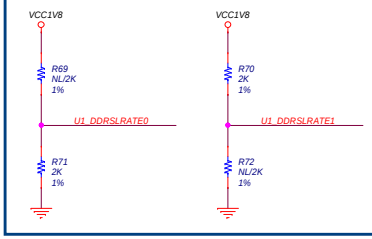


A103-1



Trace need 20 mil.

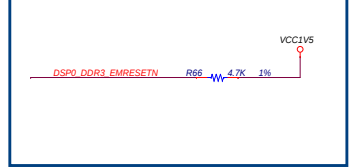
A103-1



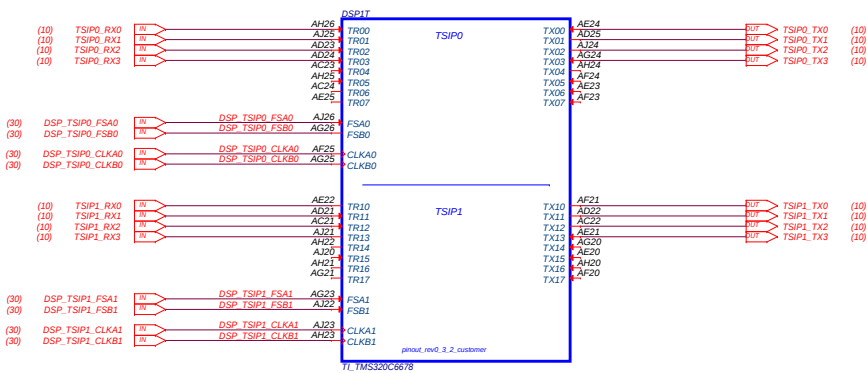
DDR3 Slew-Rate Setting (DDRSRLATE[1:0]):

- 00 Fastest
- 10 Fast
- 01 Slow
- 11 Slowest

A103-1



TSIP0, 1



16M SPI NOR Flash

A103-1

SPI1 change to N25Q128A18SF40F (1410021525)

VCC1V8

C303 0.1uF 16V

VCC1V8 R162 4.7K NOR_HD#

DSP_SS[PC50] R163 4.7K NOR_WP#

DSP_SS[MOSI] R164 4.7K NOR_WP#

DSP_SS[MISO] R165 4.7K NOR_WP#

DSP_SS[MISO] R166 4.7K VCC1V8

(30) NOR_WP# IN

DSP_SS[MISO] R166 4.7K VCC1V8

1M-bit I2C EEPROM

0x50h/0x51h

VCC1V8

R427 NL/0 R428 NL/0 R429 NL/0

R164 NL/0 R165 0 R167 0

C304 0.1uF 16V

VCC1V8

EEPROM1

DJ VCC

E1 E2

E2 E2

VSS SDA

S2 M24M01-1HMN6TP

<Characteristic>

EEPROM_WP R168 4.7K

DSP_SCL R169 4.7K

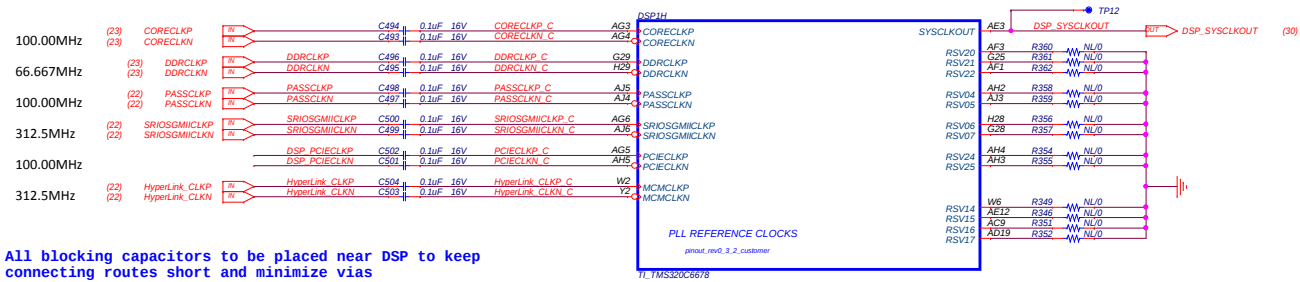
DSP_SDA R169 4.7K

R179 4.7K

EEPROM_WP (30)

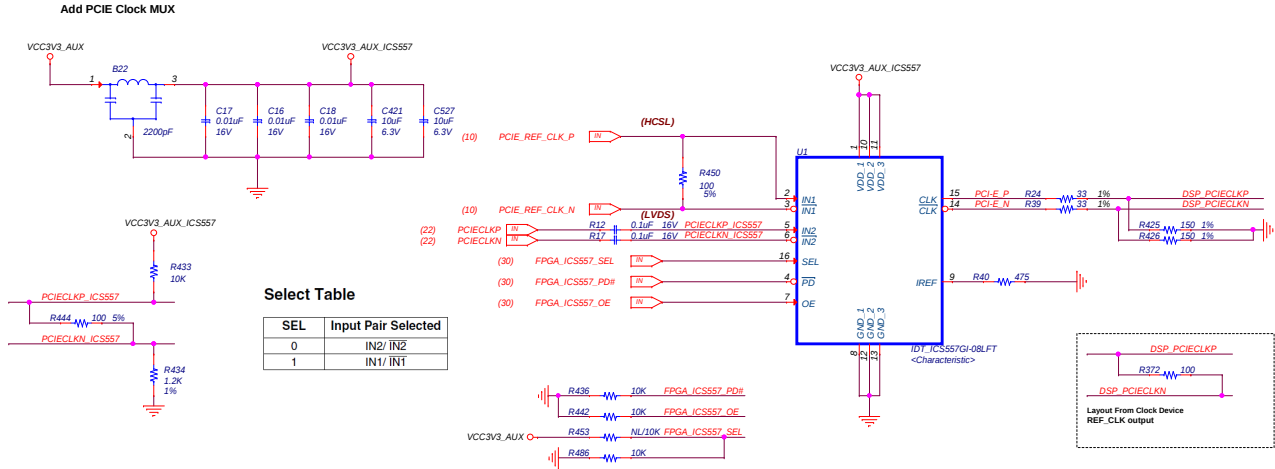
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DSP CLOCK

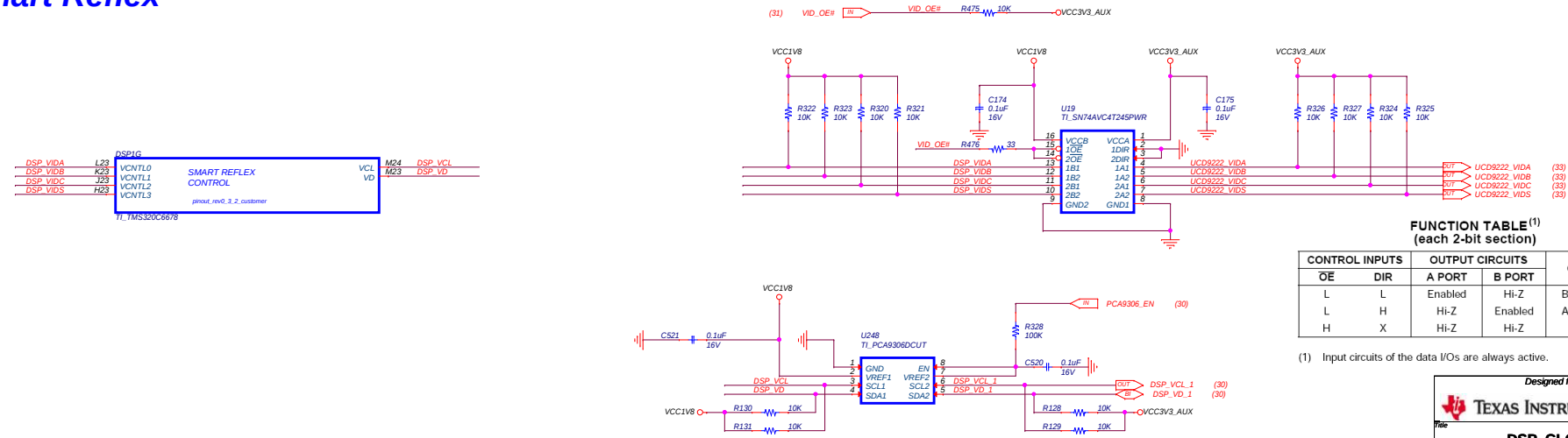


All blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias

All DC-blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias

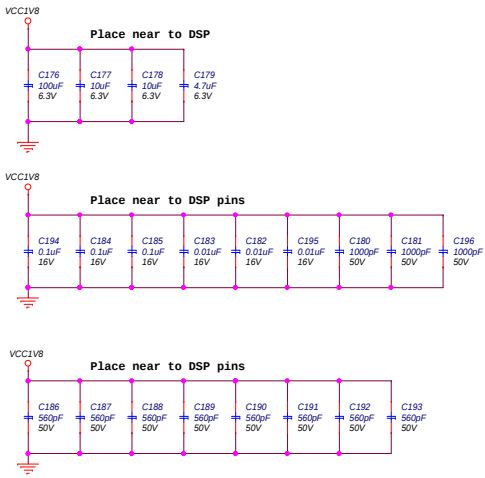
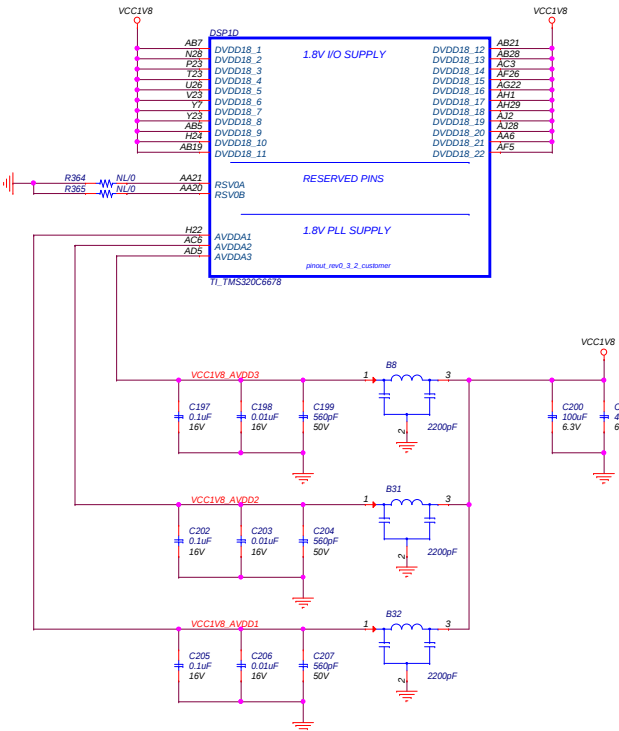


Smart Reflex

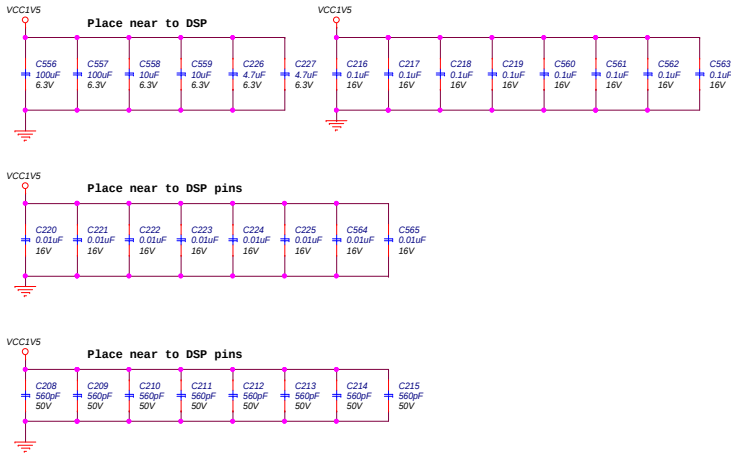
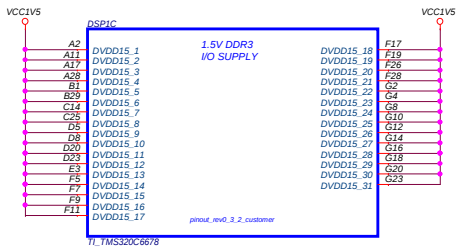


(1) Input circuits of the data I/Os are always active.

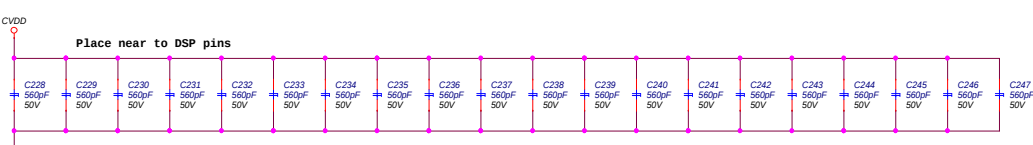
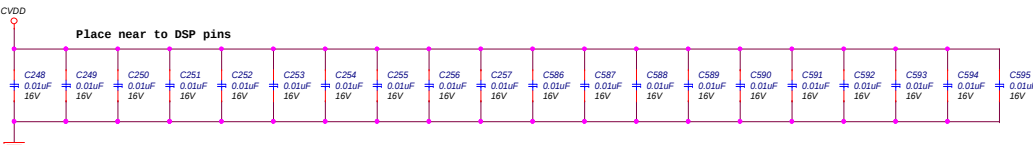
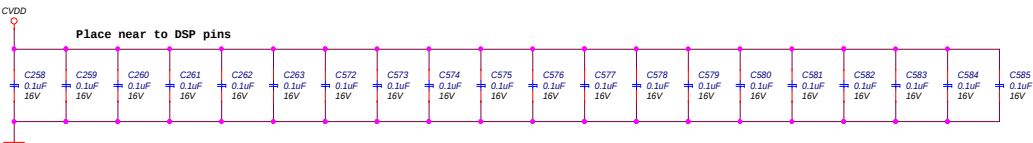
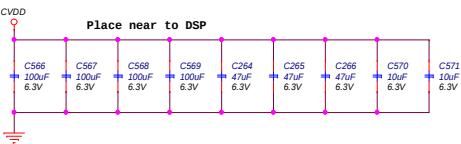
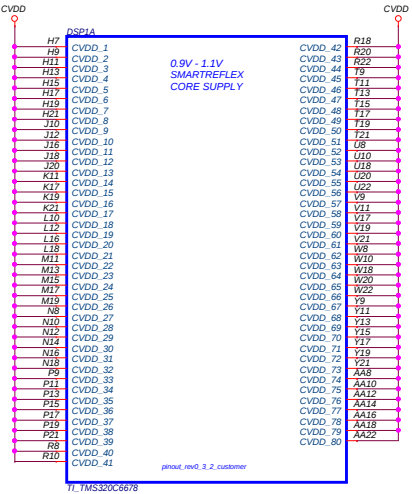
1.8V



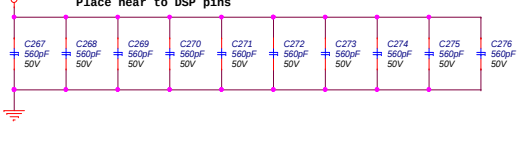
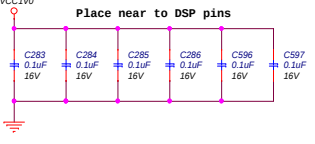
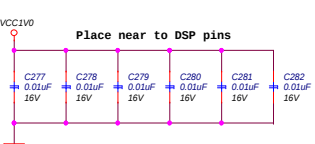
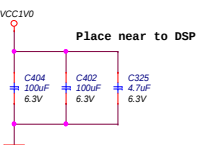
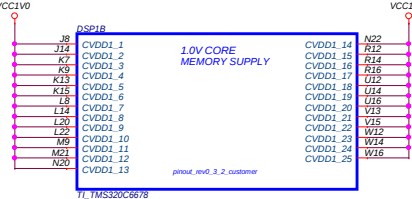
1.5V



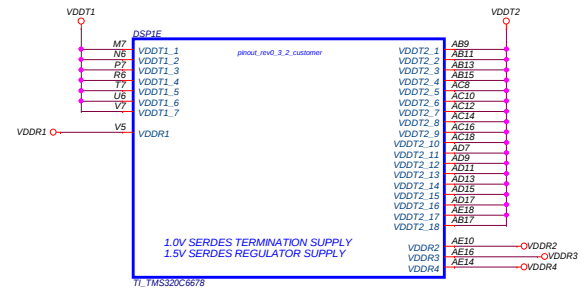
0.9V - 1.1V (Smart Reflex)



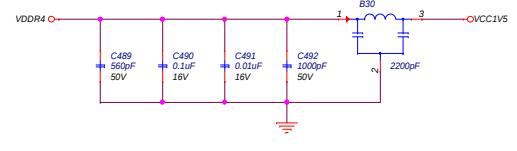
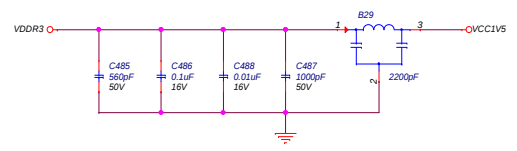
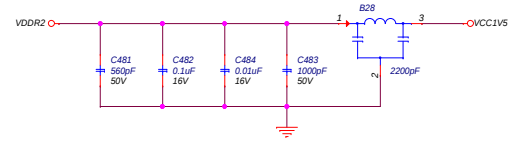
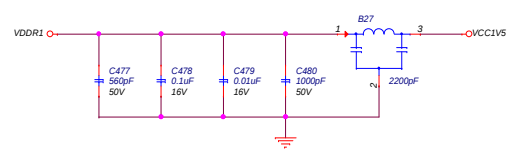
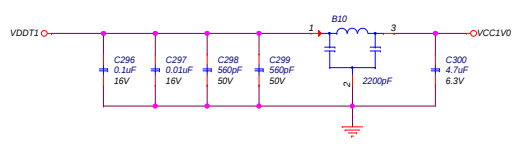
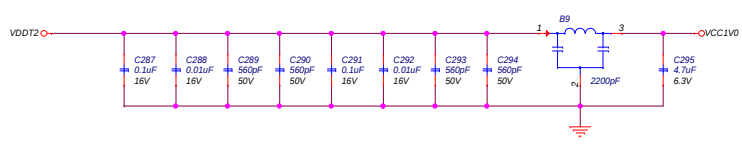
VCC1V0

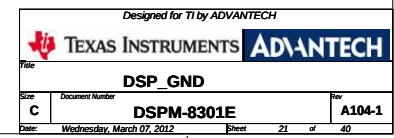


1.0V & 1.5V for Serdes

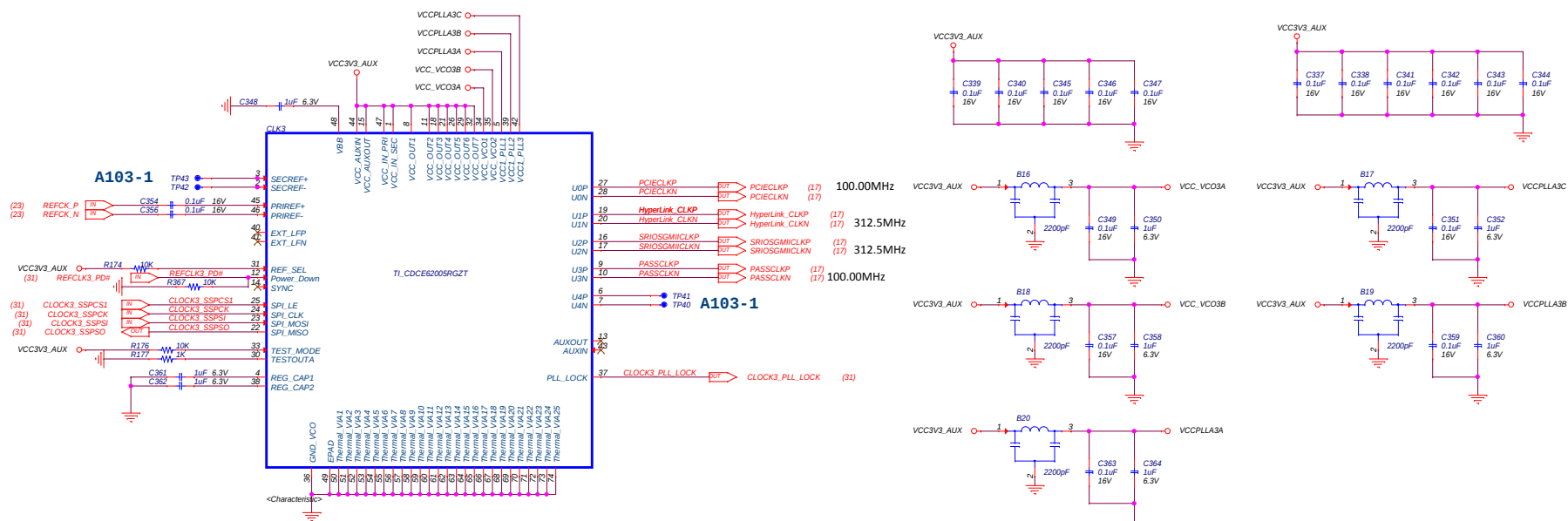


Place near to DSP pins

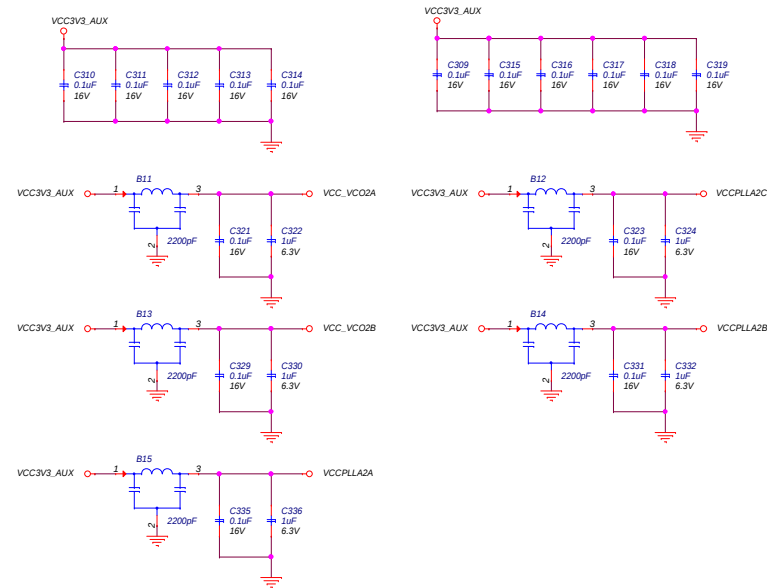


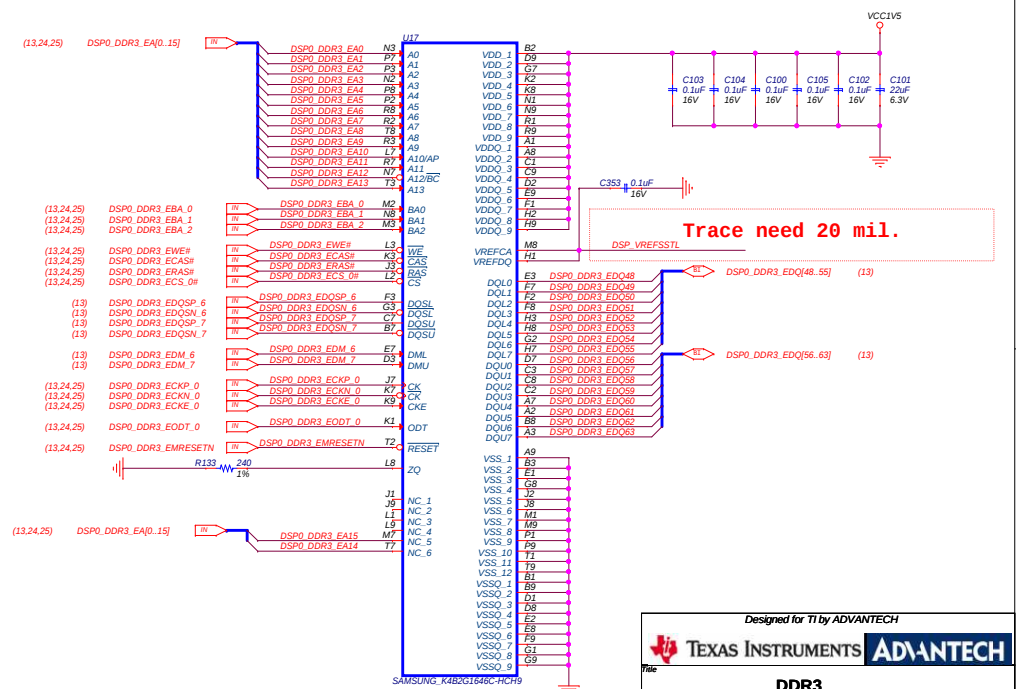
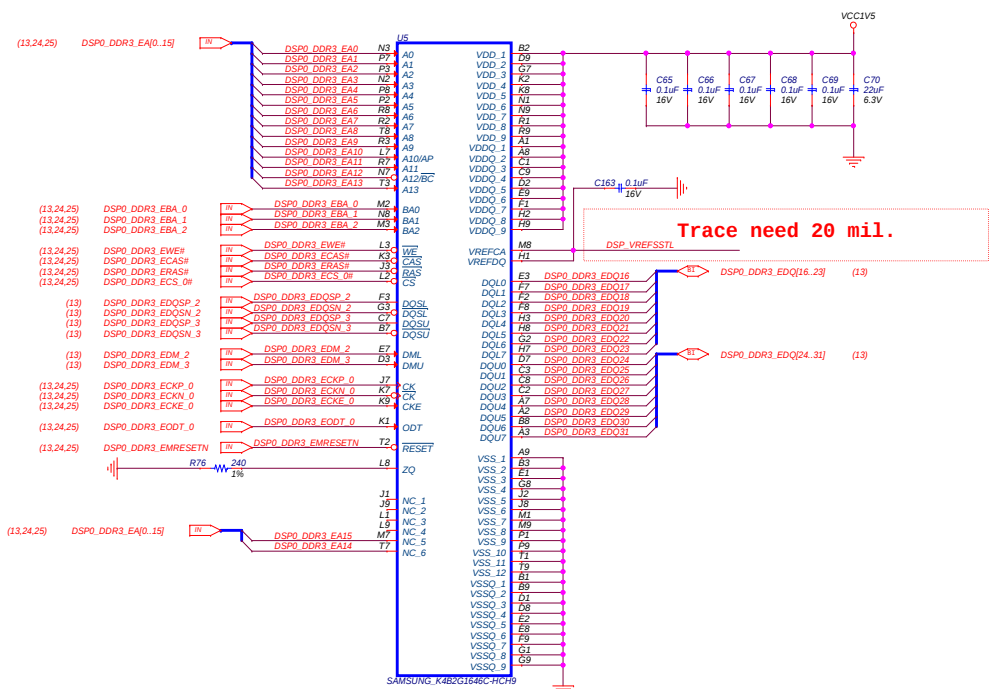
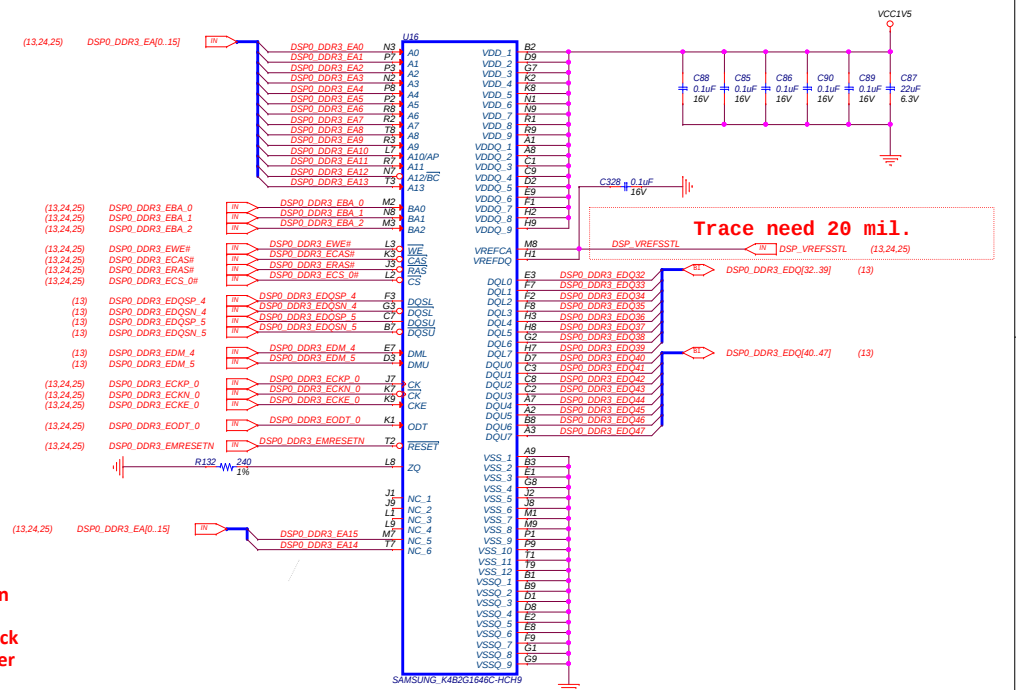
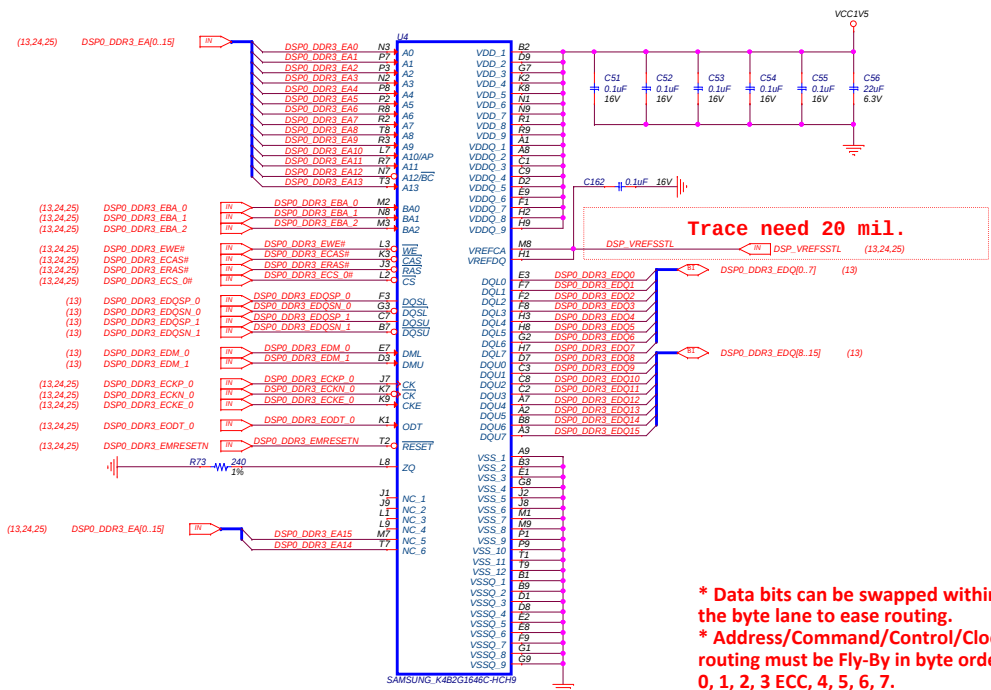


CLOCK GEN3

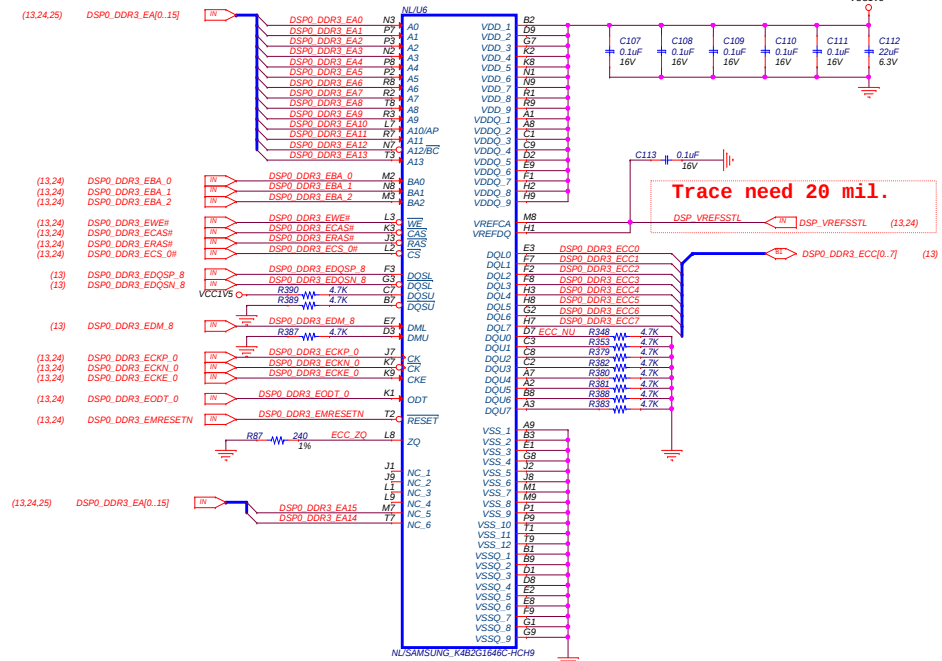


Those caps should be located near the CDCE62005(CLK2)





U4, U5, U16, U17, U8 change SAMSUNG_K4B2G1646C-HCH9



Designed for TI by ADVANTECH			
 TEXAS INSTRUMENTS			
File _____			
DDR3_ECC			
Size	Document Number	New	
C	DSPM-8301E	A104-1	
Date:	Wednesday, March 07, 2012	Sheet	25 of 40



MARVELL_88E1111-B2-BAB1C000



88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

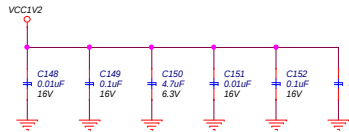
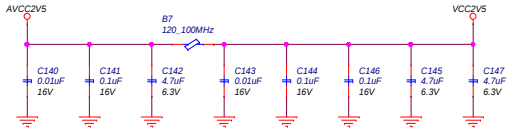
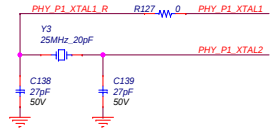
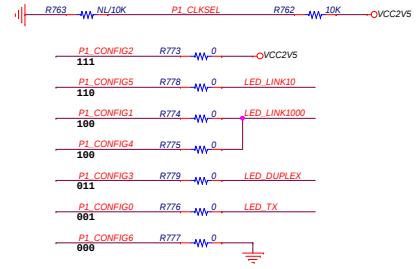
Pin to Constant Mapping

Pin	Bit[2:0]
VDD0	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

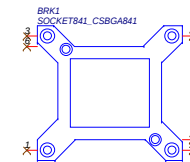
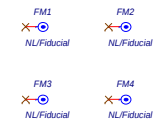
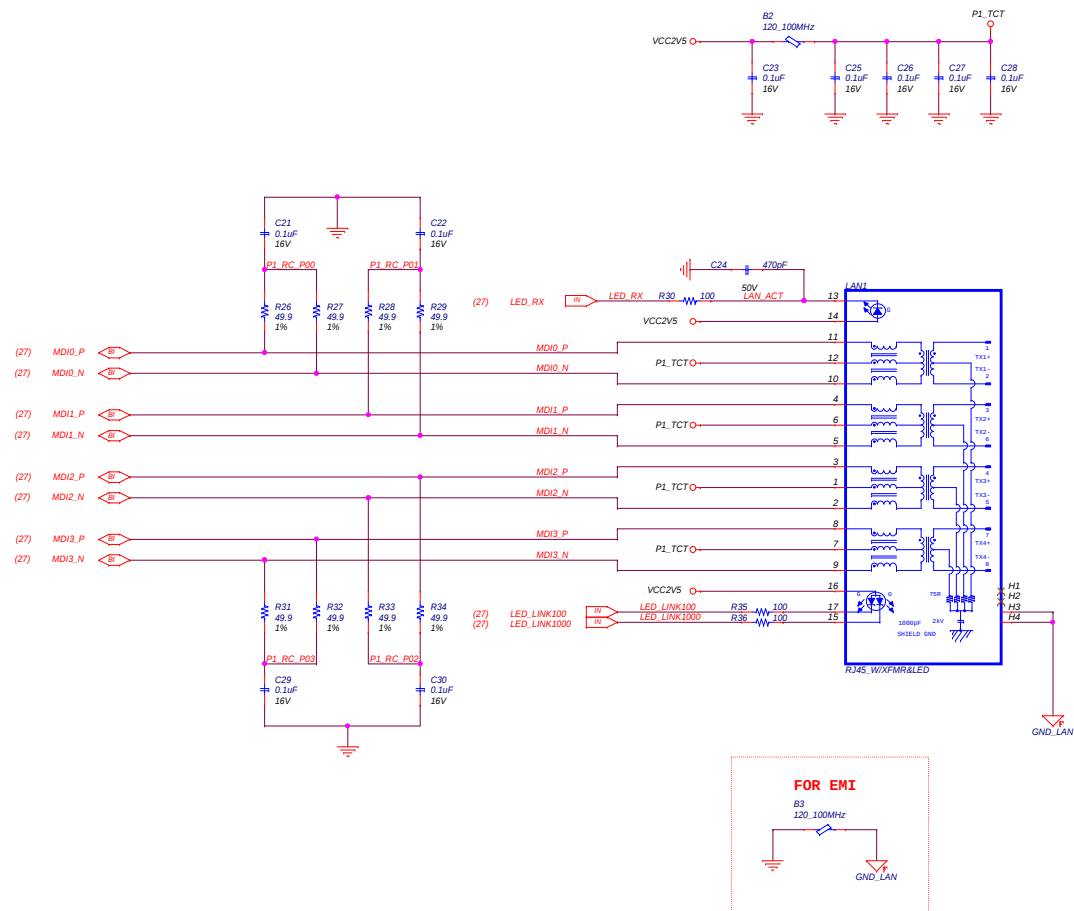
CONFIG Pin Connection

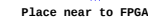
Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDD0	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
CONFIG6	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

PHY Address = 0x01

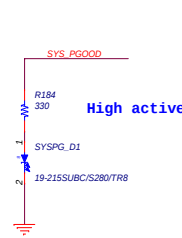
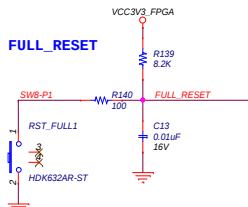
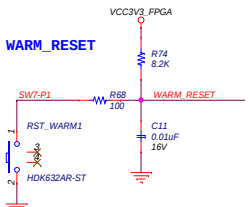
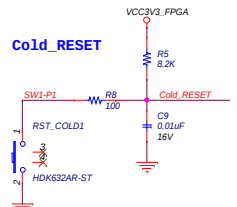
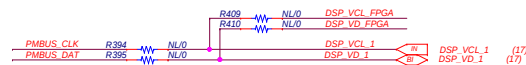
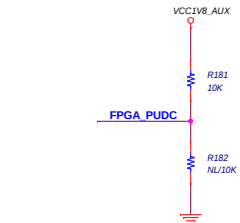


On board





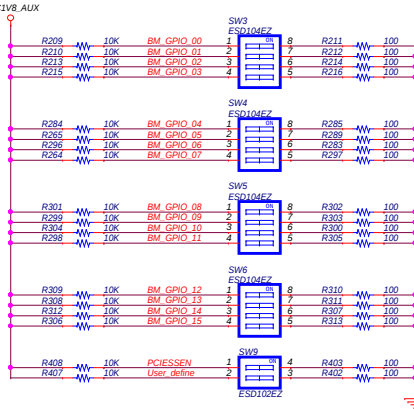
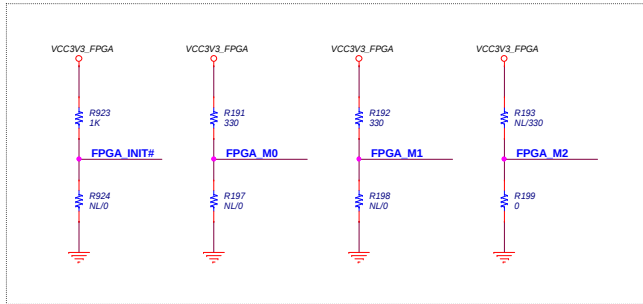
c. FPGA_IC557_SEL, pin.F13



PUDC:
User I/O Pull-Up Control. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank VCC0 input.
0: Pull-ups during configuration
1: No pull-ups

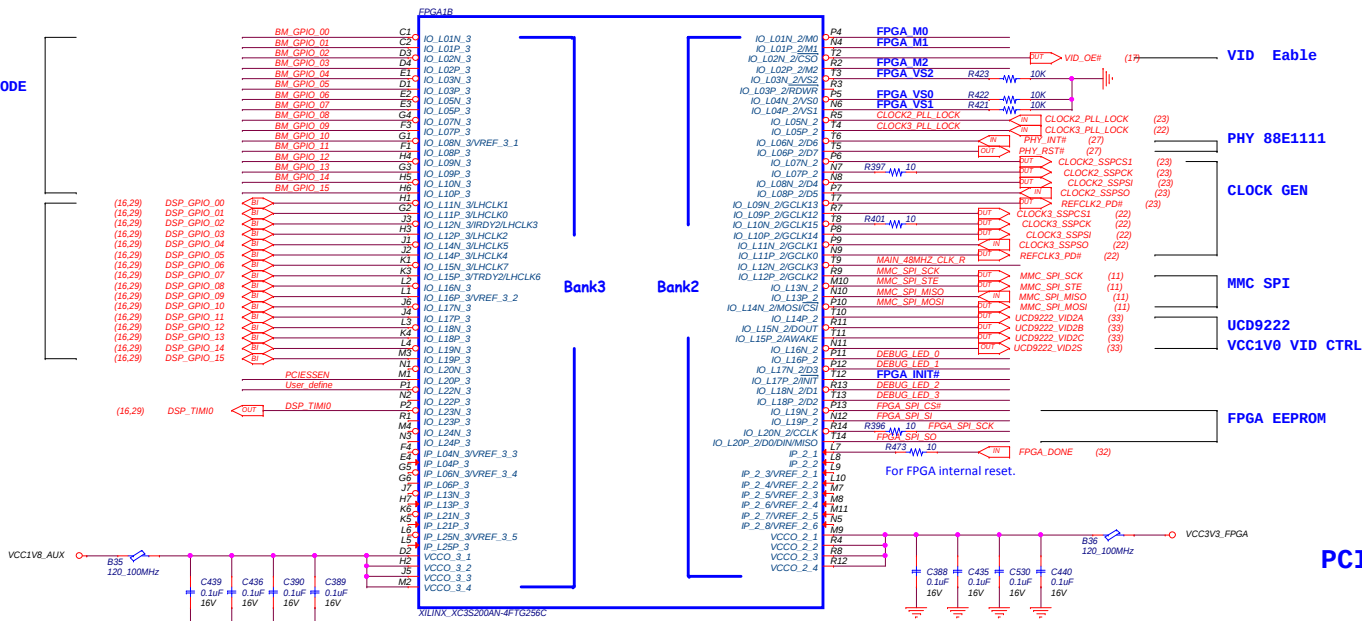
BOOT STRAP CONFIGURATION

default value : TBD

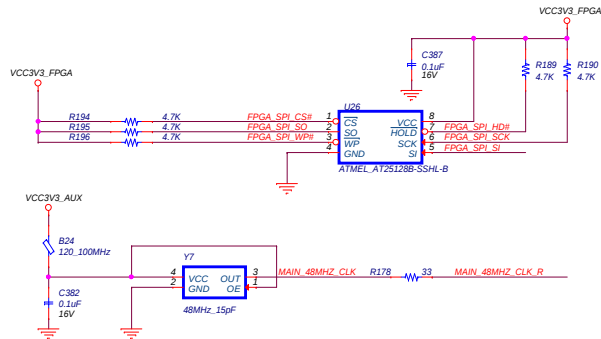
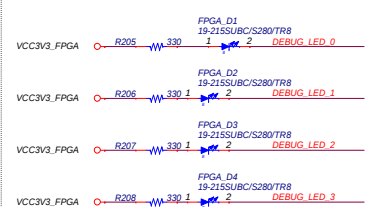


For BOOT MODE SWITCH

DSP GPIO TO FPGA



DEBUG_LED



Boot Configuration

DIP Switch	DSP	Boot Mode	Primary Function	
			Pull Up	Pull Down
BM_GPIO0	GPIO0	LENDIAN	Little Endian	Big Endian
BM_GPIO1	GPIO1	BOOTMODE00	Boot Device	
BM_GPIO2	GPIO2	BOOTMODE01	Boot Device	
BM_GPIO3	GPIO3	BOOTMODE02	Boot Device	
BM_GPIO4	GPIO4	BOOTMODE03	Device Cfg	
BM_GPIO5	GPIO5	BOOTMODE04	Device Cfg	
BM_GPIO6	GPIO6	BOOTMODE05	Device Cfg	
BM_GPIO7	GPIO7	BOOTMODE06	Device Cfg	
BM_GPIO8	GPIO8	BOOTMODE07	Device Cfg	
BM_GPIO9	GPIO9	BOOTMODE08	Device Cfg	
BM_GPIO10	GPIO10	BOOTMODE09	Device Cfg	
BM_GPIO11	GPIO11	BOOTMODE10	PLL Multiplier/I2C	
BM_GPIO12	GPIO12	BOOTMODE11	PLL Multiplier/I2C	
BM_GPIO13	GPIO13	BOOTMODE12	PLL Multiplier/I2C	
BM_GPIO14	GPIO14	PCIESSMODE0	Endpt/RootComplex	
BM_GPIO15	GPIO15	PCIESSMODE1	Endpt/RootComplex	

Boot Device

BM_GPIO	BOOT Device	NOTE
3 2 1	Device	
0 0 0	EMIF16	
0 0 1	sRIO	
0 1 0	SMGII	PA driven from core clk
0 1 1	SGMII	PA driver from PA clk
1 0 0	PCle	
1 0 1	I2C	
1 1 0	SPI	
1 1 1	HyperLink	

Device Configuration

BM_GPIO [10:4]	Device Configuration Field	The device configuration fields GPIO[10:4] are used to configure the boot peripheral and, therefore, the bit definitions depend on the boot mode.
----------------	----------------------------	---

PLL Settings

BM_GPIO	INPUT	CorePac System PLL Configuration
13 12 11	CLK (MHz)	
0 0 0	50.00	
0 0 1	66.67	
0 1 0	80.00	PA driven from core clk
0 1 1	100.00	PA driver from PA clk
1 0 0	156.25	
1 0 1	250.00	
1 1 0	312.50	
1 1 1	122.88	

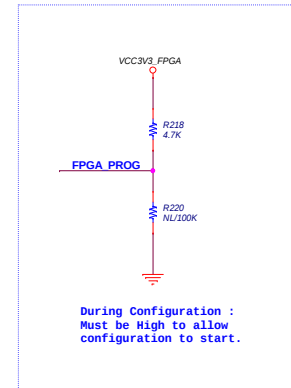
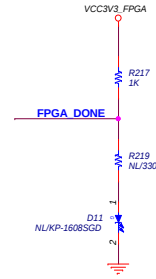
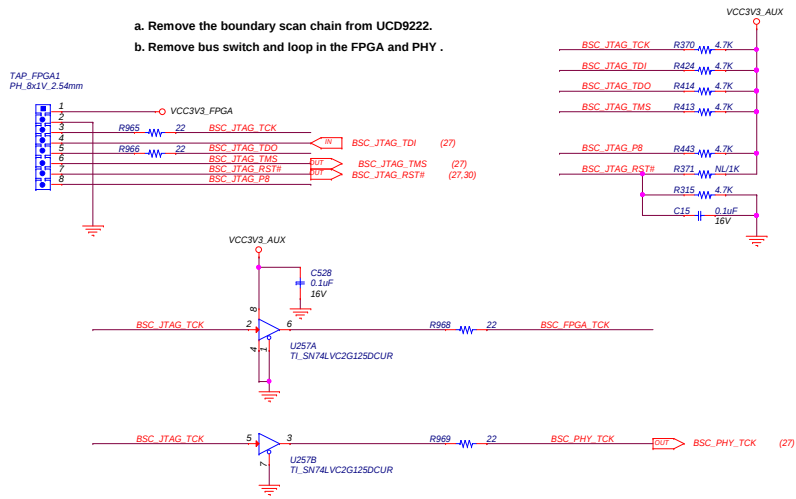
PCIE Mode selection(PCIESSMODE[1:0])

BM_GPIO [15:14]	INPUT	Description
00b		PCle in End-point mode
01b		PCle in Legacy End-point mode(no support for MSI)
10b		PCle in Legacy Root complex mode

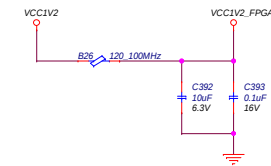
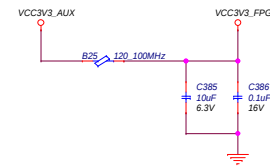
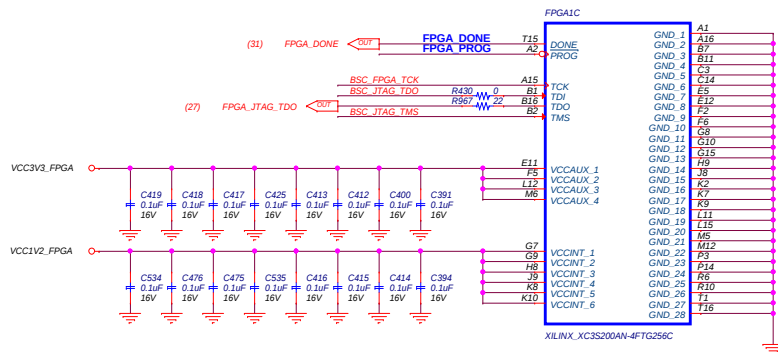
PCIESSSEN

Input	Description
0	Initial state of the power domain and the clock domain for PCIE subsystem is disabled
1	Initial state of the power domain and the clock domain for PCIE subsystem is enabled

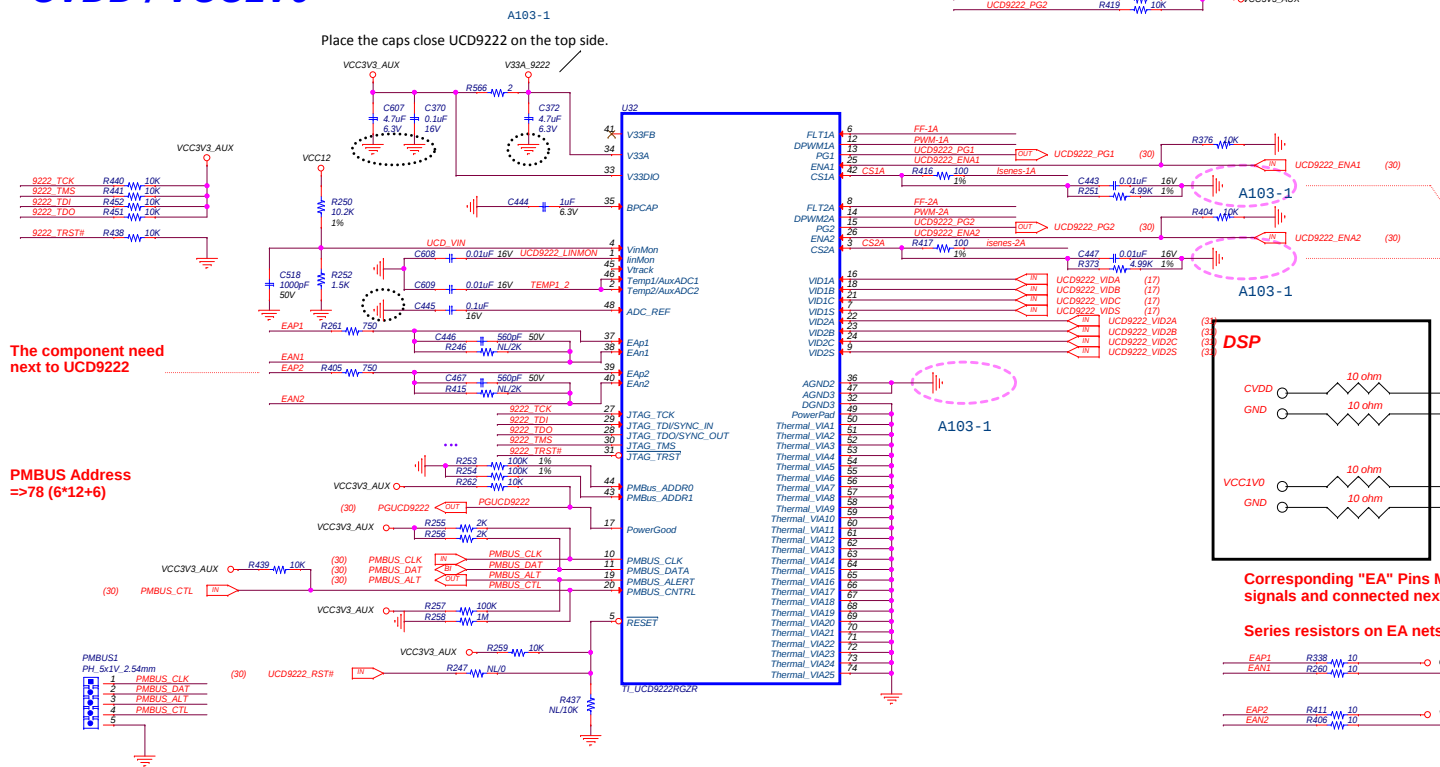
- a. Remove the boundary scan chain from UCD9222.
b. Remove bus switch and loop in the FPGA and PHY .



During Configuration :
Must be High to allow
configuration to start.



CVDD / VCC1V0



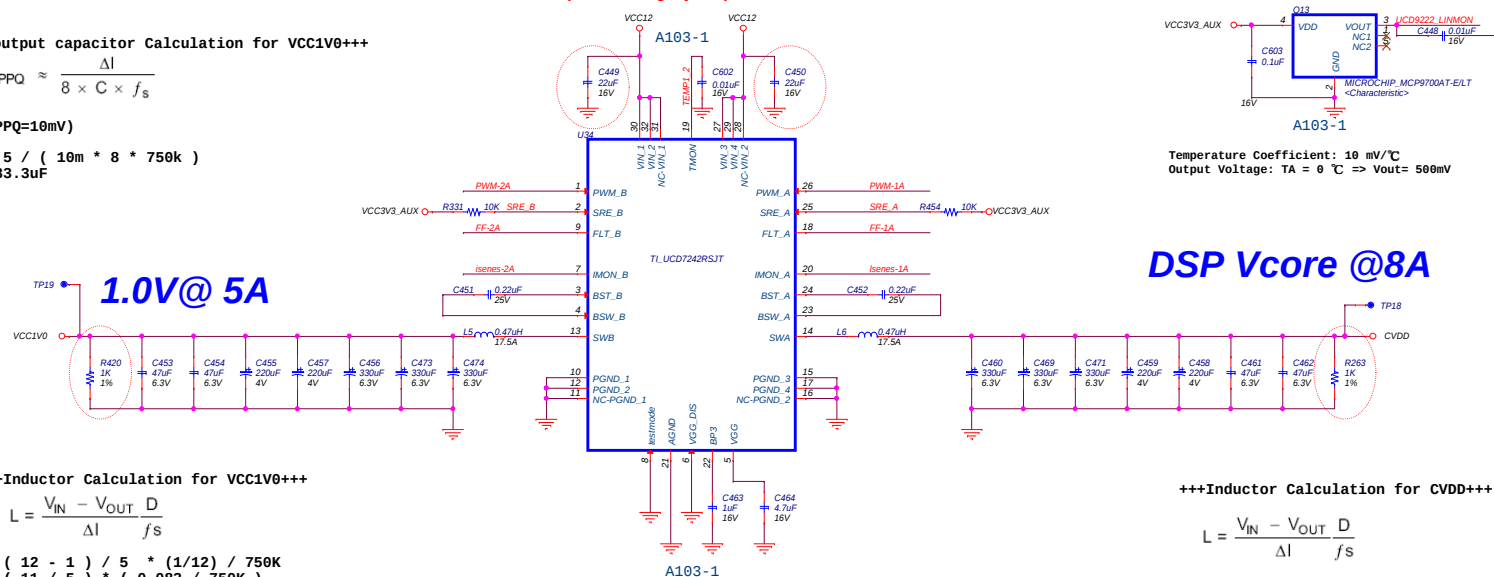
Each 22uF Cin cap needs to tightly coupled to Vin and PGND of the UCD7242.

+++output capacitor Calculation for VCC1V0+++

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

($V_{PPQ}=10\text{mV}$)

$$C = 5 / (10m * 8 * 750k)$$
$$C = 83.3\mu F$$



+++Inductor Calculation for VCC1V0+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{f_s}$$

$$L = (12 - 1) / 5 * (1/12) / 750K$$
$$L = (11 / 5) * (0.083 / 750K)$$
$$L = 0.243 \mu H$$

DSP Vcore @8A

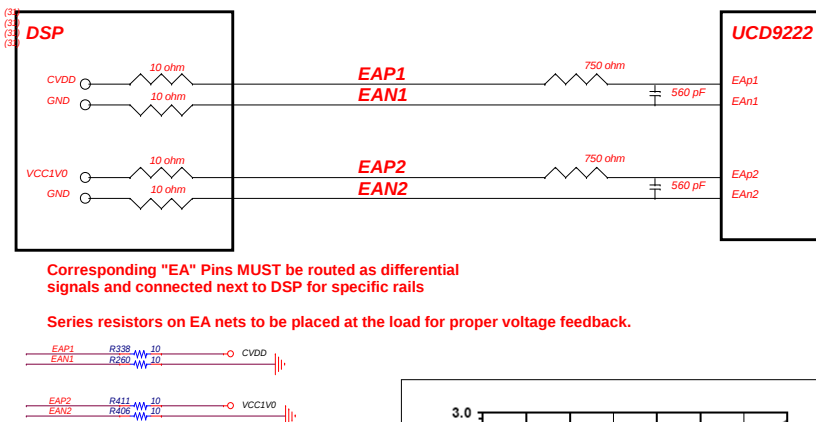
+++Inductor Calculation for CVDD+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{f_s}$$

$$\begin{aligned} L &= (12 - 1) / (8) * (1/12) / 750K \\ L &= (11 / 8) * (0.083 / 750K) \\ L &= 0.152 \mu H \end{aligned}$$

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--



Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

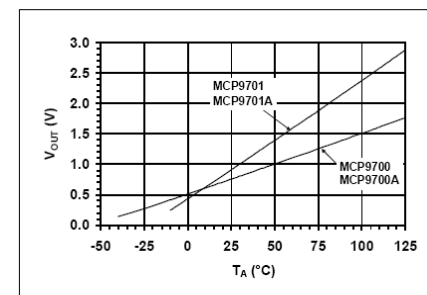


FIGURE 2-16: Output Voltage vs. Ambient Temperature.

+++output capacitor Calculation for VCC1V0+++

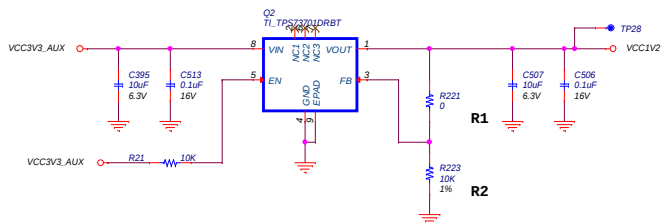
$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

(VPPQ=10mV)

$$C = 8 / (10m * 8 * 750k)$$
$$C = 133.3\mu F$$

VCC1V2

1.2V @0.38A

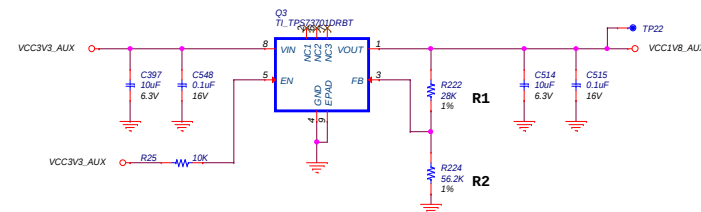


$$V_{out} = (R1 + R2) / R2 * 1.204$$

$$1.204V = (0 + 10K) / 10K * 1.204$$

VCC1V8_AUX

1.8V_AUX @0.3A

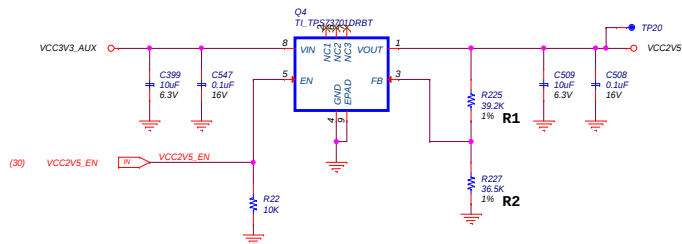


$$V_{out} = (R1 + R2) / R2 * 1.204$$

$$1.805V = (28K + 56.2K) / 56.2K * 1.205$$

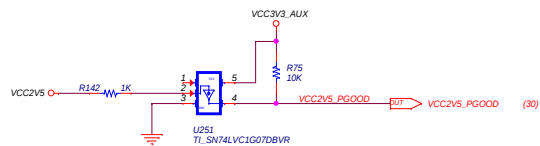
VCC2V5

2.5V @0.21A



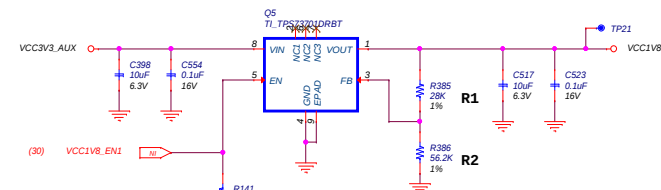
$$V_{out} = (R1 + R2) / R2 * 1.204$$

$$2.50V = (39.2K + 36.5K) / 36.5K * 1.204$$



VCC1V8

1.8V@0.5A

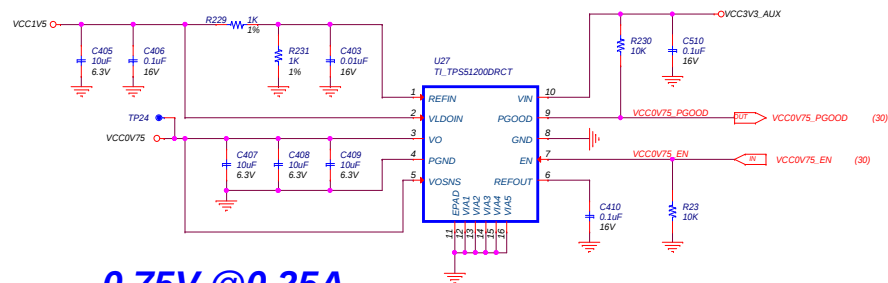


$$V_{out} = (R1 + R2) / R2 * 1.204$$

$$1.805V = (28K + 56.2K) / 56.2K * 1.205$$

VCC0V75

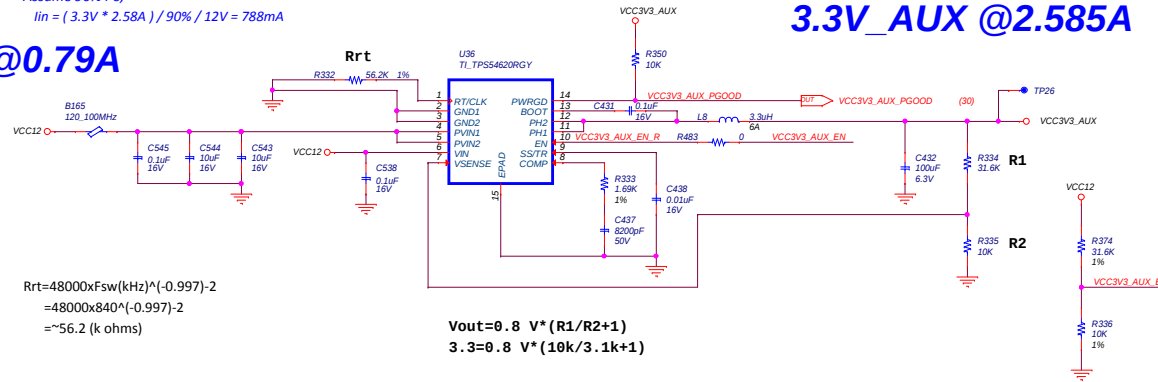
0.75V @0.25A



VCC3V3_AUX

Assume 90% P_e ,
 $I_{in} = (3.3V \times 2.58A) / 90\% / 12V = 788mA$

12V@0.79A



$$R_{rt} = 48000 \times F_{sw}(\text{kHz})^{(-0.997)-2}$$

$$= 48000 \times 840^{(-0.997)-2}$$

$$= \sim 56.2 \text{ (k ohms)}$$

$$V_{out} = 0.8 \text{ V} \times (R1/R2 + 1)$$

$$3.3 = 0.8 \text{ V} \times (10k/3.1k + 1)$$

(Over all tolerance is 5%, DC tolerance is 2.5%)

+++output capacitor Calculation+++

$$C_{out} > (2 \times \Delta I_{out}) / (F_{sw} \times \Delta V_{out})$$

$$C_{out} > (2 \times 3) / (840 \text{ kHz} \times 0.0825)$$

$$C_{out} > \sim 87 \mu\text{F}$$

Reference Capacitor=100uF

(KIND=0.3)

+++Inductor Calculation+++

$$L = (V_{in} - V_{out}) / (I_{out} \times \text{Kind}) \times (V_{out} / (V_{in} \times F_{sw}))$$

$$L = ((12 - 3.3) / (3A \times 0.3)) \times (3.3 / (12 \times 840 \text{ kHz}))$$

$$L = 9.67 \times 0.33 \mu$$

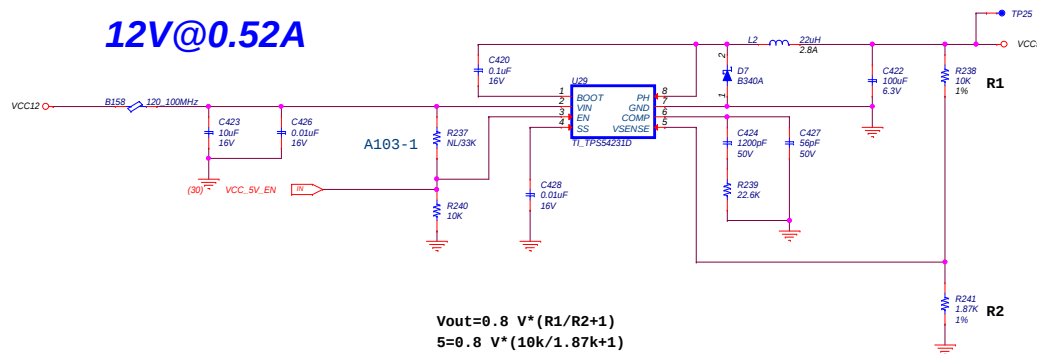
$$L = \sim 3.2 \mu\text{H}$$

Reference Inductor 3.3uH

VCC5

Assume 80% P_e ,
 $I_{in} = (5V \times 1A) / 80\% / 12V = 520mA$

12V@0.52A



$$V_{out} = 0.8 \text{ V} \times (R1/R2 + 1)$$

$$5 = 0.8 \text{ V} \times (10k/1.87k + 1)$$

+++output capacitor Calculation+++

$$C_{O_min} = 1 / (2 \times \pi \times R_O \times F_{CO_max})$$

$$C_{out} = 1 / (2 \times 3.14 \times 5 \times 25K)$$

$$C_{out} = 1.3 \mu\text{F}$$

Reference Capacitor=100uF

5V @1A

+++Inductor Calculation+++ (KIND=0.3)

$$L = ((V_{in(max)} - V_{out}) / I_{out} \times \text{Kind}) \times (V_{out} / (V_{in(max)} \times F_{sw}))$$

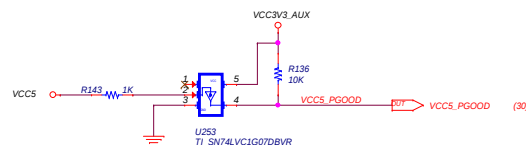
$$L = ((12.6 - 5) / 1 \times \text{Kind}) \times (5 / (12.7 \times 570K))$$

$$L = ((7.6 / 0.3) \times (5 / (7239K)))$$

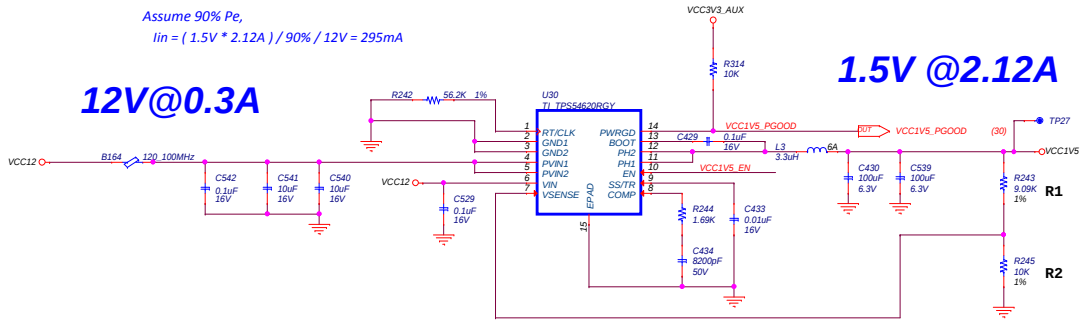
$$L = (25.3) \times (0.69M)$$

$$L = 17.5 \mu\text{H}$$

Reference Inductor 22uH



VCC1V5



$V_{out} = 0.8 \text{ V} * (R1/R2 + 1)$
 $1.52 = 0.8 \text{ V} * (9.09k/10k + 1)$

(Over all tolerance is 5% ,DC tolerance is 2.5%) (KIND=0.3)

+++output capacitor Calculation+++
 $C_{out} = (2 * \Delta I_{out}) / (F_{sw} * \Delta V_{out})$
 $C_{out} = (2 * 2.5A) / (840kHz * 0.0375)$
 $C_{out} \sim 159\mu F$

+++Inductor Calculation+++
 $L = (V_{in} - V_{out}) / (I_{out} * Kind) * V_{out} / (V_{in} * F_{sw})$
 $L = (12 - 1.5) / (2.5A * 0.3) * 1.5 / (12 * 840kHz)$
 $L \sim 2.08\mu H$

Reference Capacitor=200uF Reference Inductor 3.3uH

History

DSPM-8301 A101-1 / 19C2830100

Jan.24.2011:

1. BOM change list: (ECOP-078102)

- a. MMC enable pin: remove R11, populate R16.
- b. DDR3 slew rate setting: remove R72, populate R70.
- c. VCC5_AUX enabled by FPGA: remove R237.
- d. Change I2C serial EEPROM for the 50h & 51h of address.
 - d.1 Change I2C EEPROM to STMicro_M24M01-HRMN6TP.
 - d.2. remove R164.
- e. Change COM1 pin header to the connector with lock.

2. Schematics change list:

- a. Update Block, Sequences, Clock diagrams.
- b. Correct the MCMRX sideband pins to output and the MCMTX sideband pins to input.
- c. Change the note 'NL/' on R235 (RSVD09), populating R234 (RSVD08).

3. FPGA code change list:

- a.1 De-assert PORz first and de-assert RESETFULLz after for DSP reset sequence.
- b. Change DSP clockings: CORECLK = PASSCLK = 100MHz, PCIECLK = 100MHz
- b. Boot mode change to I2C EEPROM and none-boot mode.
- d. All reset behaviours on the board are defined.

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- 1. Add the JTAG connection on AMC edge connector .
- 2. Remove the SW2, R9, C10, R12, R17 for LEDs re-placement.
- 3. Change I2C EEPROM (128kB) to M24M01-HRMN6TP and its footprint.
- 4. Change COM_SEL1 to DIP type and COM1 with lock.
- 5. Add a clock MUX to select the DSP PCIECLK source from the AMC FCLK or CDCE62005.
- 6. Change DDR3 1333 to 1600 by the Micron 1G X16.
- 7. Modify the boundary scan loop and remove the JTAG connections from the UCD9222 portion.
- 8. Change the PMBUS1 to 5Pin/2.54mm connector
- 9. UCD9222 changes:
 - a. Add a 10k pull-up resistor on the PMBUS_CTL and DNI it.
 - b. Add a 10k pull-down resistor on the JTAG_TSRT.
 - c. Remove the JTAG pins on the UCD9222 from the boundary scan chain.
 - d. Add a 10k pull-down resistor on the UCD9222_RST# and DNI it.
 - e. Separate analog GND to digital GND.
- 10. Add test points on all power rails.
- 11. Remove R443 on the PCIECLK to the DSP, put all ternmiantions next by PCIECLK MUX.
- 12. Install R440 on 9222_TCK, install R439 on PMBUS_CTL, might have a new firmware loading into the UCD9222 for the Beta2 and production units.
- 13. Pull down the BSC_JTAG_RST# for normal operation of phy.
- 14. Add H5 for AMC spec
- 15. Add pull up resistor (R908, R909) to the inputs to the switch so that these signals are held high when the AMC JTAG interface is selected.

- 16. Add 22-ohm series termination resistors at the outputs MCMTXPMCLK and MCMRXFLCLK which are HyperLink sideband signal clock outputs.
- 17. Add a temperature monitor to the unused TEMP2 input to the UCD9222
- 18. Add 4.7K pull-down resistors on the GPIO[15:1] pins and a 4.7K pull-up resistor on GPIO[0] so that these pins are not floating after FPGA release.
- 19. Replace the 14-pin JTAG with the Spy-Bi-Wire interface .
- 20. Add 0 Ohm resistors on all power enable signals.
- 21.ADD R485 for DSP UARTTXD termination
- 22.DSP_PCIECLOCK was set from IN2.
- 23.Change R425 and R426 package from 0603 to 0402.
- 24.Change R58 package from 0603 to 0402.
- 25. To modify the title from CLOCK GEN1 to CLOCK GEN3
- 26. Change net name from Isenes-2A to isenes-2A
- 27. U4, U5, U16, U17 U8 change to SAMSUNG_K4B1G1646G
- 28. NL/U8
- 29. NL/R431, NL/R432, Add R435

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- 1. Page26: Change mini-USB to through-hole type
- 2. Page13: Change the registers value to 2k ohms and the pull-up voltage to IO 1.8V on the DDR3 slew rate pins
- 3. Page22,23: Add the test points on unused clock inputs and outputs of CDCE62005s
- 4. Page10: Enable the expansion I2C by default, populate the registers of R160 and R161 for I2C connections between C6678 and AMC finger
- 5. Page23: Modify the CLK2 (CDCE62005) inputs for the common HyperLink timing,TCLKB will be the PRI_REF input and branch another one to the FPGA by two pairs. The 100MHz input from CLK3 CDCE62005 will be changed to its SEC_REF input.
- 6. AGND change to GND
- 7. Leave R160 and R161 as NL and add 2 more resistors on these nets connecting to AMC connector pins 159 and 160. Install 0 ohms in these new resistors

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- 1. Remove R484 and R487 and cross-wire these signals to make the connections functionally match the C6670 EVMs
- 2. Change R433 to 10k, change R434 to 1.2k, change R12 and R17 from 0 ohm to 0.1uF
- 3. Modify R183 and R134 from 4.7k to 1k

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