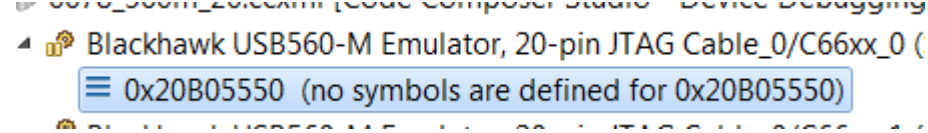


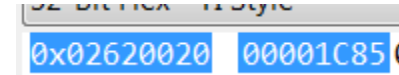
## How to test BOOTP C6678 EVM in BE mode

**Step 1: make sure under LE IBL Ethernet boot mode you can see bootp (this verifies your environment)**

Program Counter (PC):



DEVSTAT:



Wireshark:

66	15.6452470	0.0.0.0	0.0.0.0	BOOTP	342	Boot
78	18.7947570	0.0.0.0	0.0.0.0	BOOTP	342	Boot
93	21.9445800	0.0.0.0	0.0.0.0	BOOTP	342	Boot

**Step 2: Update IBL to big endian (use everything under latest MCSDK 2.1.2.6):**

- 1) eepromwriter\_evm6678l.out located at ..\tools\writer\eeeprom\evmc6678l\bin built in big endian mode. ===> you don't need to re-build it in big endian mode, just use it as it is for LE eeprom writer
- 2) Copied i2crom\_0x51\_c6678\_be.bin from ..\tools\boot\_loader\ibl\src\make\bin to ..\tools\writer\eeeprom\evmc667#l\bin. Copied file renamed to app.bin.
- 3) eepromwriter\_input.txt in ..\tools\writer\eeeprom\evmc6678l\bin. file\_name setequal to app.bin and bus\_addr equal to 0x51. Madesure start\_addr and swap\_data are set to 0.
- 4) EVM switched to No boot mode and LE mode.
- 5) Connect and gel file load.
- 6) eepromwriter\_evm6678l.out loaded on core 0.
- 7) Memory load of app.bin at 0x0C000000 (size 32-bits).

Format: Raw Data

Target

Start Address: 0x0c000000

Length: 0x326f

Note: "Length" represents the number of memory words.

Type-size: 32 bits

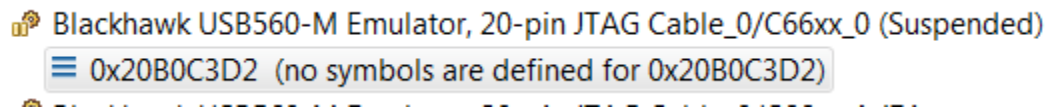
32-Bit Hex - TI Style	<input checked="" type="checkbox"/> L1D Cache	<input type="checkbox"/> L1P Cache	<input checked="" type="checkbox"/> L2 Cache			
0x0C000000	00004000	00002800	00000000	00080100	00005100	64000100
0x0C000018	0000C800	00000000	00000000	00000000	00000000	00000000
0x0C000030	00000000	00000000	00000000	00000000	00000000	00000000
0x0C000048	00000000	00000000	00000000	00000000	00000000	00000000
0x0C000060	00000000	00000000	00000000	00000000	00000000	00000000
0x0C000078	00000000	00000000	00004000	00002800	00000000	00080100
0x0C000090	00005100	64000100	0000C800	00000000	00000000	00000000

- 8) "EEPROM programming completed successfully" displayed at console.  
[C66xx\_0] EEPROM Writer Utility Version 01.00.00.05

Writing 51644 bytes from DSP memory address 0x0c000000 to EEPROM bus address 0x0051  
starting from device address 0x0000 ...  
Reading 51644 bytes from EEPROM bus address 0x0051 to DSP memory address 0x0c010000  
starting from device address 0x0000 ...  
Verifying data read ...  
EEPROM programming completed successfully

### STEP 3: Test IBL BE:

PC:



DEVSTAT

0x02620020	00001C84
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Wireshark:

Time	Source	Destination	Protocol	Length	Info
41.9.92986400	0.0.0.0	0.0.0.0	BOOTP	342	Boot
52.13.0795660	0.0.0.0	0.0.0.0	BOOTP	342	Boot
64.16.2292280	0.0.0.0	0.0.0.0	BOOTP	342	Boot