**C6678/C6670/C6657 MCSDK 2.1 PCIE example:**

**DEVSTAT (no boot)/ PCIE\_SERDES\_STS/PCIE\_SERDES\_CFGPLL**

 **RC**

 **EP**

**RC/EP**

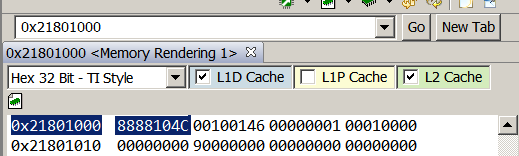
**RC/EP**

**Is PCIE Link up? (bit 4-0 should be 0x11 and stable)**

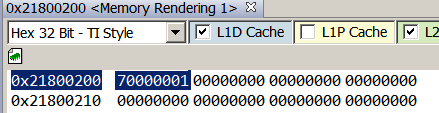
**RC/EP**

**RC side:**

BAR



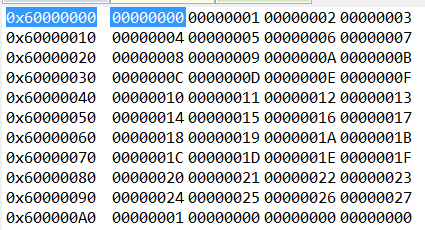
OB



IB

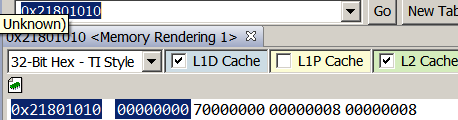


RC writes a test pattern to PCIE data region:

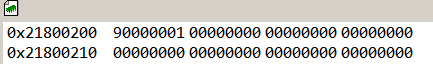


**EP side:**

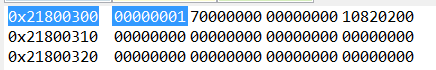
BAR



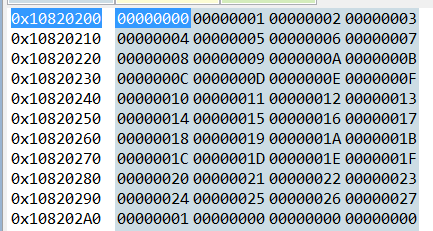
OB



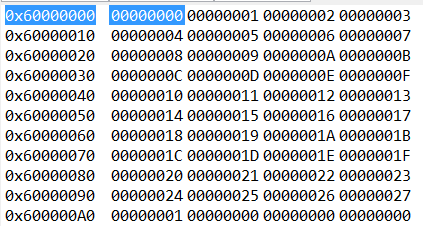
IB



EP should receive the data:



Then, EP loop data back by writing to PCIE data region



**RC side:**

Should receive the data

