Lightning

DSPC-8681E

Quad-TMS320C6678 DSP PCI-E HL Card

H/W Manual

Author:	
Status:	Version 0.3
Document ID:	
Location:	

History

Version	Date	Handled by	Comments
0.1	2012.01.06		Initial draft
0.2	2012.02.16		
0.3	2012.06.21		

Approved by

Date	Approve

Version Summary

Version	Changes
0.1	Initial draft
0.2	

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1. General

1.1 General Introduction

This document is the H/W user manual of DSPC-8681E, the PCI-E x8 Half-Length add-on card with quad-TMS320C6678 DSPs. DSPC-8681E is composed of four TI TMS320C6678 DSPs, one PCI-E GEN2 switch PEX8624 and one RJ45 LAN port.

1.2 Product Specifications

Below information describes the components designed on DSPC8681E PCI-E card.

DSP

- TI TMS320C6678 Multi-core Fixed and Floating-Point Digital Signal Processor.

DSP Memory

- 1024MB memory size on each DSP composed of 64-bit data width with four 2G bits DDR3-1333 x16 memory chips

FPGA

- XILINX XC3S200AN

Handle the DSPs' interrupt events, booting configurations, power sequences, and reset sequences and programming clock generator of CDCE62005 and the LVDS clock buffers.

PCI-express Switch

- PEX8624 (24 lanes / PCI-E GEN2)

Upstream port: PCI-E x8 to HOST, Downstream port: PCI-E x2 4-port to four DSPs.

Ethernet PHY

- BCM54616S

Support 10/100/1000 Mb/s with 1000BASE-T interface.

I/O Expansion

- Standard PCI-E x8 golden finger

I/O connector

- CN1: XILINX XC3S200AN JTAG interface.
- CN2: TI 60 pins DSP emulator connector.
- CN3: The DSP boundary scan connector.

- CN4: PEX8624 and BCM54616S boundary scan connector.
- CN5: RJ45 connector for LAN.
- CN6: FAN connector for the heatsink.
- COM1: 3 pins UART connector.
- 560V2_PWR1:XDS560v2 Mezzanine Power Connector.

Indicator

- Four LEDs, Debug LED1 to Debug LED4, are used for the FPGA XC3S200AN debugging.
- Five LEDs, P5_D1 to P5_D5, indicate available PCI-E ports.
- LED D2 indicates the error event of PEX8624.
- LED D3 indicates the interrupt event of PEX8624.
- LED SYSPG_D1 indicates that all power rails are stable.

EEPROM

- Four pieces of 1M bits I2C EEPROM are attached to four DSPs respectively. The EEPROM is contained of the DSP boot code and the initializations for the first boot while the card power-on and then branch to PCI-E interface for the second boot by the HOST computer.
- One piece of 128kbit SPI EEPROM is attached to PCI-E switch (PEX8624) for specific port configurations. No content is stored in the EEPROM.

Power Requirement

- 12V and 3.3V from PCI-E golden finger.

OS Verification

- Booting image (TBD).
- Application Program (TBD).

Environments

- Operating temperatures: -5°C to 45°C
- Storage temperatures: -20°C to 70°C
- Relative humidity: 5% to 95% (Non-condensing)

Certification

- CE/ FCC Class A
- UL/ CCC
- Compliant with RoHS

1.3 DSPC-8681E Block Diagrams

The internal connections on DSPC-8681E PCI-E card are described and shown as below figures.

The whole system interface block diagram for the Lightning broad is shown as Figure6. Each TMS320C6678 DSP contains several interfaces such as DDR, HyperLink, Serial RapidIO, PCIe, and SGMII for Ethernet connection.

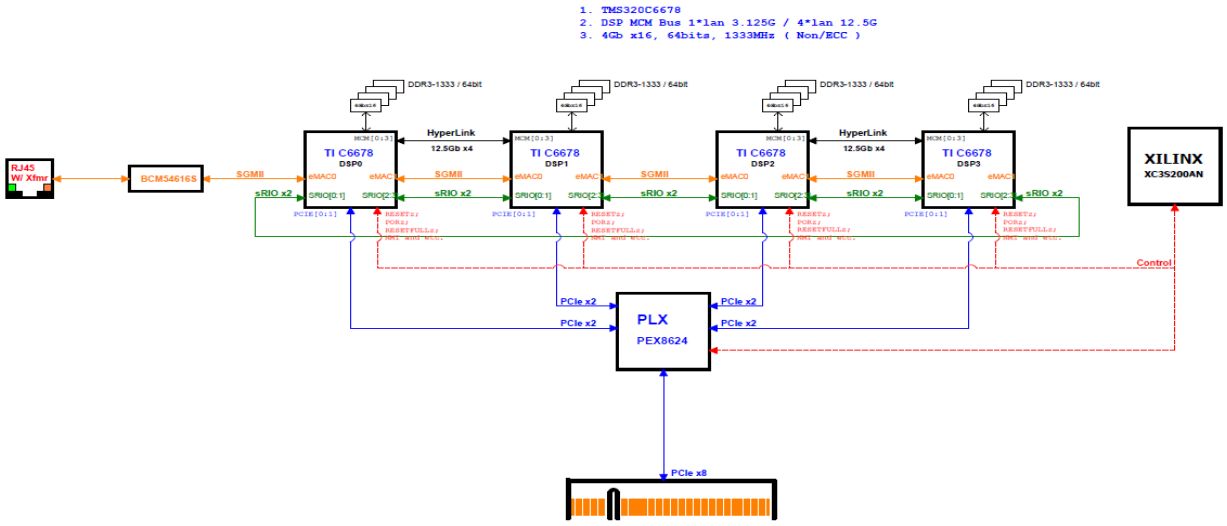

Figure1: DSPC-8681E System Block Diagram

1.4 DSPC-8681E PCI-E card Placement

Below figure shows main components on DSPC-8681E. It's only for reference if user needs to learn specific DSP or want to find a key chip on the card during developing.

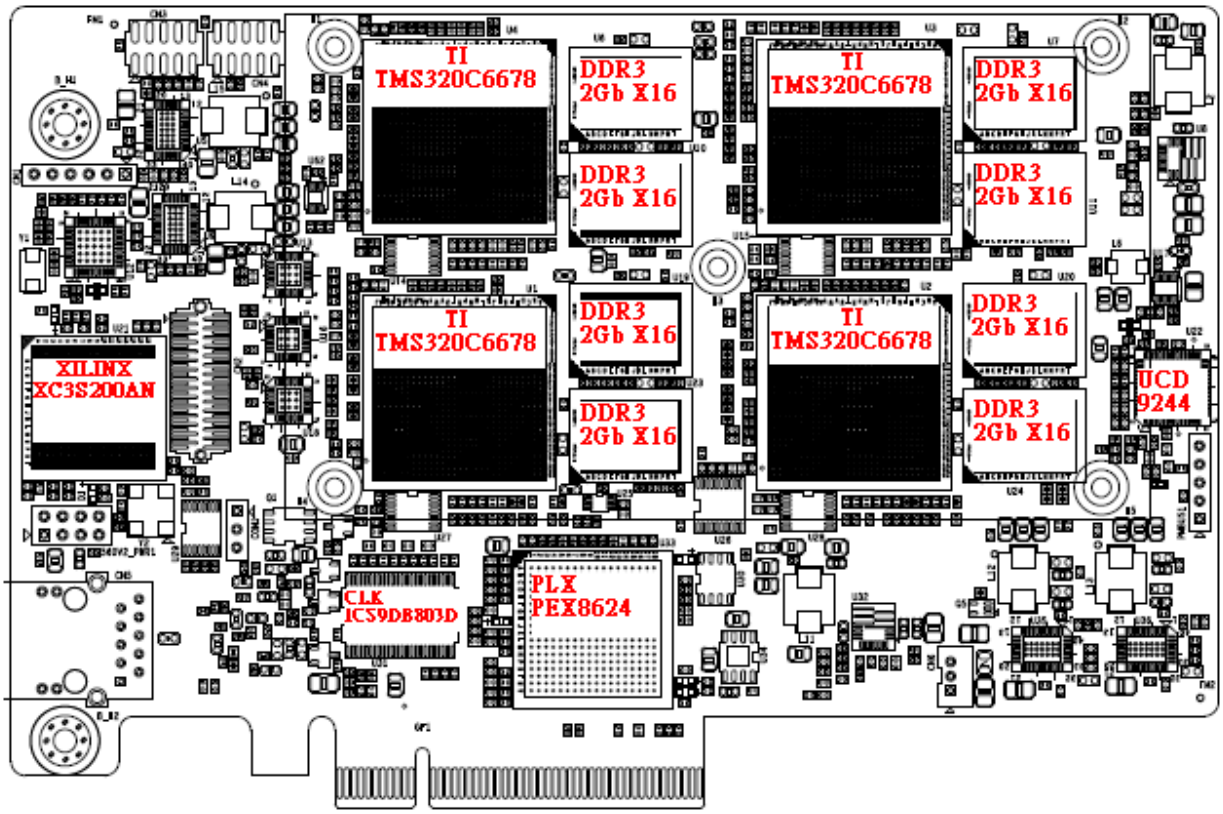

Figure2: DSPC-8681E PCI-E card Placement

2. Hardware Specification

2.1 Power Feed

The power source of DSPC-8681E is provided by two power rails, 12V and 3.3V from host, via PCI-E x 8 golden fingers.

2.2 Power Distribution

The major power on DSPC-8681E is illustrated as below Figure. Figure8 shows the power rails and the chips requirements on the DSPC-8681E. User could refer to DSPC-8681E schematics for more details regarding the power supplies on DSPC-8681E.

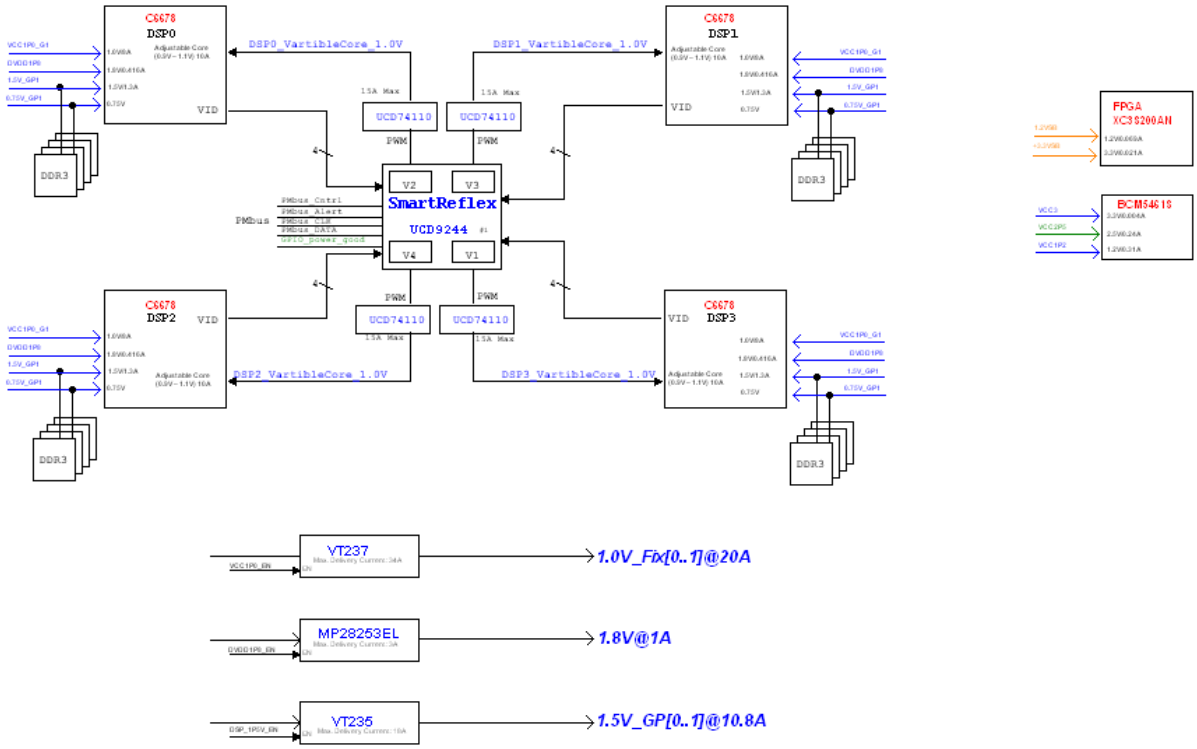

Figure3: Power Distribution Block Diagram

2.3 Power Budget

The estimated operational power budget of DSPC-8681E is about 52.751W. This value is estimated based on the assumption of the power dissipations and utilizations of the key components. For detailed number, it is summarized in the following table (Table1. DSPC-8681E Power Budget).

- VCC12 load= 6.882 A.
- VCC3.3 load=2.435 A
- Total power consumption (for EE Design) ~ 90.62W.
- Total power consumption (for Thermal Design) ~ 52.75W.
- Power budget table please refer to below.

						Max. Power Design			Operating (for Thermal)		
	PCIe full-length DSP card	V	I	Qty	Isub.	Efficiency	Pd (W)	12V(I)	3vsb(I)	Utilization	Pd (W)	Note
DSP CVDD (12V-->1.0V)												(UCD9244 + UCD7242)
	C6678	1.00	7.950	4	31.800	85%	37.412	3.118	x	70%	22.260	
VCC1V0 (12V-->1.0V)												VT237
	C6678	1.00	4.670	4	18.680	85%	21.976	1.831	x	70%	13.076	
VCC1V0 (12V-->1.0V)												MP28253EL
	PCIe SW (PEX8624)	1.00	2.600	1	2.600	85%	3.059	0.255	x	70%	1.820	
1.5V (12V-->1.5V)					8.988			1.322				VT237
	C6678	1.50	0.567	4	2.268	85%	4.002	0.334	x	70%	2.381	
	DDR3 (Micron_128Mx16)	1.50	0.420	16	6.720	85%	11.859	0.988	x	70%	7.056	
1.8V (12V-->1.8V)					0.736							MP28253EL
	C6678	1.80	0.184	4	0.736	80%	1.656	0.138	x	70%	0.927	
3.3V					0.860							
	FPGA (XC3S200AN)	3.30	0.056	1	0.056	80%	0.231	x	0.070	70%	0.129	
	ICS9DB803D	3.30	0.200	1	0.200	80%	0.825	x	0.250	70%	0.462	
	PHY (BCM5461S)	3.30	0.004	1	0.004	80%	0.017	x	0.005	70%	0.009	
	CDCE62005	3.30	0.350	1	0.350	80%	1.444	x	0.438	70%	0.809	
	Others	3.30	0.250	1	0.250	80%	1.031	x	0.313	70%	0.578	
	2.5V (3.3V-->2.5V)				0.730							APL5912KAC-TRG (LDO)
	PCIe SW (PEX8624)	2.50	0.090	1	0.090	60%	0.375	x	0.114	70%	0.158	
	PHY (BCM5461S)	2.50	0.190	1	0.190	60%	0.792	x	0.240	70%	0.333	
	CDCLVD110A	2.50	0.150	3	0.450	60%	1.875	x	0.568	70%	0.788	
	1.2V_AUX (3.3V-->1.2V_AUX)				0.560							APL5912KAC-TRG (LDO)
	PHY (BCM5461S)	1.20	0.310	1	0.310	40%	0.930	x	0.282	70%	0.260	
	FPGA (XC3S200AN)	1.20	0.250	1	0.250	40%	0.750	x	0.227	70%	0.210	
Power loss		x	x	x	x	x	x	x	x	20%	10.251	
Total power consumption							Pmax.	12V(I)	3VSB(I)		Pop.	
							88.233	6.664	2.506		51.255	

Table 1: DSPC-8681E Power Budget

2.4 Power Sequence

DSPC-8681E consists of many devices on it, including DSP, PCIe switch, PHY & FPGA etc. Hence, the power sequence is designed to meet all devices' power-on requirements. And the timing parameters are shown in below table (Table2. System Power Sequence Parameter) while the power sequence is shown in below figure (Figure9. DSPC-8681E overall power sequence).

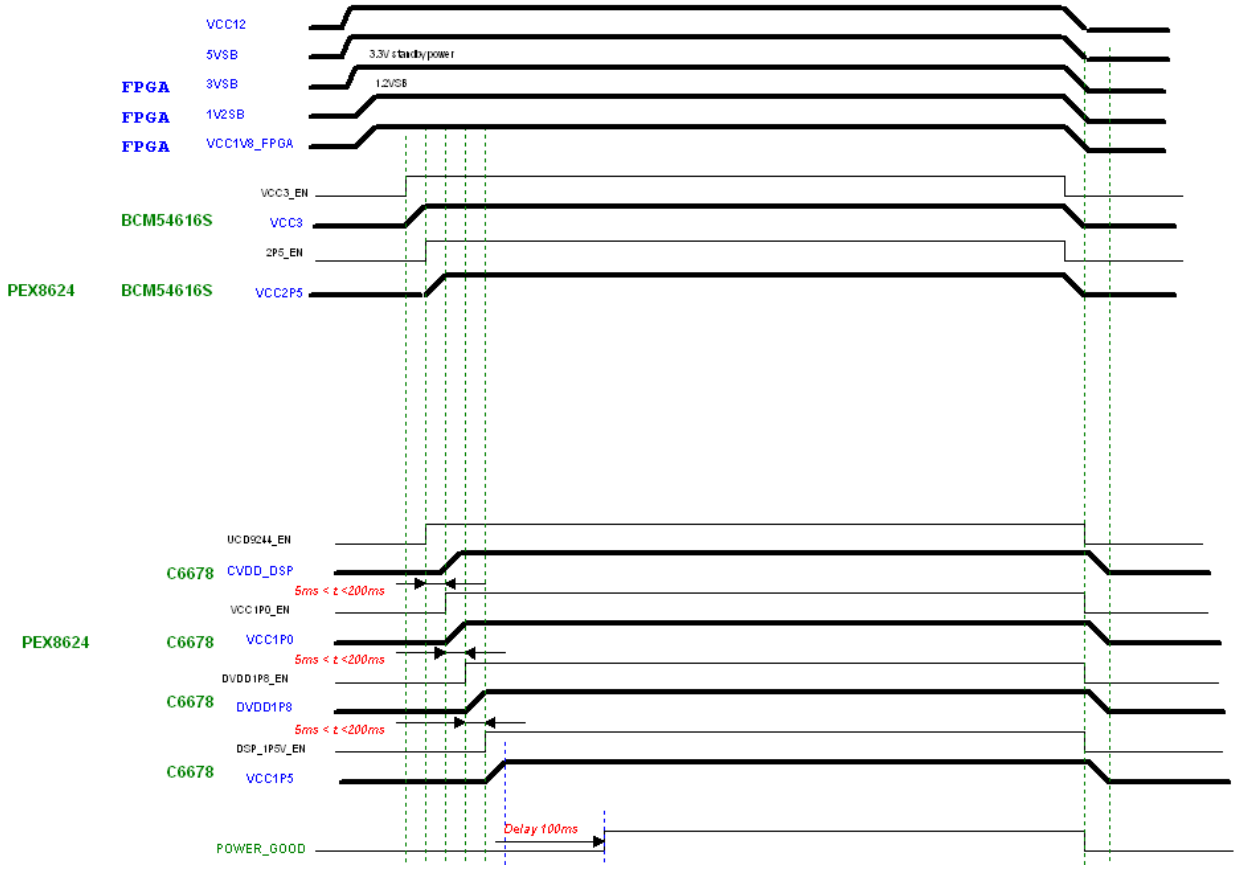

Figure4: DSPC-8681E overall power sequence

Sym	Parameter	Timing	Note
T0	VCC1P0_EN is ramped up after UCD9244_EN.	5ms<t<200ms	
T1	VCC1P8_EN is ramped up after VCC1P0_EN.	5ms<t<200ms	
T2	VCC1P5V_EN is ramped up after VCC1P8_EN.	5ms<t<200ms	
T3	POWER_GOOD is asserted after the last power rail(VCC1P5V)	t>100ms	

Table 2: System Power Sequence Parameter

For the power sequence on each main component are designed based on the specifications of each chipset and shown in below figure (Figure 5. Power distribution on DSPC-8681E PCIe card).

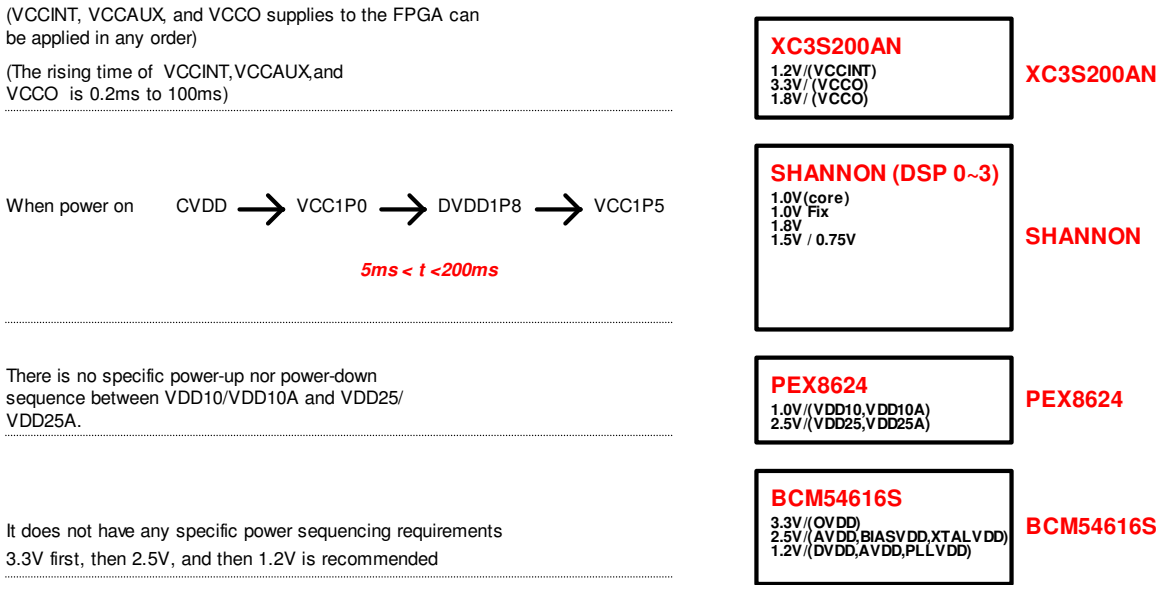

Figure 5: Power Distribution on DSPC-8681E PCIe Card

2.5 Platform Clock

The DSPC-8681E clocks are generated by the clock synthesizers, crystals and oscillators. Introductions for each clock are described as below.

CDCE62005: It's a Low-Jitter clock generator with 25.0MHz crystal. It's programmed to provide 166.66MHZ, 250MHZ and 100MHz with LVDS level for the DSP reference clocks.

ICS9D803D: It's a PCI-E GEN2 clock buffer and provides five reference clocks to the PCI-E switch by HCSL and to the DSP PCI-E clocks by LVDS level.

CDCLVD110A: It's a 1:10 LVDS clock buffer. There are three clock buffers whic fan out 166.66MHZ, 250MHZ and 100MHz to each DSP for the reference clocks of core, DDR3, HyperLink and SRIO/SGMII interfaces.

The platform clock distribution scheme is illustrated as the below Figure (Figure11. DSPC-8681E Carrier Clock Feeding Diagram).

Signal	Frequency	Source	Device
DSP0_DDR_CLKP DSP0_DDR_CLKN	166.67MHz	TI_CDCLVD110ARHBR U18	DSP0 U1
DSP1_DDR_CLKP DSP1_DDR_CLKN	166.67MHz	TI_CDCLVD110ARHBR U18	DSP1 U2
DSP2_DDR_CLKP DSP2_DDR_CLKN	166.67MHz	TI_CDCLVD110ARHBR U18	DSP2 U3
DSP3_DDR_CLKP DSP3_DDR_CLKN	166.67MHz	TI_CDCLVD110ARHBR U18	DSP3 U4
DSP0_CORE_CLKP DSP0_CORE_CLKN	100.00MHz	TI_CDCLVD110ARHBR U13	DSP0 U1
DSP1_CORE_CLKP DSP1_CORE_CLKN	100.00MHz	TI_CDCLVD110ARHBR U13	DSP1 U2
DSP2_CORE_CLKP DSP2_CORE_CLKN	100.00MHz	TI_CDCLVD110ARHBR U13	DSP2 U3
DSP3_CORE_CLKP DSP3_CORE_CLKN	100.00MHz	TI_CDCLVD110ARHBR U13	DSP3 U4
DSP0_SRIOSGMII_CLKP DSP0_SRIOSGMII_CLKN	250.00MHz	TI_CDCLVD110ARHBR U16	DSP0 U1
DSP1_SRIOSGMII_CLKP DSP1_SRIOSGMII_CLKN	250.00MHz	TI_CDCLVD110ARHBR U16	DSP1 U2
DSP2_SRIOSGMII_CLKP DSP2_SRIOSGMII_CLKN	250.00MHz	TI_CDCLVD110ARHBR U16	DSP2 U3
DSP3_SRIOSGMII_CLKP DSP3_SRIOSGMII_CLKN	250.00MHz	TI_CDCLVD110ARHBR U16	DSP3 U4
DSP0_PCIE_REF_CLKP DSP0_PCIE_REF_CLKN	100.00MHz	IDT_ICS9DB803DFLFT U31	DSP0 U1
DSP1_PCIE_REF_CLKP DSP1_PCIE_REF_CLKN	100.00MHz	IDT_ICS9DB803DFLFT U31	DSP1 U2
DSP2_PCIE_REF_CLKP DSP2_PCIE_REF_CLKN	100.00MHz	IDT_ICS9DB803DFLFT U31	DSP2 U3
DSP3_PCIE_REF_CLKP DSP3_PCIE_REF_CLKN	100.00MHz	IDT_ICS9DB803DFLFT U31	DSP3 U4
DSP0_MCM_CLKP DSP0_MCM_CLKN	250.00MHz	TI_CDCLVD110ARHBR U16	DSP0 U1
DSP1_MCM_CLKP DSP1_MCM_CLKN	250.00MHz	TI_CDCLVD110ARHBR U16	DSP1 U2
DSP2_MCM_CLKP DSP2_MCM_CLKN	250.00MHz	TI_CDCLVD110ARHBR U16	DSP2 U3

Signal	Frequency	Source	Device
DSP3_MCM_CLKP DSP3_MCM_CLKN	250.00MHz	TI_CDCLVD110ARHBR U16	DSP3 U4
54616_XTALO 54616_XTALI	25.00MHz	Crystal	BCM54616SC0KFBG U58
MAIN_48MHZ_CLK_R	48.00MHz	Oscillator	XILINX XC3S200AN U21
PCIE_REF_CLK_P PCIE_REF_CLK_N	100MHz	PCI-E Gold Finger GF1	ICS9DB803DFLFT U31

Table 3: Clock Domains

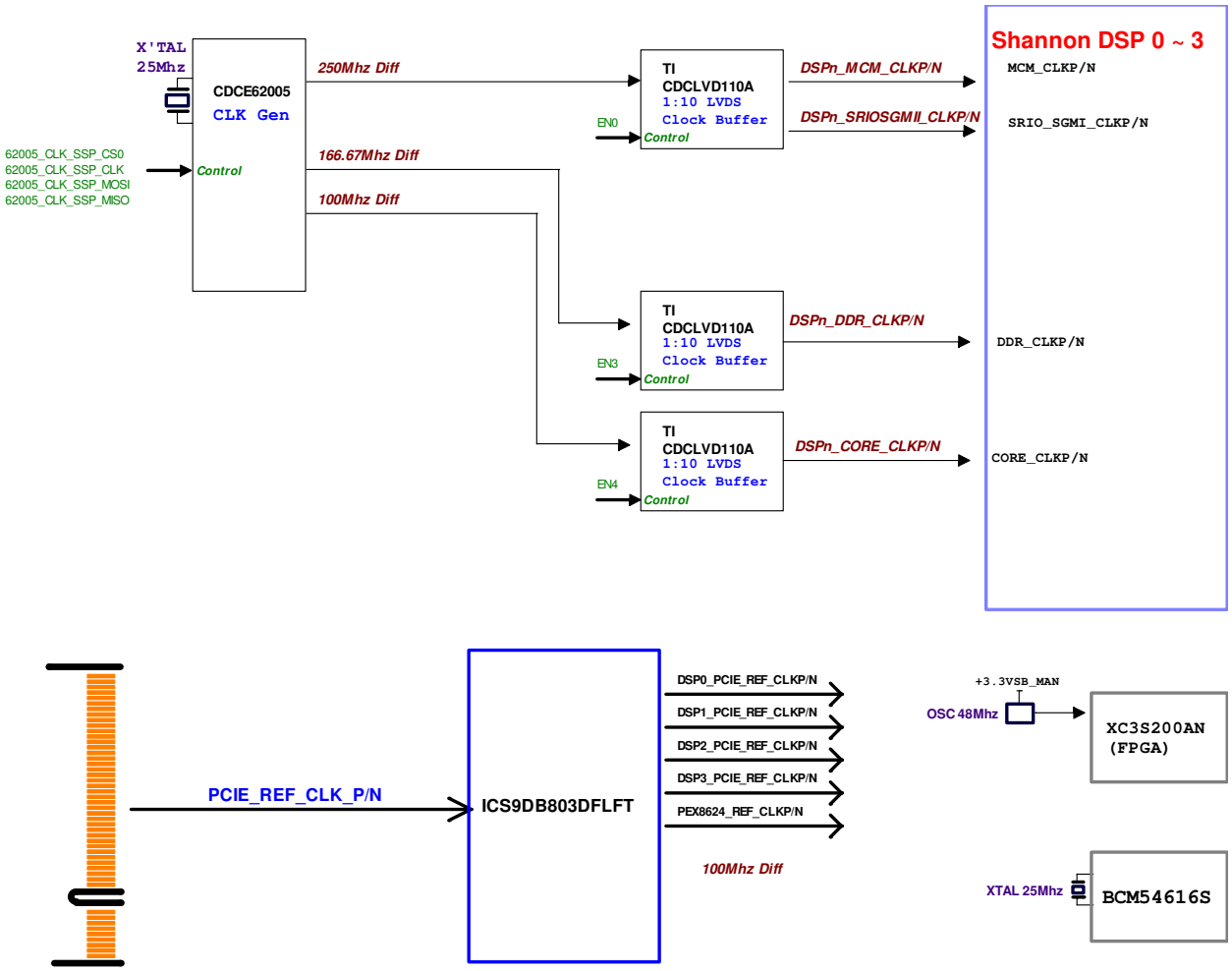

Figure6: DSPC-8681E Carrier Clock Feeding Diagram

2.6 Reset Block Diagram

DSPC-8681E reset mechanism is shown in Figure 12. DSPC-8681E Reset Block Diagram with below description of the reset sequence on DSPC-8681E.

- The FPGA on the card will do the power-on sequence and make all power rails on the card be ready.
- The FPGA waits for the PWROK on PCI-E golden finger (PCIE_GF_RST#) asserted.
- After PCI-E PWROK asserted as well as all the power on the card valid, the FPGA will de-assert SYS_RESETz of PEX8624, the PCI-E switch, PHY_RESETz of BCM54616s, the PHY chip, and DSP[0:3]_RESET# on four DSP chips.
- To wait for 5mS, the FPGA de-assert the DSP_POR# to four DSPs.
- To wait for 5mS, the FPAG de-assert the DSP_RESETFULLz to four DSPs.
- During DSP_RESETFULLz de-asserted, the DSP straps the boot configurations on its own GPIO pins driven by the FPAG.
- 1ms later after DSP_RESETFULLz de-asserted, the FPGA will set the GPIO pins on the FPGA side at input, after that, the reset sequence on DSPC-8681E is completed then.

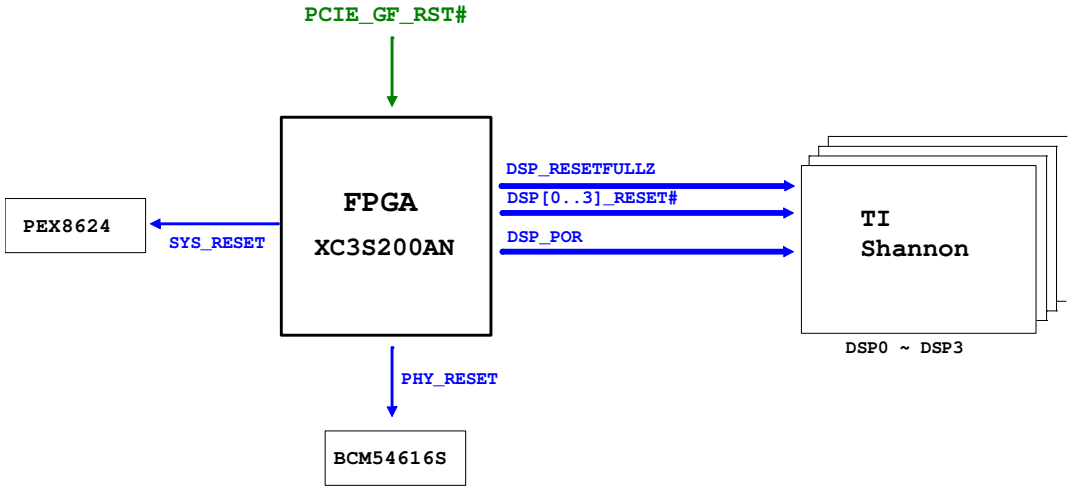

Figure7: DSPC-8681E Reset Block Diagram

2.7 Reset Sequence

Below figure is provided by TMS320C6678 data manual which describes the reset timings related to DSP power rails (CVDD, CVDD1, DVDD15 and DVDD18), reference clocks (core clock and DDR3 clock) and three reset events (RESETz, PORz and RESETFULLz). User can refer to TMS320C6678 Data Manual on TI webpage for the details.

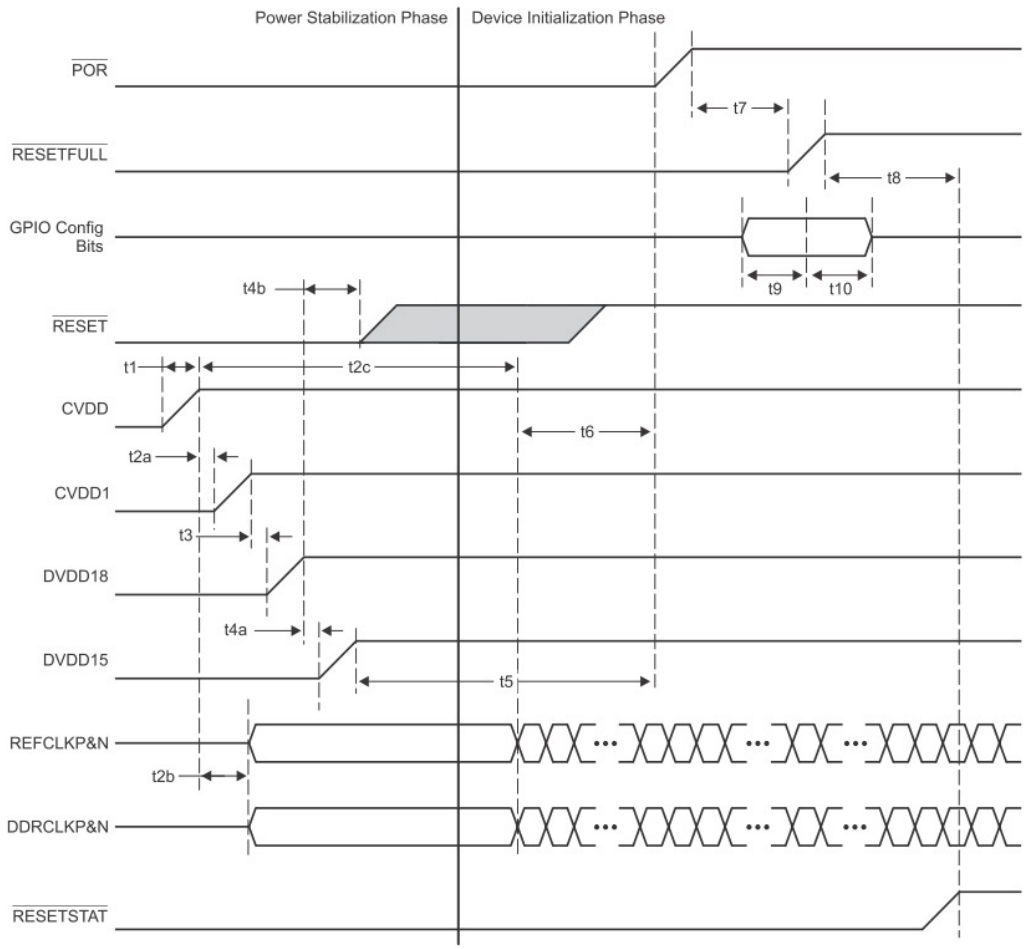

Figure8: The DSP Reset Sequence on DSPC-8681E

2.8 DSP (TI TMS320C6678) Block Diagram

The DSPC-8681E PCI-E add-on card adopts TI 8-core DSP TMS320C6678 and its core frequency is 1000MHz.

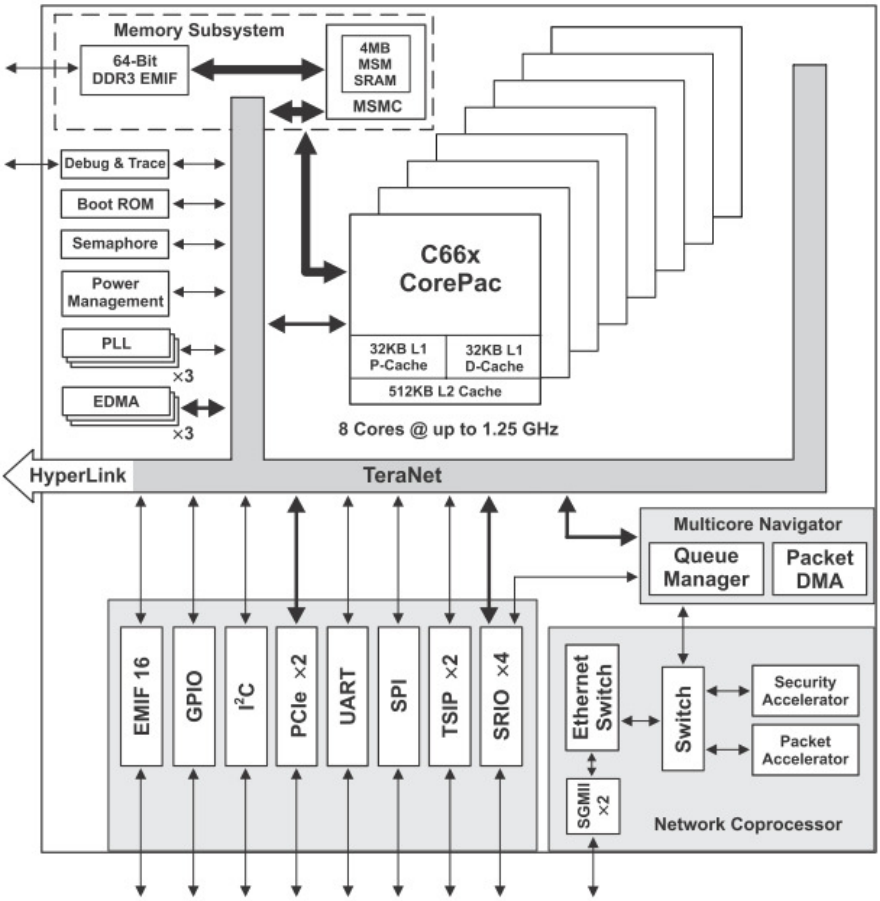

Figure9: TI TMS320C6678 Block Diagram

2.9 Memory (DDR3)

Four DDR3 memory devices are populated for each DSP on the DSPC-8681E PCI-E add-on card. The RAM speed is 1333MHz while each DSP connects to four 2G bit (128M x 16) DDR3 devices via DDR interface.

2.10 SRIO interface

For SRIO connection, DSPC-8681E adopts a ring topology to chain four DSPs by one lane SRIO interface. One SRIO lane is connected to previous DSP while another lane is connected to next DSP on DSPC-8681E, e.g. the DSP#3 connects the DSP#0 with x1 SRIO port and connect the DSP#2 with another x1 SRIO port.

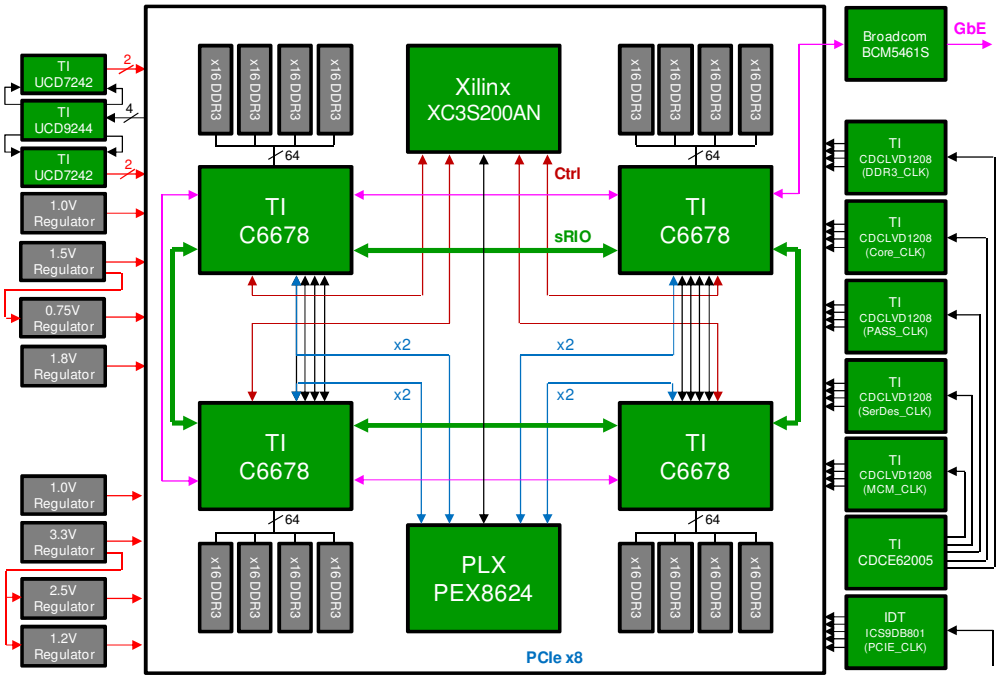

Figure10: Serial RapidIO Ring

2.11 PCI-E interface

DSPC-8681E adopts a star topology to link host platform with two-lane PCIE interface via a PCI-E GEN2 switch, PEX8624. One PCI-E Gen2 port is designed with two Lanes (Supports Up To 5G baud Per Lane) connected to each DSP.

With PEX8624, it can support up to six PCI Express GEN ports with 24 lanes of integrated on-chip SerDes and provide an aggregated bandwidth of up to 240 GT/s.

Below table describes the port mapping of PEX8624 on DSPC-8681E while below figure describes the PCIe interconnection on DSPC-8681E.

Port	Function
0	Connects to Host computer (Root Complex) by PCI-E X8
5	Connects to DSP0 through PCI-E X2 interface
6	Connects to DSP1 through PCI-E X2 interface
8	Connects to DSP2 through PCI-E X2 interface
9	Connects to DSP3 through PCI-E X2 interface

Table 4: PCI-E port mapping on PEX8624

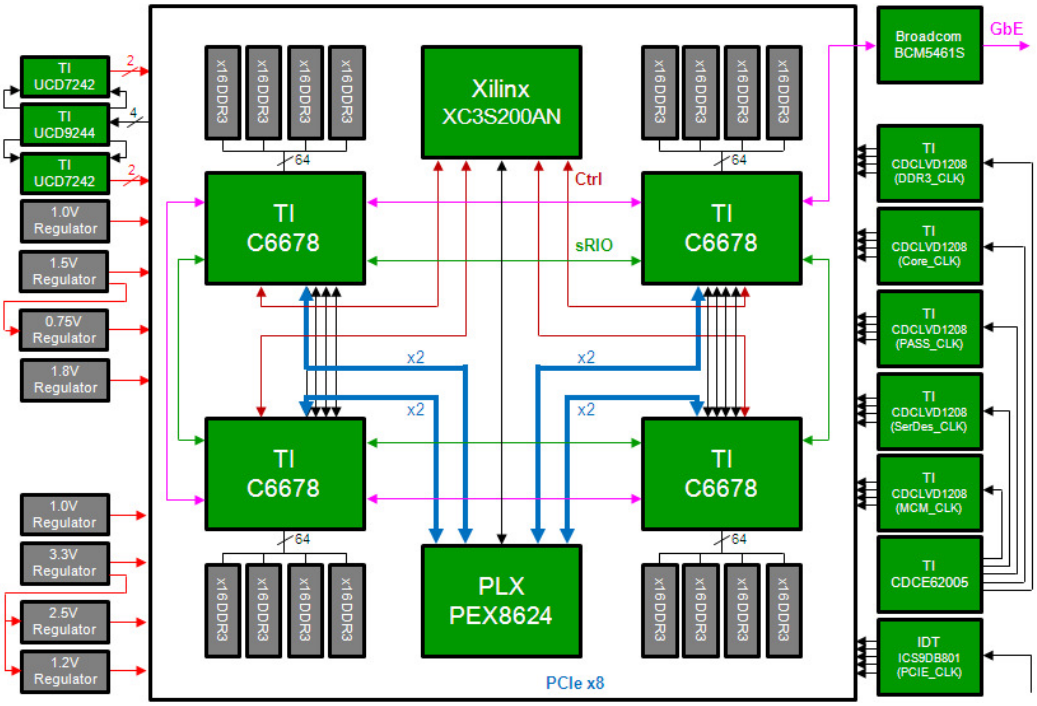

Figure11: PCIe interconnection

2.12 Ethernet MAC

There are two Gigabit Ethernet MACs in DSP TMS320C6678 and are connected by SGMII SERDES interface. Therefore, the route of LAN packets is forwarded orderly by LAN port, DSP#0, DSP#1, DSP#2 and DSP#3. On DSPC-8681E, a daisy chain for LAN connections in implemented whereas the LAN port is connected to DSP#0 via a PHY, BCM54616s, to provide 1000BASE-T Gigabit Ethernet feature.

With Ethernet PHY BCM54616S, it supports Ethernet 10/100/1000M bit/s with SGMII interface and integrates triple-speed Ethernet transceiver-MAC to magnetic, including 1000BASE-T IEEE 802.3ab, 100BASE-TX IEEE802.3u and 10BASE-T IEEE 802.3.

Below figure describes the LAN connection on DSPC-8681E.

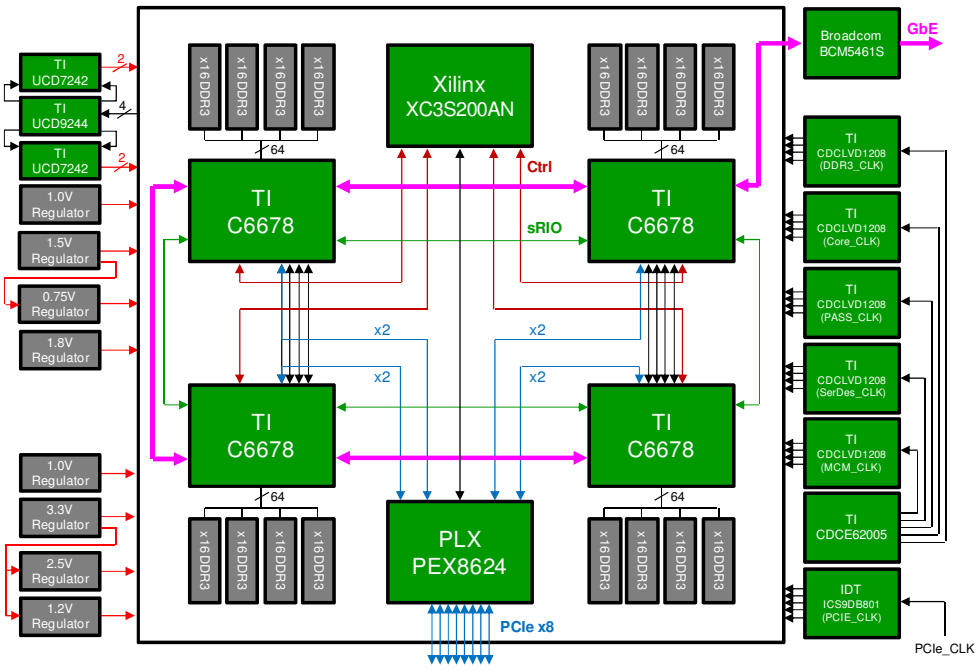

Figure12: LAN interconnection

2.13 HyperLink interface

Another high-speed interlink, named HyperLink, is implemented on DSPC-8681E to connect each two DSPs (DSP#0 – DSP#1 and DSP#2 – DSP#3) as a pair, and its interface can provide up to 50GT/s (12.5GT/s per lane) for data transactions.

This HyperLink interface on the TMS320C6678 is used to exchange data between two DSPs with low latency for the specific process accelerations on DSPC-8681E PCIE card. There are four-lane SerDes interface designed to operate up to 12.5Gbps per lane. The links of the HyperLink bus on DSPC-8681E are connected of the DSP#0 and the DSP#1 as well as the DSP#2 and DSP#3.

Below figure describes the Hyperlink connection on DSPC-8681E.

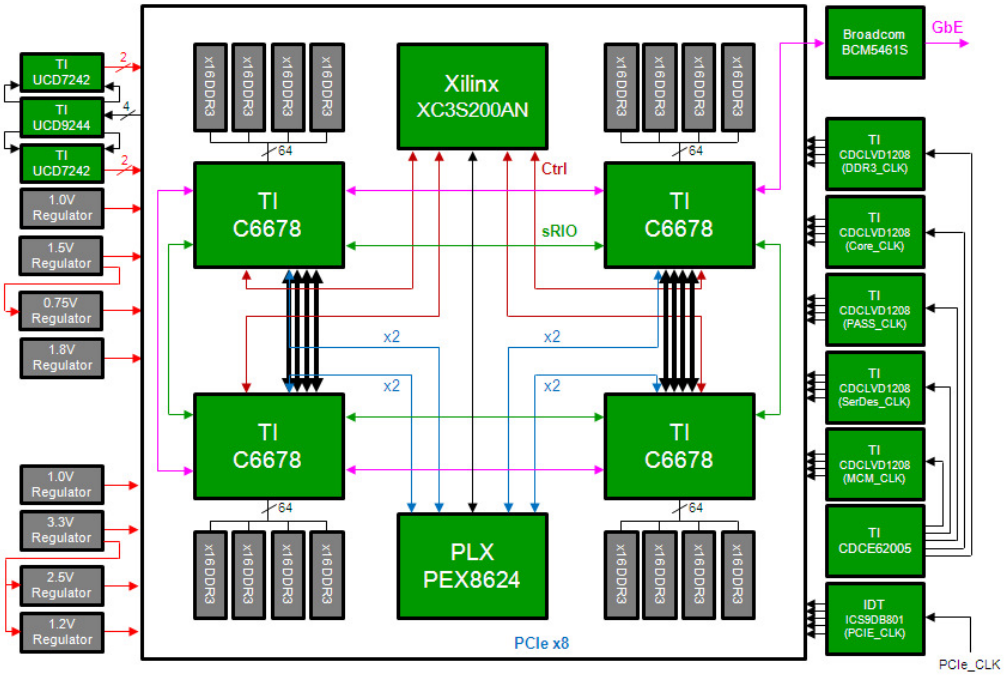

Figure13: Hyperlink connection

2.14 FGPA XC3S200AN

For FPGA design, Xilinx XC3S200AN is implemented on DSPC-8681E for the power control, DSP boot configurations, programming clock generators and clock buffers and reset events for DPS farm.

With the programmed FPGA on DSPC-8681E, below functions are provided.

- DSP boot mode setting
- Power sequences control
  - Enabling / Disabling the device power to meet the power sequence requirement.
- Reset methodology control
  - Asserting / De-asserting RESET signals to each chip respectively.
- Configure the clock generator
- Other control functions

Below figure describes the FPGA connection on DSPC-8681E.

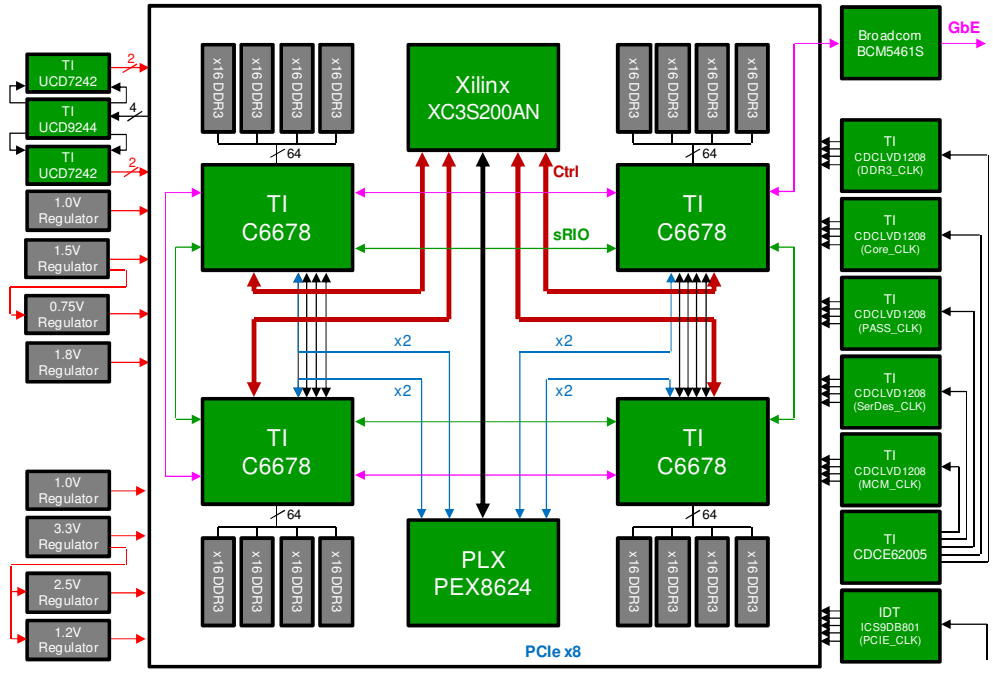

Figure14: FPGA connection

2.15 LEDs

The locations of the LED indicators on the DSPC-8681E are shown by below figures. User can find the indicators easily for specific purpose. The detail descriptions are listed by following sections.

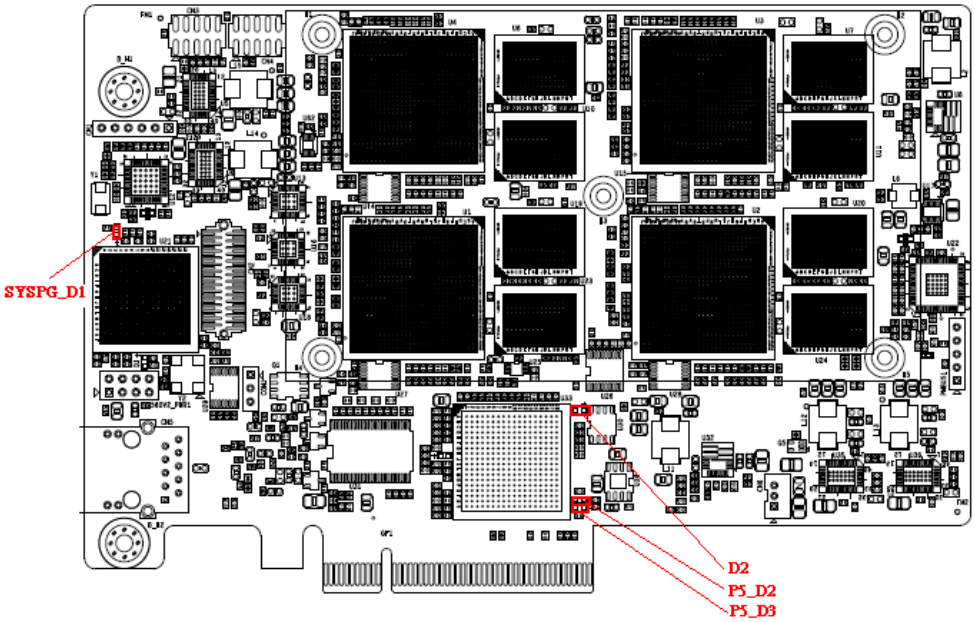

Figure15: TOP Side LED Location

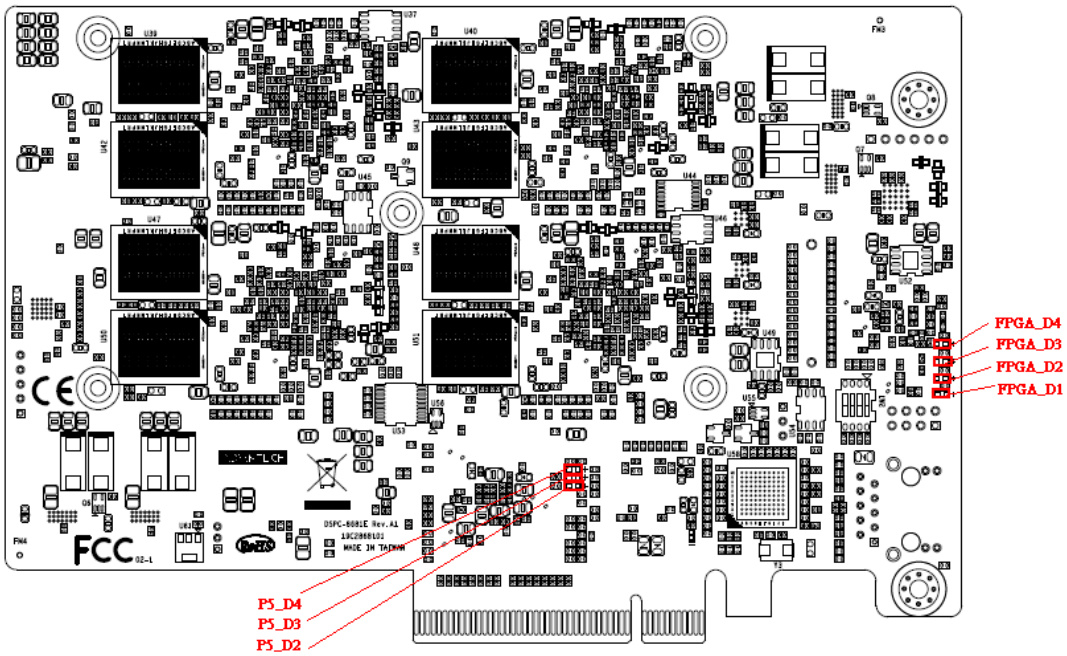

Figure16: BOTTOM Side LED Location

There are many LEDs near PEX8624, these LEDs indicates whether the PCIe ports are available or not. Details are shown below (Table5).

LED	Function
P5_D5	Port-0 good
P5_D1	Port-9 good
P5_D2	Port-8 good
P5_D3	Port-6 good
P5_D4	Port-5 good
D2	PEX8624 error
D3	PEX8624 interrupt

Table5: PCI-E switch LED

Some LEDs are near XC3S200AN. Four LEDs are used for code debugging and one LED indicates that all power rails are good. Details are shown as below (Table6).

LED	Port
SYSPG_D1	All power rails are good.
FPGA_D1	Debug LED_0
FPGA_D2	Debug LED_1
FPGA_D3	Debug LED_2
FPGA_D4	Debug LED_3

Table6: FPGA LED

Some LEDs are built in RJ-45 connector for RJ-45 behavior. The right side LED blinks with green color when activity occurs normally. The left side LED presents green color when 1000 BASE-T link is established. The left side LED present orange color when 100 BASE-TX link is established. If left side LED is dark, it means 10 BASE-T link is established or no link is established.

3. IO Connector

3.1 Connector Overview

This section describes the pin definition of the connectors on the DSPC-8681E PCIE card. User can have a detail on the pin signals for further use. For more details, please refer to the related documents from the website of the manufacturer.

- CN1: XILINX XC3S200AN JTAG, for the FPGA debugging and new firmware updating.
- CN2: TI 60-pin DSP emulator connector, for software development.
- CN3: The DSP boundary scan connector, for facility test only.
- CN4: PEX8624 and BCM54616S boundary scan connector, for the purpose of the facility test.
- CN5: RJ45 connector, Giga Ethernet port connected to DSP#0 for networking applications.
- CN6: FAN connector, for the FAN attached on the heat sink.
- COM1: 3-pin UART connector, connected to DSP#0 for the software development.
- 560V2_PWR1: XDS560v2 Mezzanine Power Connector.

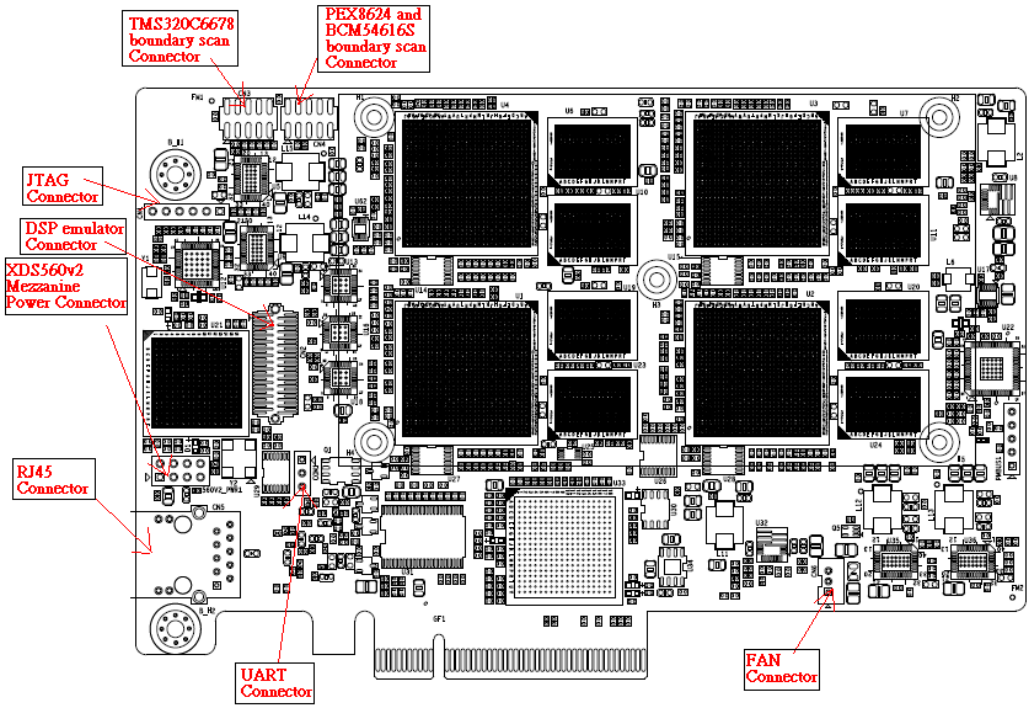

Figure17: Connector Overview

3.2 XILINX XC3S200AN JTAG interface

In this paragraph, we introduce the connector for Xilinx XC3S200AN JTAG interface.

CN1: XILINX XC3S200AN JTAG interface

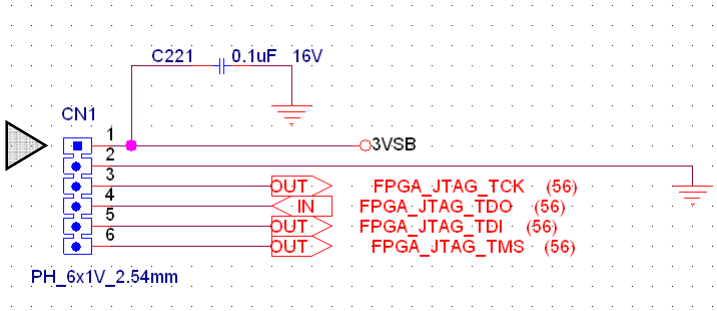

Figure18: CN1, the FPGA JTAG for firmware update

PIN	Define
1	VCC
2	GND
3	TCK
4	TDO
5	TDI
6	TMS

Table7: CN1 Pin Assignment

3.3 60 pins DSP emulator connector

In this paragraph, we introduce the 60-pin DSP emulator connector used for XDS562V2.

CN2: 60 pins DSP emulator connector

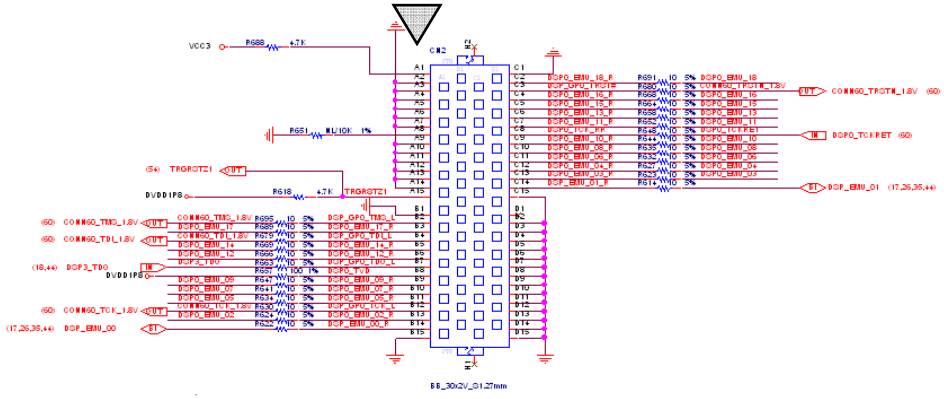

Figure19: CN2, TI 60-pin Emulation Connector

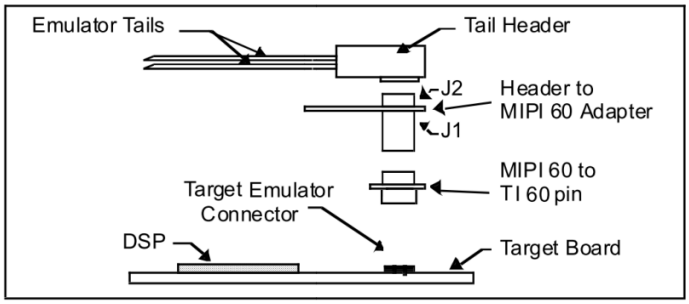

Figure20: Connection the XDS560v2 STM Emulator

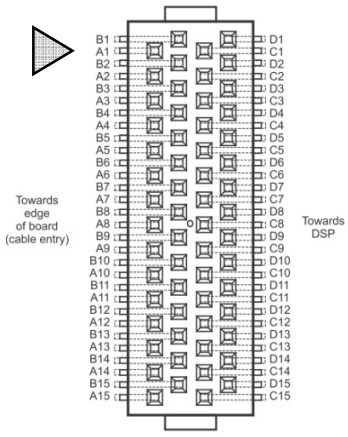

Figure21: 60-pin Header Orientation

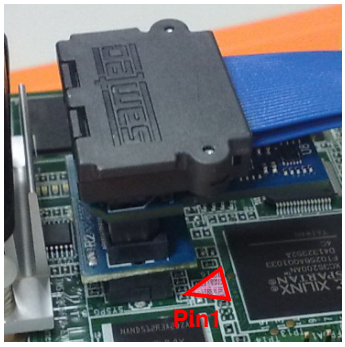

Figure22: The connection with TI XDS560v2 STM Emulator

Col / Row	A	B	C	D
1	GND	GND	GND	NC
2	GND	TMS	EMU18	GND
3	GND	EMU17	TRST#	GND
4	GND	TDI	EMU16	GND
5	GND	EMU14	EMU15	GND
6	GND	EMU12	EMU13	GND
7	GND	TDO	EMU11	GND
8	Reserve	TVD	TCLKRTN	GND
9	GND	EMU9	EMU10	GND
10	GND	EMU7	EMU8	GND
11	GND	EMU5	EMU6	GND
12	GND	TCLK	EMU4	GND
13	GND	EMU2	EMU3	GND
14	GND	EMU0	EMU1	GND
15	TGRST#	GND	GND	GND

Table8: CN2 DSP Emulator Pin Assignments

3.4 TMS320C6678 Boundary Scan Connector

In this paragraph, we introduce the boundary scan connector from the TMS320C6678 DSP.

CN3: TMS320C6678 boundary scan connector

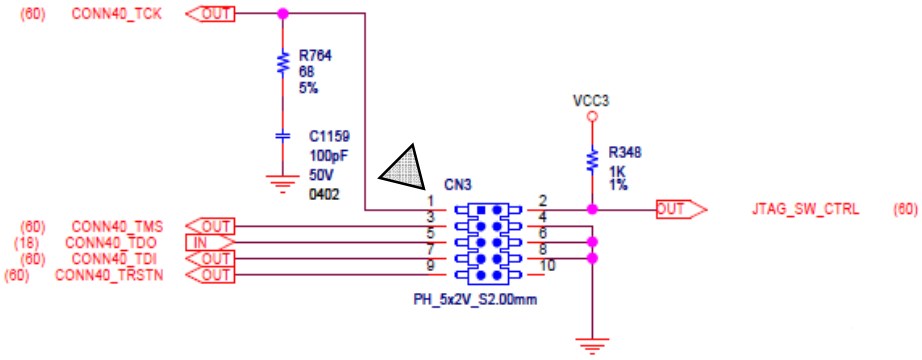

Figure23: CN3, the Boundary Scan for the DSP farm

PIN	Define	PIN	Define
1	TCK	2	PLUG_DETn
3	TMS	4	NC
5	TDO	6	GND
7	TDI	8	GND
9	TRSTn	10	GND

Table9: CN3 Pin Assignment

3.5 PEX8624 and BCM54616S boundary scan connector

In this paragraph, we introduce the boundary scan connector for PEX8648 and BCM54616S.

CN4: PEX8624 and BCM54616S boundary scan connector

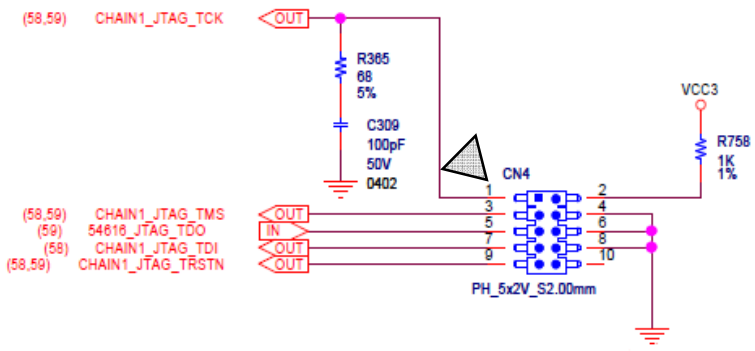

Figure24: CN4, Boundary Scan for PEX8624 and BCM54616s

PIN	Define	PIN	Define
1	TCK	2	PLUG_DETn
3	TMS	4	NC
5	TDO	6	GND
7	TDI	8	GND
9	TRSTn	10	GND

Table10: CN4 Pin Assignment

3.6 RJ45 LAN connector

In this paragraph, we introduce the RJ45 connector.

CN5: RJ45 connector

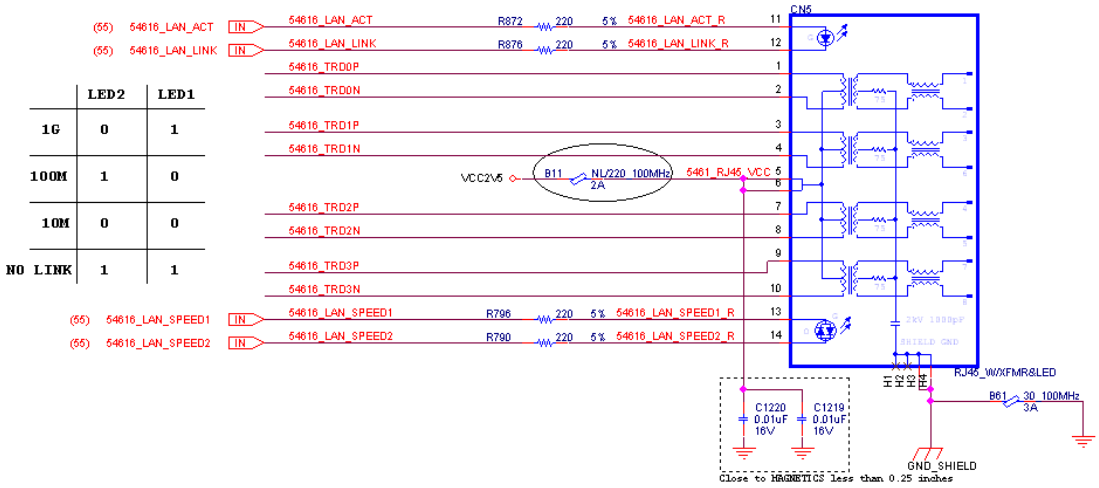

Figure25: CN5, RJ45 LAN port

PIN	Define	PIN	Define
1	TRD0P	8	TRD2N
2	TRD0N	9	TRD3P
3	TRD1P	10	TRD3N
4	TRD1N	11	LED_ACK
5	VCC	12	LED_LINK
6	VCC	13	LED_SPEED1
7	TRD2P	14	LED_SPEED2

Table11: CN5 Pin Assignment

3.7 FAN connector

In this paragraph, we introduce the FAN connector.

CN6: FAN connector

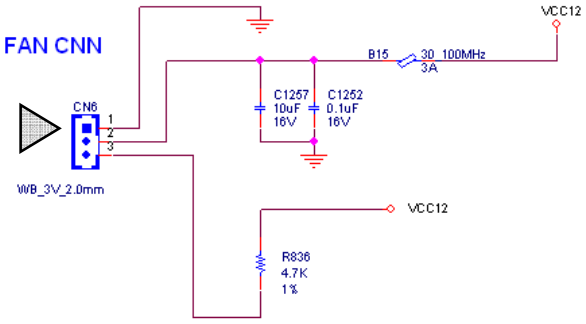

Figure26: CN6, FAN connector

PIN	Define
1	GND
2	VCC
3	VCC

Table12: CN6 Pin Assignment

3.8 UART connector

In this paragraph, we introduce the 3-pin UART connector.

COM1: 3 pins UART connector

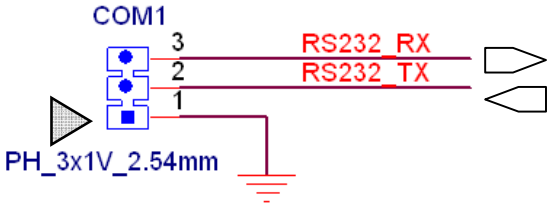

Figure27: COM1, UART pin out

PIN	Define
1	RX
2	TX
3	GND

Table13: COM1 Pin Assignment

3.9 XDS560v2 Mezzanine Power Connector

In this paragraph, we introduce the XDS560v2 Mezzanine Power Connector.

560V2_PWR1: 8-pin power connector for the XDS560v2 mezzanine emulator board.

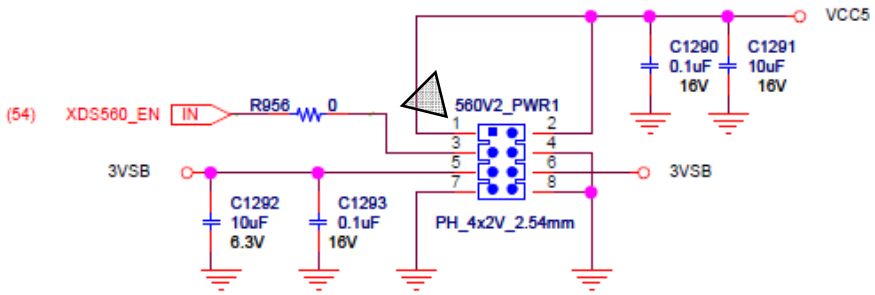

Figure28: 560V2_PWR1 Connector

PIN	Define	PIN	Define
1	VCC5	2	VCC5
3	XDS560_EN	4	GND
5	3VSB	6	3VSB
7	GND	8	GND

Table14: 560V2_PWR1 Pin Assignment

4. Jumper and Switch setting

There is one 4-bit sliding switch (SW1) on the board to set the Endian, boot devices and variety of BRA size for the DSP farm by the FPGA.

Below figure shows the position of the 4-bit sliding switch.

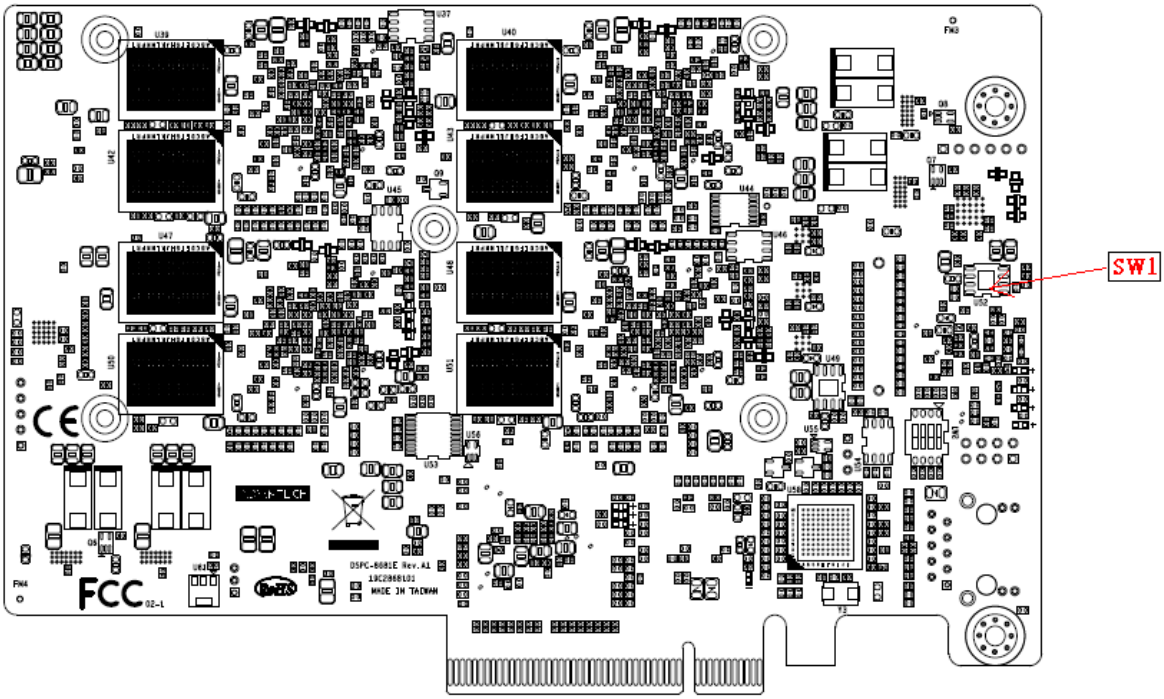

Figure29: The SW1 on DSPC-8681E PCIe Card

Below figure shows the sliding switch circuit and notes the bit number for use.

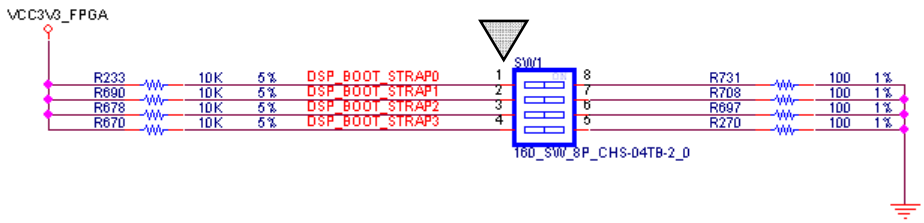

Figure30: The SW1 Schematic

The settings of Jumper and switch for DSPC-8681E are described as below table.

Configuration	Bit4	Bit3	Bit2	Bit1	Description
Endian Setting	-	-	-	ON	Big Endian (0)
	-	-	-	OFF	Little Endian (1)
Boot1 (000)	ON	ON	ON	-	None Boot (for development)
Boot2 (001)	ON	ON	OFF	-	I2C Boot from 0x51h SEEPROM
Boot3 (010)	ON	OFF	ON	-	PCIe Boot
TBD	Other states				TBD

Table14: The SW1 setting table

The data format configuration, setting is as below.

SW1.bit1 (Endian): 0- Big Endian / 1- Little Endian (default)

The Boot interface of the DSP, the setting is as below.

SW1.bit[4:2]: 000- None boot,
GPIO [13:1] on the DSPs: 0x0 0000 0000 0000b,
This mode is for the purpose of the development.

SW1.bit[4:2]: 001- I2C boot,
GPIO[13:1] on the DSPs: 0x0 0100 0000 0101b,
booting DSP from 0x51h of EEPROM and branch to the PCIE bus for the second boot (default).

SW1.bit[4:2]: 010- PCIE Boot,
GPIO[13:1] on the DSPs: 0x 0 0001 1000 0000 0100b,
booting DSP from PCIE interface.

SW1.bit[4:2]: others- reserved for future use.

The default setting of the switch (SW1) on DSPC-8681E is 0x0011b (bit[4:1]: ON, ON, OFF, OFF) for little endian data format and EEPROM boot from 0x51h.

5. Mechanical Drawing

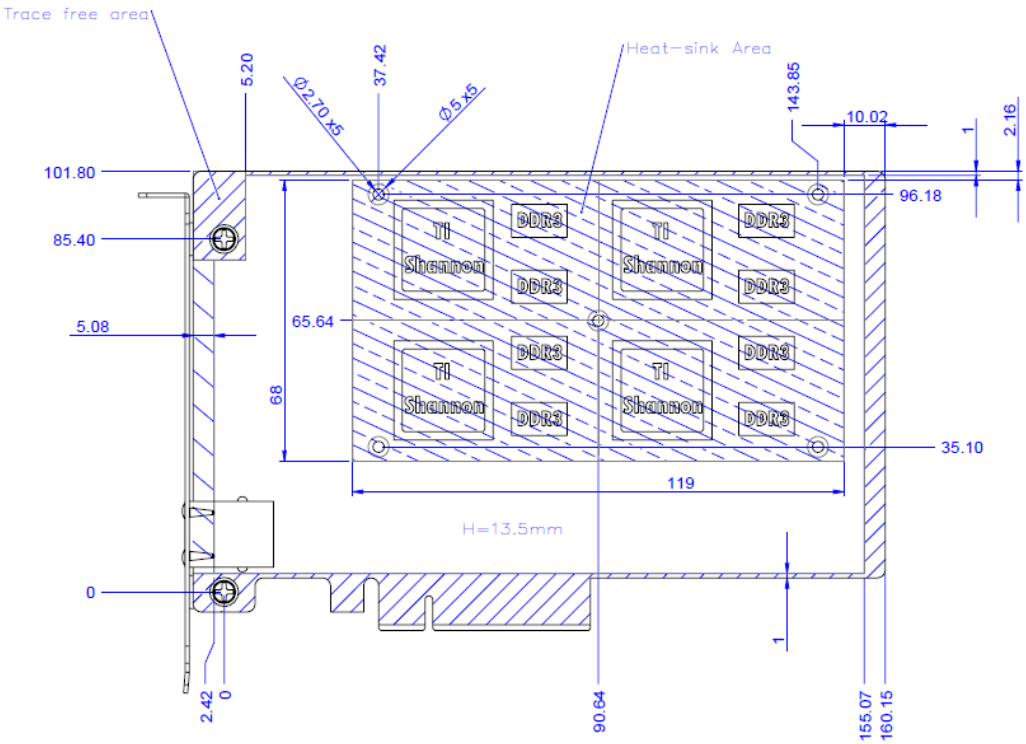

Figure31: DSPC-8681E TOP side

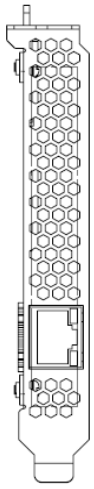

Figure32: DSPC-8681E Front Side

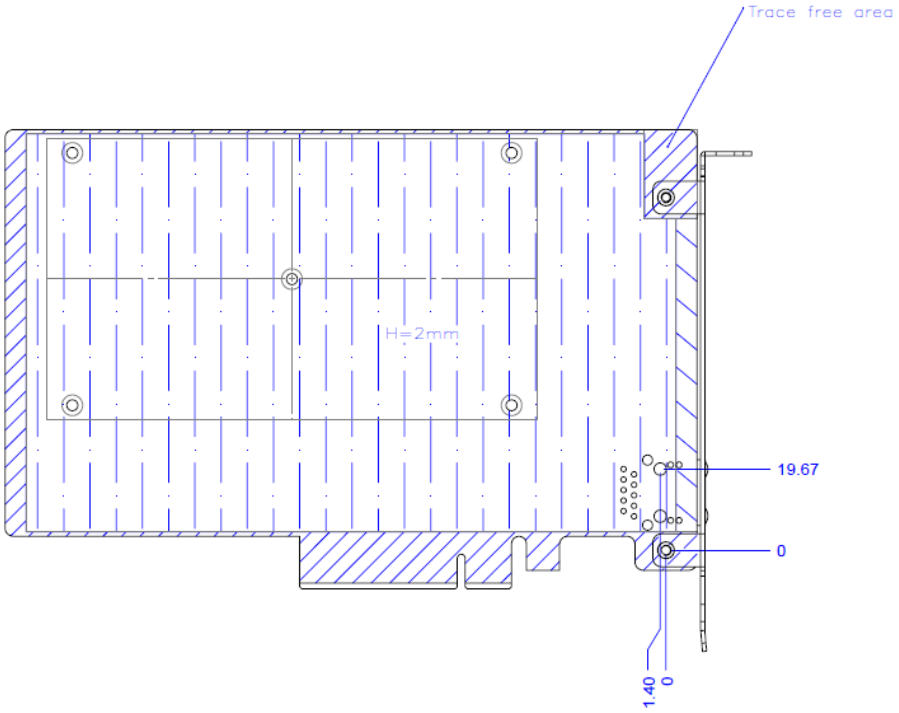

Figure 33: DSPC-8861E Bottom Side