Software Assisted Error recovery

After link initialization, the typical sequence is for the DSP software to check the *port_ok* bit in the SP(n)_ERR_STAT register before attempting to send packets. Without the *port_ok* bit being set, the two link partners are not initialized and will not be able to communicate at all. Additionally, before sending packets it is recommended to check for error conditions and clear any error status bits in the SP(n)_ERR_STAT and SP(n)_ERR_DET registers. Most of these error indication bits are simply writable to clear as described in their corresponding bit definitions. In some cases after reset, it has been observed that a given link partner may experience temporary bit errors resulting in OUTPUT ERROR-STOPPED and/or INPUT ERROR-STOPPED conditions. In these cases, hardware may or may not recover from this condition depending on the states involved, severity and location of the bit errors in the transmitted stream. Software can be used to immediately recover from the input and output error stopped states. It is recommended to add the following step after initialization and before trying to send any packets. This step can be added regardless of whether the device is currently in the output or input error-stopped states.

> Software writes a value of 0x2003F044 into the PLM Port n Control Symbol Transmit 1 register (RIO_PLM_SP(n)_LONG_CS_TX1)

This software initiated sequence immediately recovers both ends of the link from both input and output error-stopped conditions. Writing a value of 0x2003F044 into the Port n Control Symbol Transmit register causes a PNA and Link Request to be sent in the Stype 0 and 1 fields of control symbol to the link partner. The PNA causes the link partner to issue a link request to the DSP, and the link request causes the link partner to issue link response. The DSP receiving the link request issues a link response. The following figure illustrates the worst case situation where both device A and B are both in input and output error-stopped state. Note that it is really only required to issue the Port n Control Symbol generation for one end of the link.

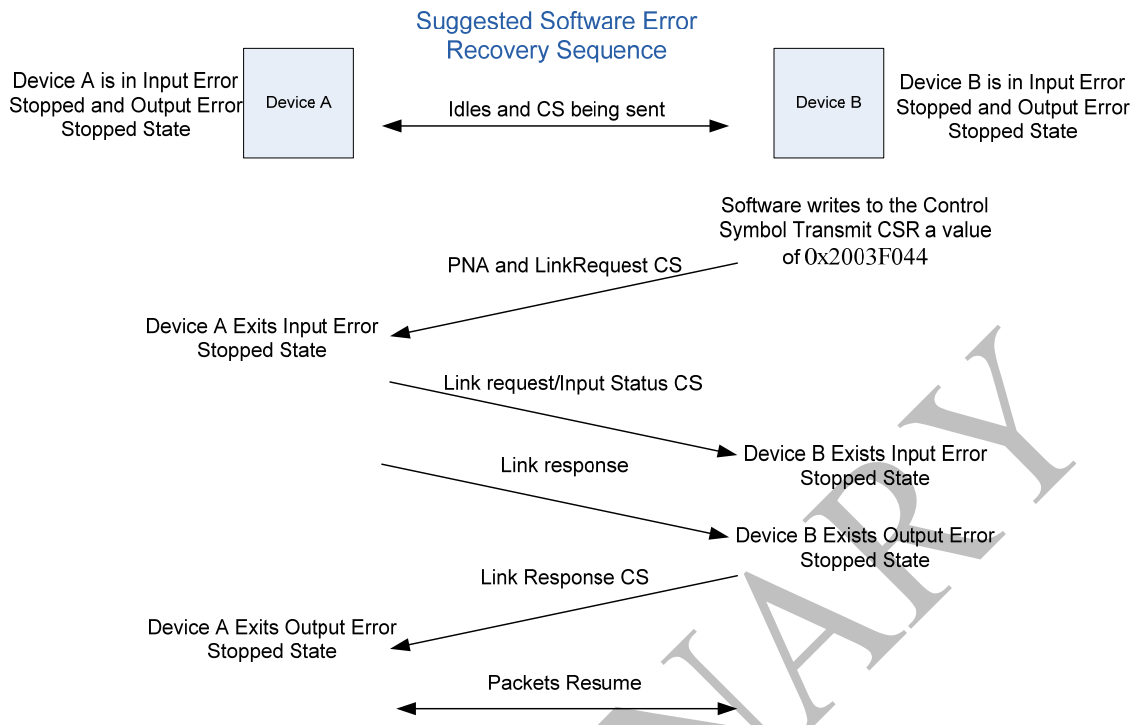

Figure 1: Error Recovery Sequence Diagram

The above sequence causes both devices to exit all input and output error stopped states. However, it does not align ACKIDs, which need to be synchronized before data or maintenance packets are sent between the link partners. If both link partners are coming out of reset, then the ACKIDs will already be aligned and no additional steps are needed. If not, then additional steps must be immediately taken to align ACKIDs. TI's DSP supports the software error recovery registers which make this process fairly straight forward. The following steps can be used to align the ACKIDs if both link partners support these registers.

1. After writing the RIO_PLM_SP(n)_LONG_CS_TX1 register = 0x2003F044 to exit the error states…

2. Each device's SP(n)_LM_RESP register will contain the link response data from step number 1. This data indicates the attached link partner's expected inbound ACKID value.

3. The DSP software can read the SP(n)_LM_RESP register and copy the expected partner's inbound ACKID to its own outbound and outstanding ACKID values in the local SP(n)_ACKID_STAT register.

4. The DSP can then send a maintenance packet to the link partner's SP(n)_ACKID_STAT register to program the ACKIDs to match expected values of the

DSP. When the maintenance packet is sent, it will overwrite all the fields of this register, so the value written should be: outstanding = outbound = DSP's expected inbound ACKID value, and the inbound = 1 + ACKID from step 3.

5. ACKIDs are now aligned and data packets can be exchanged normally.