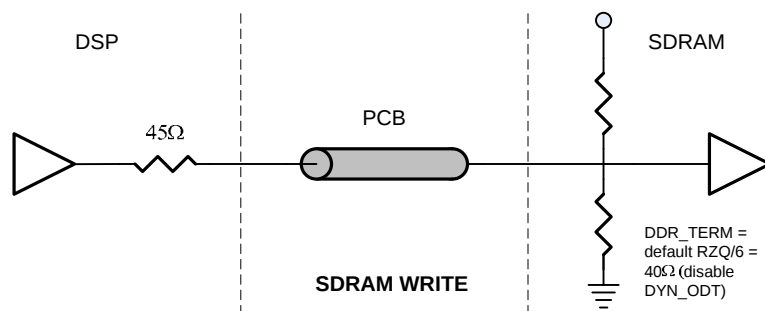


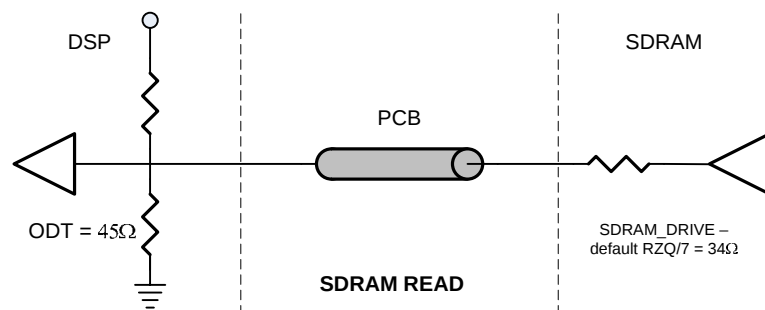
The routing guidance below augments the instructions contained in the *DDR3 Design Requirements for Keystone Devices* document (SPRABI1A). Any conflicts between the two documents need to be resolved.

There are many memory topologies possible and a listing of the supported topologies are listed in Section 2.6 of the *DDR3 Design Requirements for Keystone Devices* document (SPRABI1A). In general, the DDR3 interface has been verified to operate up to 1333MT/s with up to 9 loads on the fly-by nets (address, control, command and clock). Validation has focused on single-rank memory implementations with only a single load on the data group signals (data, data mask and data strobe). Topologies with fewer loads should all operate at this level of performance.

All data group signals are point-to-point in the validated topologies. They are driven by the Keystone device on writes and driven by the SDRAM memories during reads. There are no external resistors needed on these routes. The receivers in both cases (SDRAMs on writes and Keystone device on reads) will assert On-Die Terminations (ODT) at the appropriate times. The following diagrams depict the impedances seen on these nets during write and read cycles.



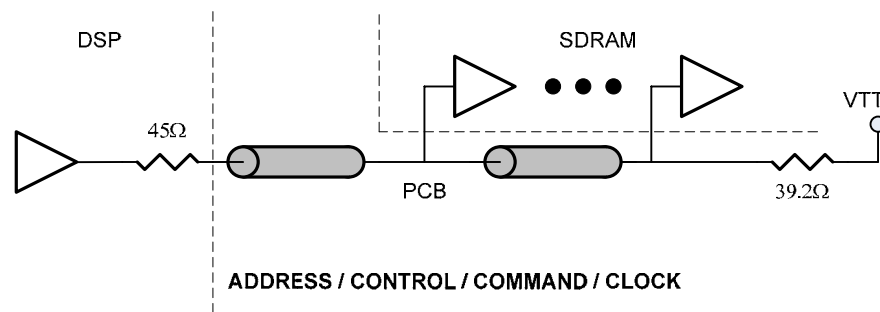
During writes, the output impedance of the Keystone device is approximately 45 ohms. We recommend that the SDRAM be implemented with a 240 RZQ resistor and that it be configured to present an ODT at RZQ/6 for an effective termination of 40 ohms.



During reads, we recommend that the SDRAM be configured for an effective drive impedance of $RZQ/7$ or 34 ohms (assuming the RZQ resistor is 240 ohms). The ODT within the Keystone device will have an effective Thevenin impedance of 45 ohms.

Each byte-lane needs to be length-matched to the length of its differential data strobe pair. Byte lanes do not have to be length matched to one another.

The fly-by signals include the address, control, command and clock routing groups. These must all travel along the same general path to be properly routed. The differential clock signals are routed first. Then the address, control and command groups are routed to match the clock length. The lengths for all of these groups must be matched from the Keystone device to each of the SDRAM memories. Additionally, the stub lengths at the SDRAMs must also be controlled. Terminations for the fly-by nets will be after the last SDRAM. The address, control and command groups will be terminated through a 39.3 ohm resistor to VTT. The clock pairs will be terminated through 39.3 ohm resistors to a common node connected to a capacitor that is then connected to VDDQ. The Keystone device will present a 45 ohm output impedance when driving these signals. This is shown in the following diagram.



There is a second set of clock and control outputs to support a second rank of memory. These are DDRCLKOUT[P/N]1, DDRODT1, DDRCKE1 and DDRCE1. These cannot be used with the single rank topology discussed above. Specifically, since the fly-by nets must all be length-matched to the clock to each SDRAM, you cannot use both clock pairs and achieve proper fly-by routing.

PCB trace impedance is related to all of the routing discussion above. There is no single, optimum answer to this question. Layout topologies and routing strategies differ from board to board. We recommend that you execute signal integrity simulations to optimize your design implementation. We can offer routing examples that are known to work and you can then customize them for your needs. PCB materials, trace widths and dielectric thicknesses need to be controlled to achieve the desired operating performance.

The EVMs have single-ended routes configured for 50 ohms and the differential routes configured for 100 ohms. The stack-up and trace widths are optimized to provide these

impedances. Signal integrity simulations and timing analysis has been completed on the EVM board layouts.

The JEDEC UDIMM specification provides guidance for UDIMM manufacturers. These recommendations are equally applicable to customer layouts. They recommend 40 ohm routes on the fly-by nets between the controller and the first SDRAM and then 60 ohm routes between the SDRAMs and to the terminations. However, footnotes under Table 39 state that lightly loaded UDIMMs (single rank implementations like the topologies we expect customers to implement with KeyStone devices) should target 49 ohms rather than 60 ohms. The JEDEC UDIMM specification does not explicitly state an impedance for the data group signals but implies that the default impedance is 60 ohms. Differential routes can be constructed from these same single-ended track structures resulting in differential impedances under 100 ohms.