Electrical Compliance Test Specification
SuperSpeed Universal Serial Bus

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Revision: 0.9

Scope of this Revision

The 0.7 revision of the specification describes the testing to be applied to hardware based on the Universal Serial Bus 3.0 Specification, revision 1.0.

Revision History

Revision	Issue Date	Comments
0.5	02/25/2009	For review only.
0.7	06/03/2009	For review only.
.9	09/10/2009	Complete draft of test algorithms.
.9RC1	9/15/2009	Final .9 draft release candidate after workgroup reviews.

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1 Introduction

This document provides the compliance criteria and test descriptions for SuperSpeed USB devices, hubs and host controllers that conform to the Universal Serial Bus 3.0 Specification, rev 1.0. It is relevant for anyone building SuperSpeed USB hardware. These criteria address the electrical requirements for a SuperSpeed physical layer design. Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

Each test assertion is formatted as follows:

Assertion #	Assertion Description	Test #	Comments

Assertion#: Unique identifier for each spec requirement. The identifier is in the form USB3_SPEC_SECTION_NUMBER#X where USB_SPEC_SECTION_NUMBER is the applicable section number from the physical layer chapter of the USB 3.0 spec (chapter 6) and X is a unique integer for a requirement in that section.

Assertion Description: Specific requirement from the specification

Test #: A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

N/A This item is not explicitly tested in a USB SuperSpeed test description. Items can be labeled N/A for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the USB SuperSpeed compliance test.

TD.1.X This item is covered by the test described in test description 1.X in this specification.

TBD A test description is not yet written for this assertion. The comments field provides more details on such items.

Comments: Provides additional information on requirements that are marked TBD.

1.1 Related Documents

[1] Universal Serial Bus 3.0 Specification, revision 1.0, November 12, 2008

[2] USB 3.0 Super Speed Electrical Compliance Methodology, revision 0.5.

[3] Universal Serial Bus Specification, Revision 2.0, April 27, 2000.

[4] *USB-IF USB 2.0 Electrical Test Specification*, Version 1.03, January 2005.

1.2 USB 2.0 Compliance

USB 2,0 testing is required for USB 3.0 devices and is covered by a separate compliance testing program. Refer to [3] and [4] for details.

2 Test Descriptions

TD.1.1 Low Frequency Periodic Signaling TX Test.

This test verifies that the low frequency periodic signal transmitter meets the timing requirements when measured at the compliance test port.

Overview of Test Steps

1. The test performs the following steps.Connect the DUT to a simple breakout test fixture. Disconnect bus power if the DUT is a bus powered device.
2. Power on the device under test (connect bus powered if DUT is a bus powered device) and let it pass through the Rx.Detect state to the Polling.LFPS substate.
3. Trigger on the initial LFPS burst sent by the DUT and capture the first five bursts for analysis..
4. Measure the following LFPS parameters and compare against the USB 3.0 specification requirements: tburst, trepeat, tperiod, tRiseFall2080, Duty cycle, $V_{CM-AC-LFPS}$, and $V_{TX-DIFF-PP-LFPS}$. For these measurements the start of an LFPS burst is defined as starting when the absolute value of the differential voltage has exceeded 100 mV and the end of an LFPS burst is defined as when the absolute value of the differential voltage has been below 100 mV for 50 ns. tperiod, tRiseFall2080, Duty cycle, $V_{CM-AC-LFPS,}$ and $V_{TX-DIFF-PP-LFPS}$ are only measured during the period from 100 nanoseconds after the burst start to 100 nanoseconds before the burst stop.

TD.1.2 Low Frequency Periodic Signaling RX Test.

This test verifies that the DUT low frequency periodic signal receiver recognizes LFPS signaling with voltage swings and duty cycles that are at the limits of what the specification allows. The link test specification includes test that vary additional LFPS parameters to test the LFPS receiver.

Overview of Test Steps

The test performs the following steps.

1. Connect the DUT to a simple breakout test fixture. Disconnect bus power if the DUT is a bus powered device.
2. Power on the device under test (connect bus powered if DUT is a bus powered device) and let it pass through the Rx.Detect state to the Polling.LFPS substate.
3. Trigger on the initial LFPS burst sent by the DUT and send LFPS signals to the DUT with the following parameters:
    a. tPeriod 50 ns.
    b. $V_{TX-DIFF-PP-LFPS}$ 800 mV.
    c. Duty Cycle 50%
4. The test passes if the device recognizes the LFPS and starts sending the TXEQ sequence.
5. The test is repeated with the following parameters:
    a. tPeriod 50 ns, $V_{TX-DIFF-PP-LFPS}$ 1200 mV, Duty Cycle 50%.
    b. tPeriod 50 ns, $V_{TX-DIFF-PP-LFPS}$ 1000 mV, Duty Cycle 40%.
    c. tPeriod 50 ns, $V_{TX-DIFF-PP-LFPS}$ 1000 mV, Duty Cycle 60%.

TD.1.3 Transmitted Eye Test

This test verifies that the transmitter meets the eye width, deterministic jitter and random jitter requirements when measured at the compliance test port with -3.5dB of transmitter equalization and after processing with the reference CTLE and JTF..

In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active as follows for the various DUT types.

Device upstream. No crosstalk.

Hub upstream. Hub upstream port under test transmits in high speed USB 2.0 test packet mode.

Host/Hub downstream. Host/Hub downstream port under test transmits in high speed USB 2.0 test packet mode.

For Hub and Host downstream ports the test is repeated with a device connected and get descriptors run in loopback with a software tool.

No transmitter testing is done with multiple downstream ports active on hosts/hubs.

Overview of Test Steps

The test runs in the Polling.Compliance substate, and performs the following steps.

1. Connect the DUT to a simple break-out test fixture without VBUS supplied.
2. Power on the device under test and apply VBUS if the DUT is not a host, let it pass through the Rx.Detect state to the Compliance state. SSC shall be enabled.
3. Transmit the CP0 compliance pattern on the SuperSpeed USB port under test and capture the transmitted waveform on a high speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps. The data may be acquired over a maximum of 4 captures on the scope.

Note - It is acceptable to capture slightly less than 1 million unit intervals due to SSC.

TBD – Analysis will be done to sweep 250k UI window through CP0 captures and look at variation. If the variation is significant the requirement may be changed to 1 million consecutive UI in the next specification revision.

4. Send a PING.LFPS to the RX port of the device under test to cause the compliance pattern to transition to CP1. A single PING.LFPS burst is sent with the following parameters:
    a. 100 nanosecond duration.
    b. 20 Mhz frequency (2 periods).
5. Transmit the CP1 compliance pattern on the SuperSpeed USB port under test and capture the transmitted waveformon a high speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps. The data may be acquired over a maximum of 4 captures on the scope.

Note - It is acceptable to capture slightly less than 1 million unit intervals due to SSC.

6. The compliance channel is embedded to the measured CP0 and CP1 data.
    a. Host test: 3 meter cable + 5” device PCB trace.
    b. Devcie test: 3 meter cable + 11” host PCB trace.

Note: Reference S parameter files for the embedded channels will be provided in the next revision of this specification.

7. Compute the data eye using CP0 and compare it against the normative transmitter specifications contained in table 6-12 of the USB 3.0 specification.
8. Compute Rj using the CP1 data and compare it against the normative transmitter specifications contained in table 6-12 of the USB 3.0 specification.
9. Compute the total jitter at 10^{-12} BER using the CP0 data to compute a measured Tj and the Rj value from CP1 with the dual dirac method and compare it against the normative transmitter specification contained in table 6-12 of the USB 3.0 specification.

Note: Extrapolate Tj E-12 based on Tj measured with CP0 and CP1 Rj only.

TD.1.4 Transmitted SSC Profile Test

This test verifies that the transmitter meets SSC profile requirements when measured at the compliance test port with -3.5dB of transmitter equalization and after processing with the JTF.

In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active as follows for the various DUT types.

Device upstream. No crosstalk.

Hub upstream. Hub upstream port under test transmits in high speed USB 2.0 test packet mode.

Host/Hub downstream. Host/Hub downstream port under test transmits in high speed USB 2.0 test packet mode.

Note: A PCI Express host adaptor is tested in a system that provides a 100 Mhz PCI Express reference clock with a valid SSC profile.

For Hub and Host downstream ports the test is repeated with a device connected and get descriptors run in loopback with a software tool.

No transmitter testing is done with multiple downstream ports active on hosts/hubs.

Overview of Test Steps

The test runs in the Polling.Compliance substate, and performs the following steps.

1. Connect the DUT to a simple break-out test fixture.
2. Power on the device under test, let it pass through the Rx.Detect state to the Polling.Compliance substate. SSC shall be enabled.
3. Send a PING.LFPS to the RX port of the device under test to cause the compliance pattern to transition to CP1.
4. Transmit the CP1 compliance pattern on the SuperSpeed USB port under test and capture the transmitted waveformon a high speed oscilloscope over a minimum of 1,000,000 unit intervals (200 μsec) at a sample rate of no more than 25 ps. The data may be acquired over a maximum of 4 captures on the scope.

Note - It is acceptable to capture slightly less than 1 million unit intervals due to SSC.

5. The CP1 waveform is used to analyze that the slew rate (derivative) of the period jitter after applying the CDR filter does not exceed $T_{CDR\_SLEW\_MAX}$.
6. The CP1 waveform is used to test that $t_{SSC\text{-}MOD\text{-}RATE}$ and $t_{SSC\text{-}FREQ\text{-}DEVIATION}$ meet the USB 3.0 specification. $t_{SSC\text{-}FREQ\text{-}DEVIATION}$ can vary between +300/-3700 and +300/-5300 PPM.

TD.1.5 Receiver Jitter Tolerance Test

TBD – Add informative test cases with No SSC and center spread SSC.

This test verifies that the receiver properly functions in the presence of deterministic and random jitter at multiple frequencies. The jitter characteristics are defined by the USB 3.0 specification. In order to reduce test time, the receiver is tested to a bit error ratio (BER) of 10^{-10}..In order to comprehend noise effects, such as crosstalk, it is up to the component manufacturer to make sure that any other links are active as follows.

Device upstream. No USB 2.0 crosstalk.

Hub upstream. Hub upstream port transmits in high speed USB 2.0 test packet mode.

Host/Hub downstream. Host/Hub downstream port transmits in high speed USB 2.0 test packet mode.

For Hub and Host downstream ports the test is repeated with a device connected and get descriptors run in loopback with a software tool.

No receiver testing is done with multiple downstream ports active on hosts/hubs.

The receiver test is performed with asynchronous SSC clocks in the test system and the device under test. The test system SSC shall be triangular at the maximum specified SSC frequency (33 Khz) and downspread 5000 ppm. The test system SSC shall meet the specification limits on slew rate. Note: When the DUT is in loopback for this test it shall not exit loopback unless it receives a warm reset or an LFPS Exit Handshake.

Overview of Test Steps

The test runs in the Polling.Loopback substate, and performs the following steps.

1. Connect the DUT to the compliance channel.
2. Connect the compliance channel to the signal source with the signal source set to 3.0 dB de-emphasis nominal..

Calibrate Rj (2.42 +/- 10% ps RMS/30.8 +/- 10% ps peak to peak at a BER of 10^{-10}) with clock pattern (CP1). Calibrate at the end of the channel applying the CTLE and JTF. SSC is off for this step.

Calibrate Sj (40.0 ps +0/-10% at 50 MHz) with CP0. Calibrate at the end of the channel applying only CTLE. SSC is off for this step.

Measure Tj at the end of the channel with CP0 applying JTF and CTLE. Tj must be .66 UI at a BER of 10^{-12} nominal +2.6/-10% allowed variation. SSC is on for this step. The test equipment source may adjust the de-emphasis level if necessary to meet the Tj requirement.

Measure eye height at a BER of 10^{-6} at the end of the channel with all jitter sources and SSC on applying JTF and CTLE. Adjust amplitude to provide 100 mV +10/-0% of eye height.

3. Power on the device, let it pass through the Rx.Detect state to the Polling state and force entry to the Polling.Loopback substate by transmitting the TS2 sequence with bit 2 of symbol 5 asserted.

Note: If the DUT loses bit lock at any point from step 3 onward it fails the test.

4. Transmit the BDAT sequence from the signal source for a total of $3x10^9$ symbols ($3x10^{10}$ bits). A single SKP ordered set is inserted in the sequence every 354 symbols.

5. The DUT fails if more than one error is encountered. .

   Note: The channel to the test equipment receiver is kept as short and clean as possible.

6. Repeat steps 2-6 with 40.0 ps of periodic (sinusoidal) at a 33 MHz frequency with -3dB of equalization.
7. Repeat steps 2-6 with 40.0 ps of periodic (sinusoidal) at a 20 MHz frequency with -3dB of equalization.
8. Repeat steps 2-6 with 40.0 ps of periodic (sinusoidal) at a 10 MHz frequency with -3dB of equalization.
9. Repeat steps 2-6 with 40.0 ps of periodic (sinusoidal) at a 4.9 MHz frequency with -3dB of equalization.
10. Repeat steps 2-6 with 100 ps of periodic (sinusoidal) at a 2 MHz frequency with -3dB of equalization.
11. Repeat steps 2-6 with 200 ps of periodic (sinusoidal) at a 1 MHz frequency -3dB of equalization.
12. Repeat steps 2-6 with 400 ps of periodic (sinusoidal) at a 500 KHz frequency -3dB of equalization.