KeyStone Training

Antenna Interface 2 (AIF2)

Agenda

- Evolution from AIF1 to AIF2
- AIF2 Timer (AT)
- Physical Layer Modules (SD, RM, TM, RT)
- Protocol Layer Modules (PD, PE, DB)
- DMA Modules (AD, PKTDMA)
- Error and Exception Handling (EE)

Evolution from AIF1 to AIF2

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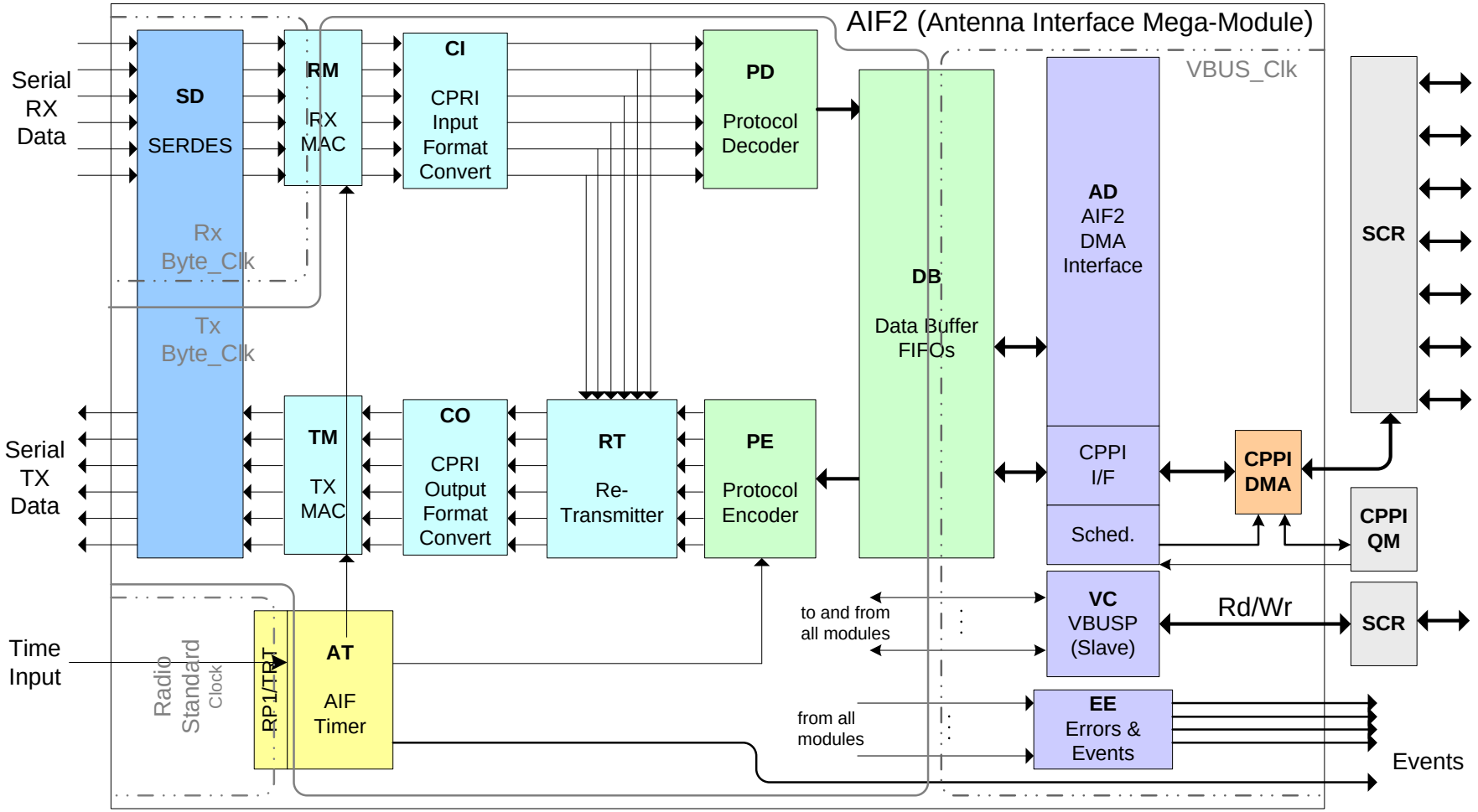
Evolution of AIF2 from AIF1

1. Clock Strategy: Dual-byte clock is used for physical layer and protocol layer modules.
2. 6 GHz SERDES bit-level scrambling supports 8x link speed.
3. AIF2 MMR reset function is supported.
4. Support multiple radio standards with more flexibility (WCDMA, LTE, WiMAX, TDS-CDMA, GSM/EDGE)
5. Full support of dual-bit map rule achieved for both OBSAI and CPRI.
6. Total of 128 channels are supported for both ingress and egress.
7. Multicore Navigator packet transfer and Direct IO for WCDMA AxC data DMA is supported.
8. Frame sync module is merged with AIF2 core (AIF2 Timer module).
9. Phy timer and Radio timer is separated (UL and DL Radix timer is supported).
10. Dynamic configuration is supported to add/delete AxC channel, AIF2 Link, and External AT events.

AIF2 Module Architecture

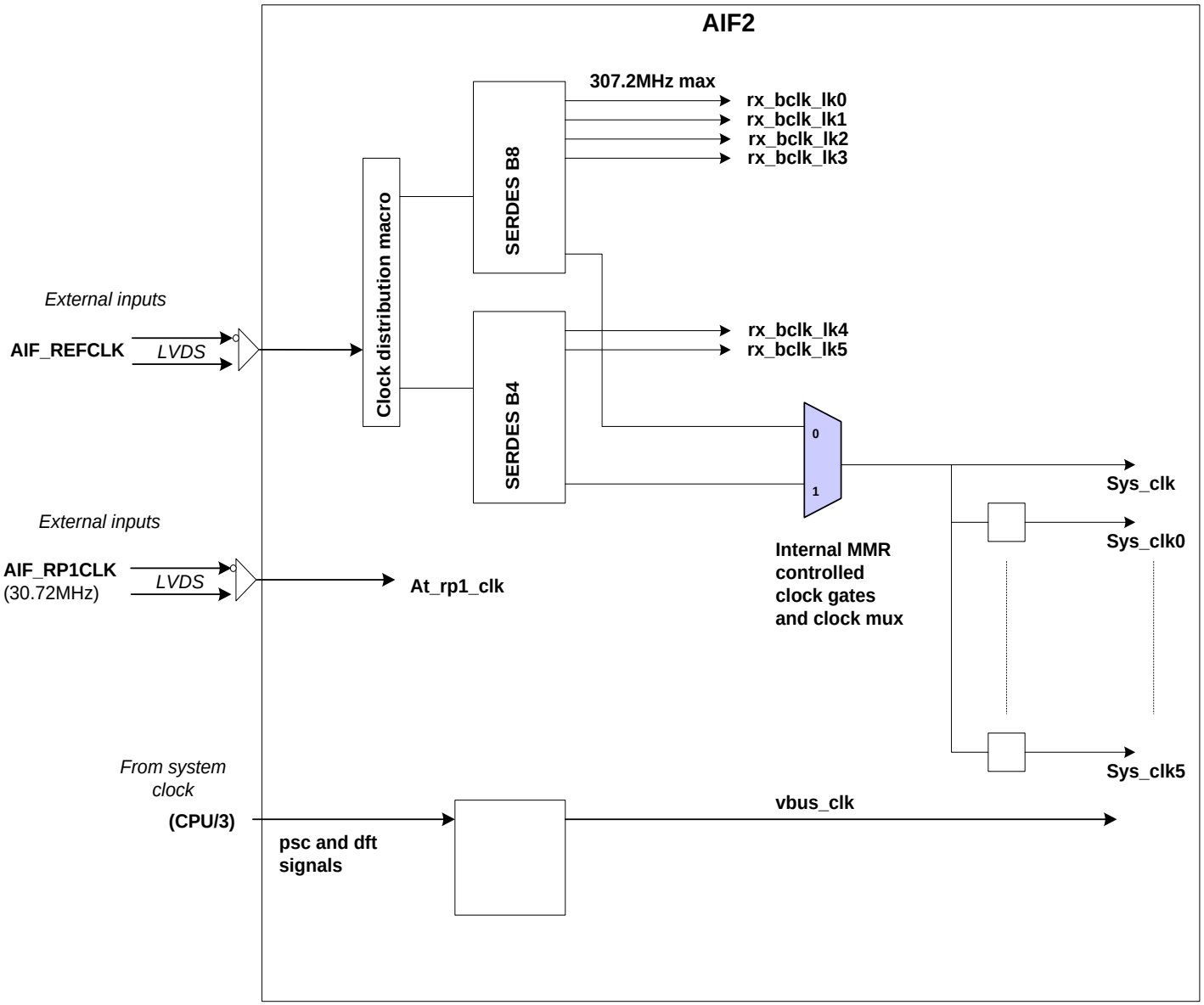


- PHY layer {SD, RM, CI, RT, CO, TM, AT}
- Protocol layer {PD, PE, DB}
- DMA layer {AD, CDMA}

AIF2 Clocking

Transmit dual-byte clock domain:

- Typically, 307.2MHz for OBSAI and 245.76 MHz for CPRI.
- Dual-byte clock is generated from the AIF_REFCLK.
- AIF_RP1CLK is used only for RP1 mode and the frequency is fixed to 30.72 MHz.
- Interface to the KeyStone system will be in the CPU clock/3 clock domain, which is called vbus_clk.



Dynamic Configuration

Types of changes are split into two basic categories:

- On-the-fly: Ping-pong configuration mechanism allows change to occur from one frame to the next without any “off” or error period of time.
- Normal Changes: An antenna carrier is torn down and then later rebuilt to accomplish a change. These changes require a “system down” period.

The major functionalities of AIF2 dynamic configuration are as follows:

- Link Add/Delete (add link without resetting AIF2 timer)
- AxC Add/Delete (add or delete AxC channel)
- GSM Base Band Hopping
- LTE (TDD) & WiMax (TDD) : Change UL/DL ratio (On the fly)
- AT Timing: System Event Add/Delete (On the fly), RadT re-synchronization

AIF2 SW Reset

- A single MMR contains a bit which is used as the software-controlled hardware reset of the AIF2.
- AIF2 CSL supports API called AIF2_reset() which activates a software reset process.
- The entire AIF2 hardware is reset when the software reset pin is activated.

The following circuitry is NOT reset during software reset:

1. Config VBUS
2. VBUSP Interface
3. Internal SCR circuits
4. vbus_clk to sys_clk re-timing bridge

AIF2 Timer (AT)

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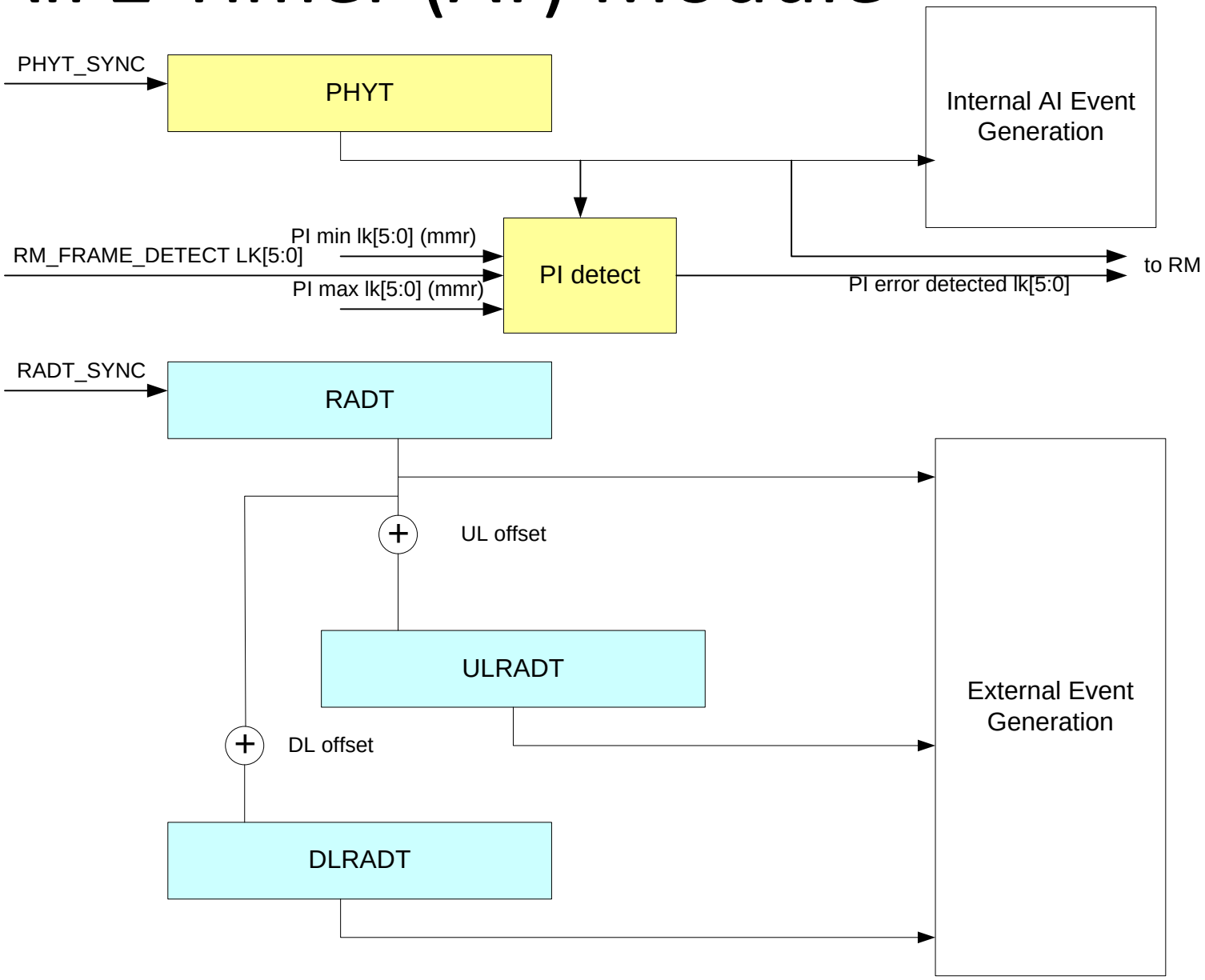
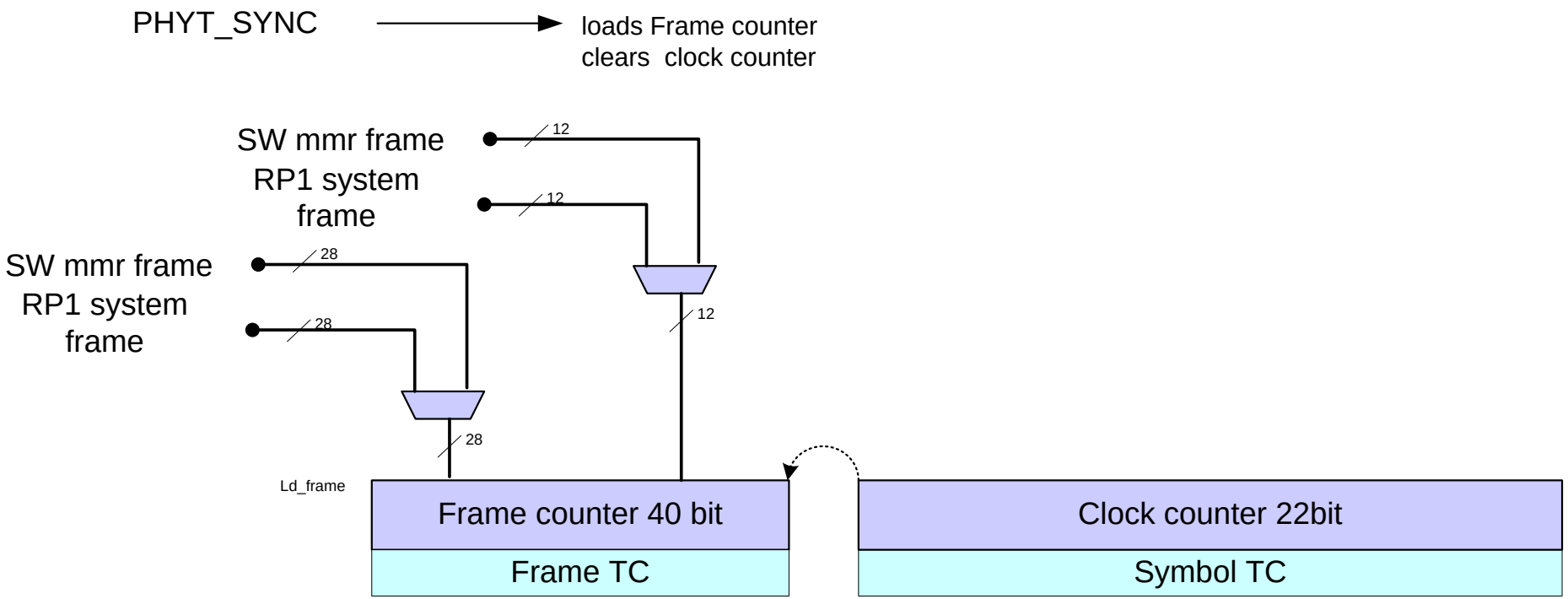
AIF2 Timer (AT) Module

Two timers in AT:

- Phy Timer (PHYT) has functionality similar to 64x+ RP3 timer.
- Rad Timer (RADT) supports various frame size for various radio standards.
- AT also supports separate UL and DL timers for application.
- UL and DL offset is configured by setting init value registers.



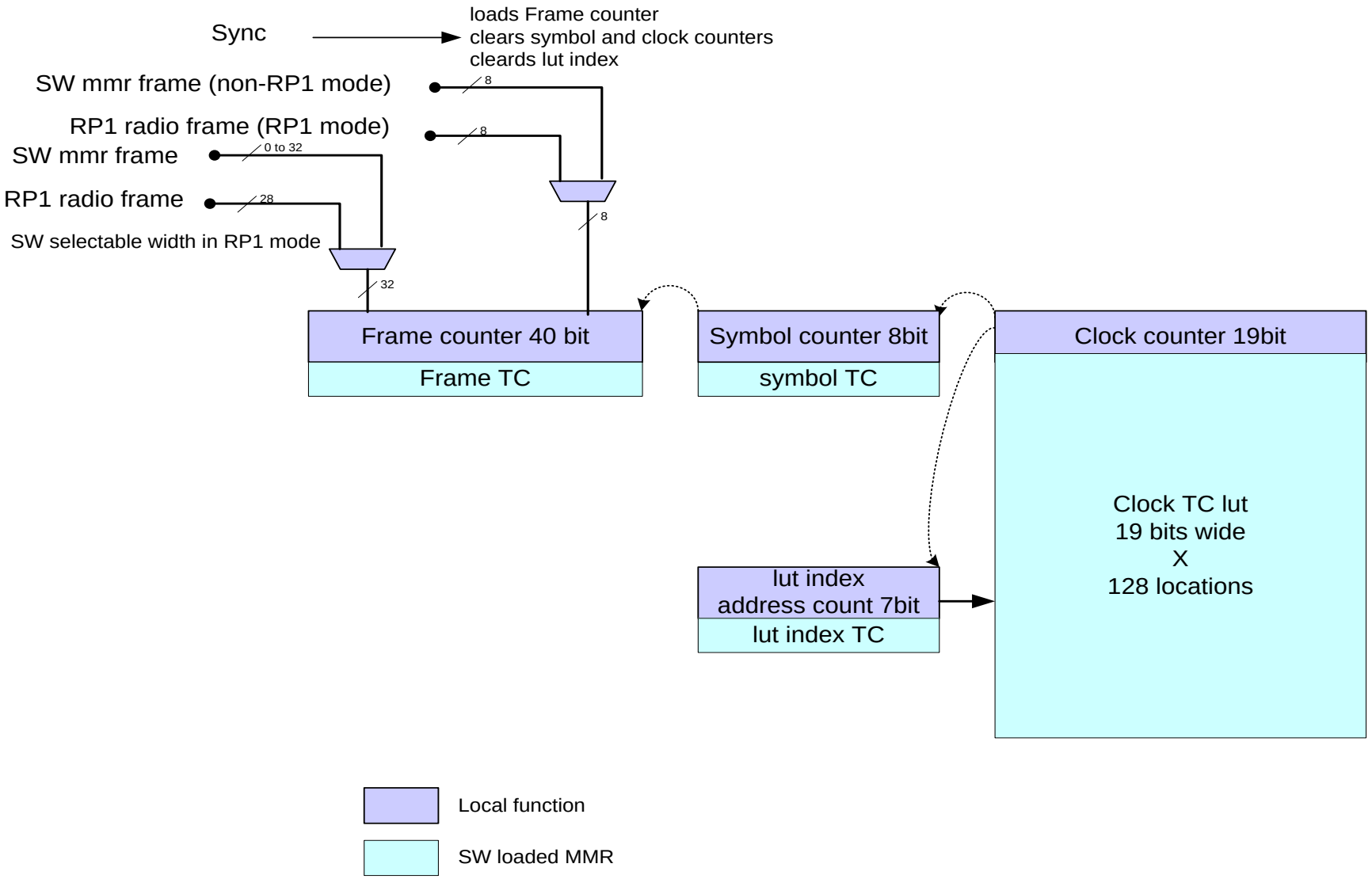
AT Phy Timer (PHYT)



Phy timer does not have a symbol and lut index address terminal counter.

Phy Frame size is 10 ms and clock counter TC for this will be 3071999 (OBSAI) and 2457599 (CPRI).

AT Radio Timer (RADT)

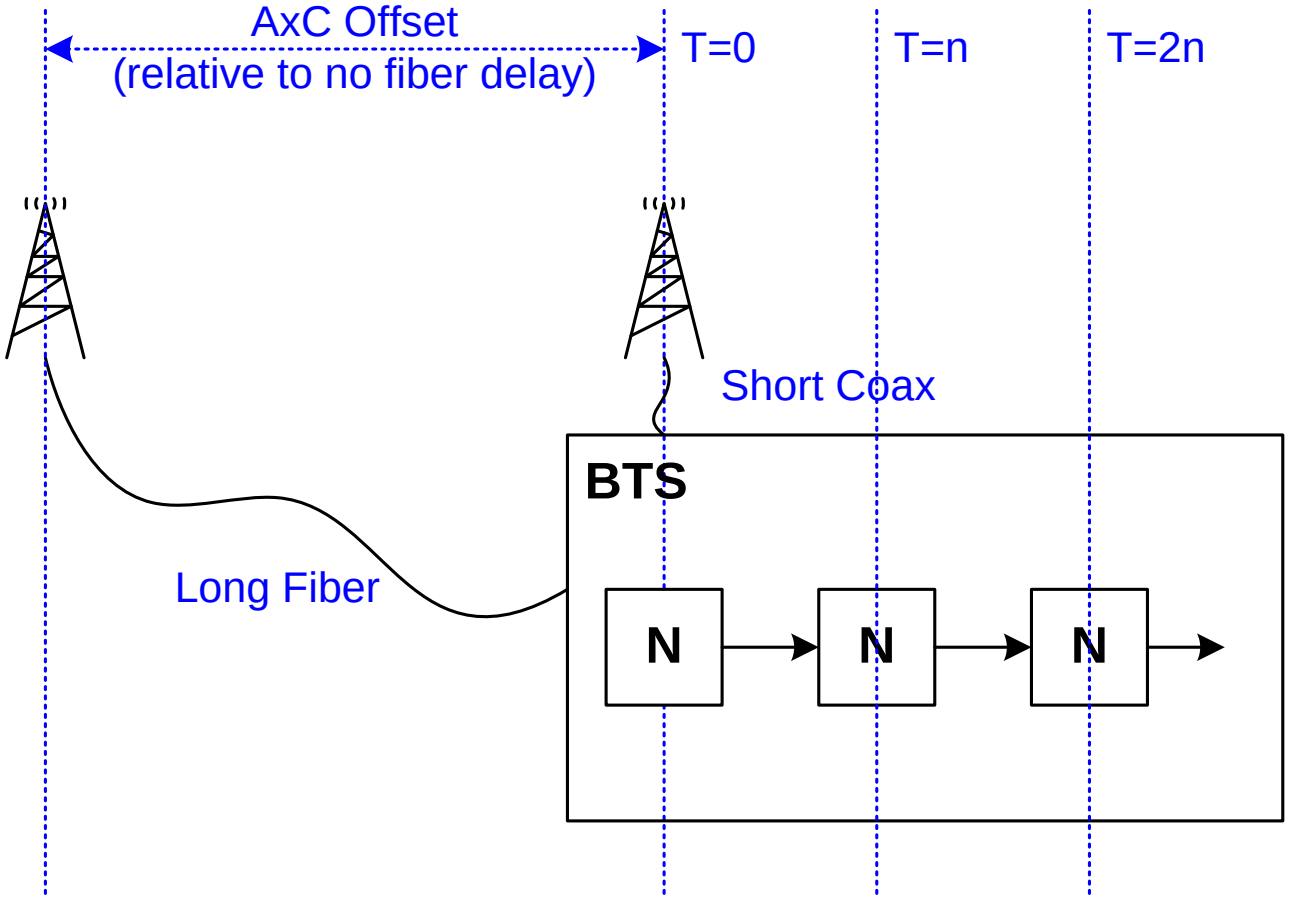


lut index address terminal counter is used for various size of symbols.

AxC Offset

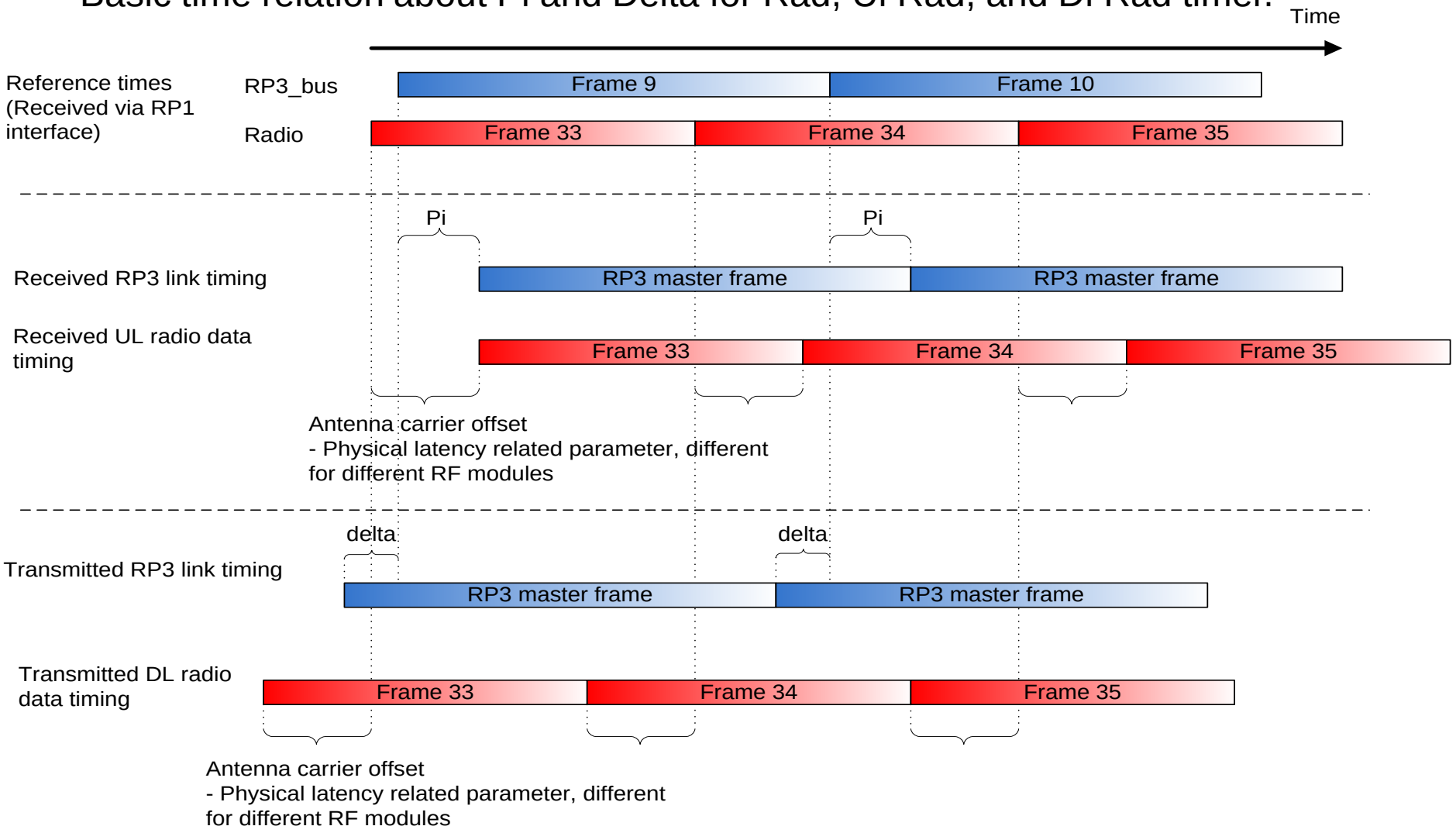
Antenna carrier offset is the relative delay from long fiber path when compared to the short coaxial delay from closer antenna.

The unit is dual-byte clock for OBSAI and number of samples for CPRI.



Pi & Delta Timing Example

Basic time relation about Pi and Delta for Rad, Ul Rad, and Dl Rad timer.



AT Event Generation

Eight external events, three special events, six DIO events, Phy level events

- AT supports eight external events for CorePac and application
- AT also supports six internal events for Direct IO
- Phy level events : Delta, PE1, PE2 events

Event strobe selection

- It is allowed to select event strobe timing like below
    1. Radt symbol or frame time
    2. Ul Radt symbol or frame time
    3. Dl Radt symbol or frame time

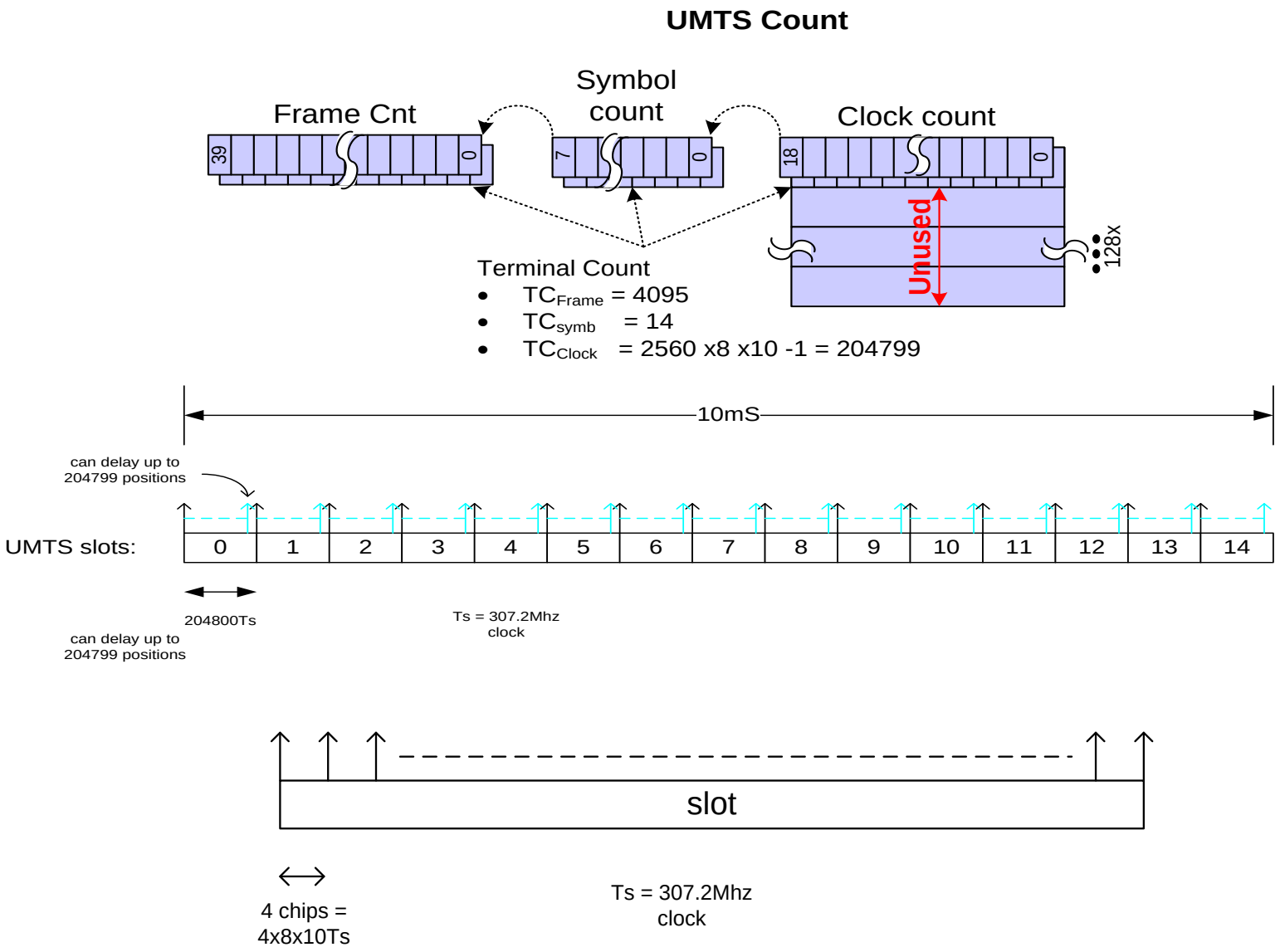
Modulo and offset

- Modulo represent the number of byte clock which shows when next trigger should be occurred
- offset is the initial time delay for each event (this is same to Faraday frame sync module offset delay)

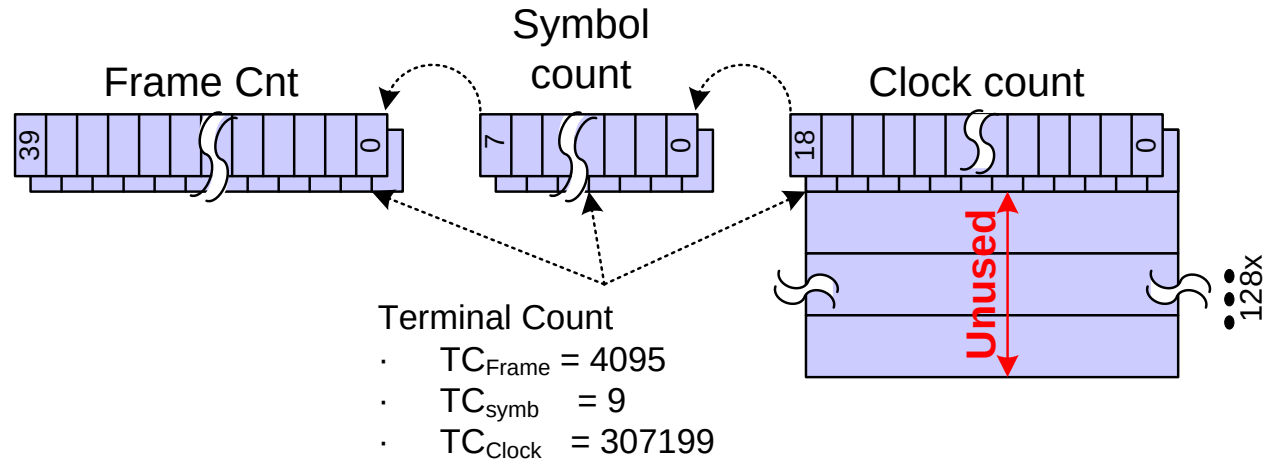
Timer field usage for different radio standards

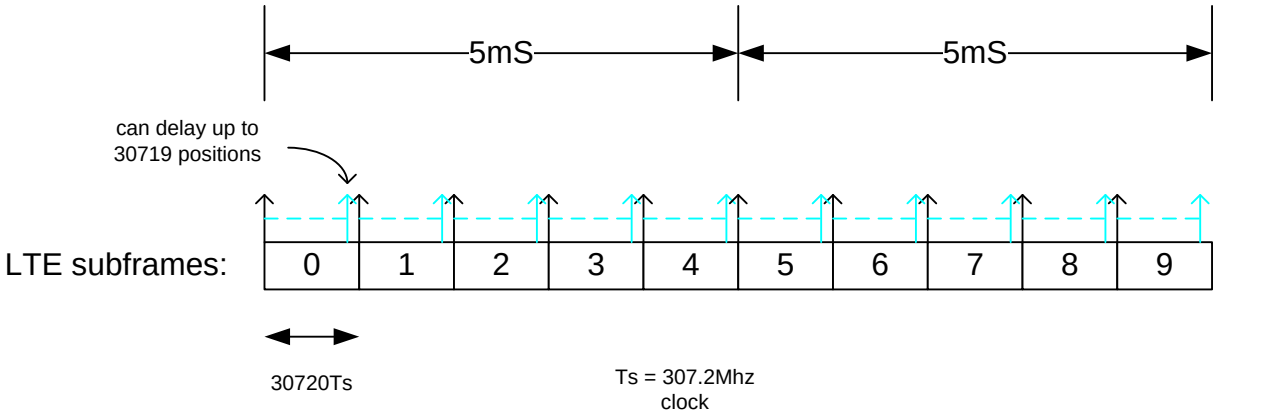
Radio Standard	Frame_Cnt	Symbol_Cnt	Clock_Count
WCDMA	10ms Frames	Time Slots	Clocks per Slot
LTE	10ms Frames	1ms Sub-Frames	Clocks per Sub-Frame
WiMax (TDD/FDD)	Frames	Symbol Count	Clocks per Symbol
TD-SCDMA (TDD)	Frames	Symbol Count	Clocks per Symbol
GSM	60ms	Time Slots per 60ms	Clocks per Time Slot

WCDMA Event Counter Example

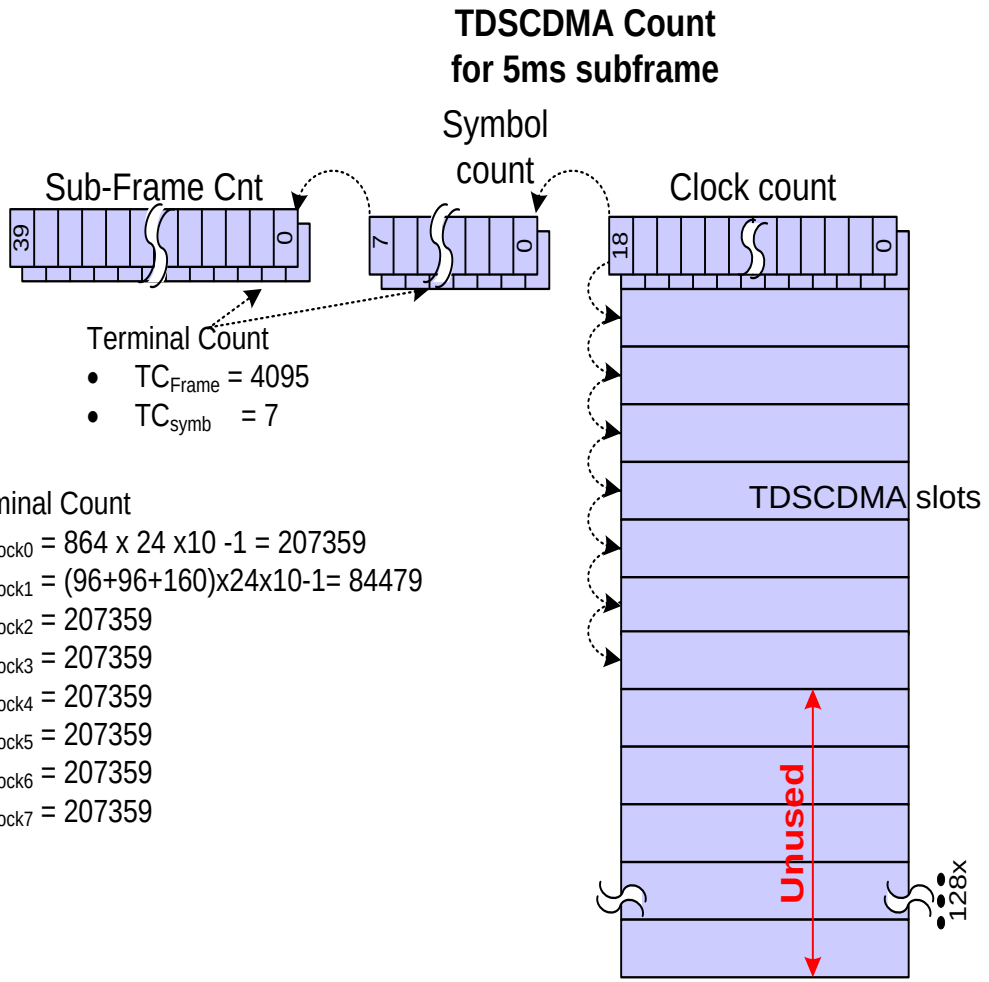


LTE Event Counter Example





TDS-CDMA Event Counter Example



Terminal Count

TC_{clock0} = 864 x 24 x10 -1 = 207359

TC_{clock1} = (96+96+160)x24x10-1= 84479

TC_{clock2} = 207359

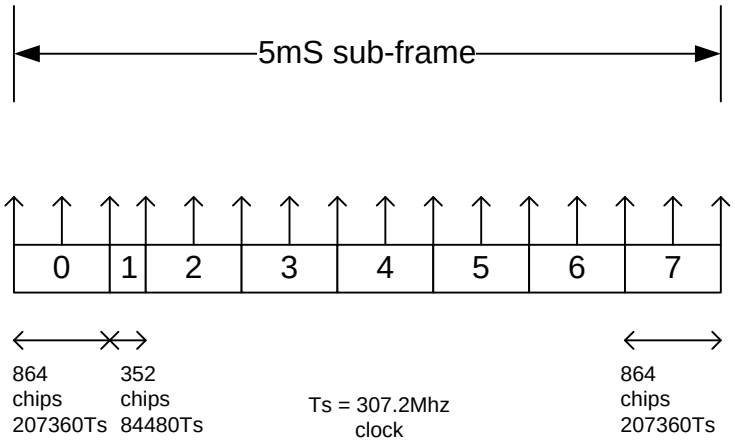
TC_{clock3} = 207359

TC_{clock4} = 207359

TC_{clock5} = 207359

TC_{clock6} = 207359

TC_{clock7} = 207359



TD-SCDMA mid symbol event can be created my modulo counter

Physical Layer Modules (SD, RM, TM, RT)

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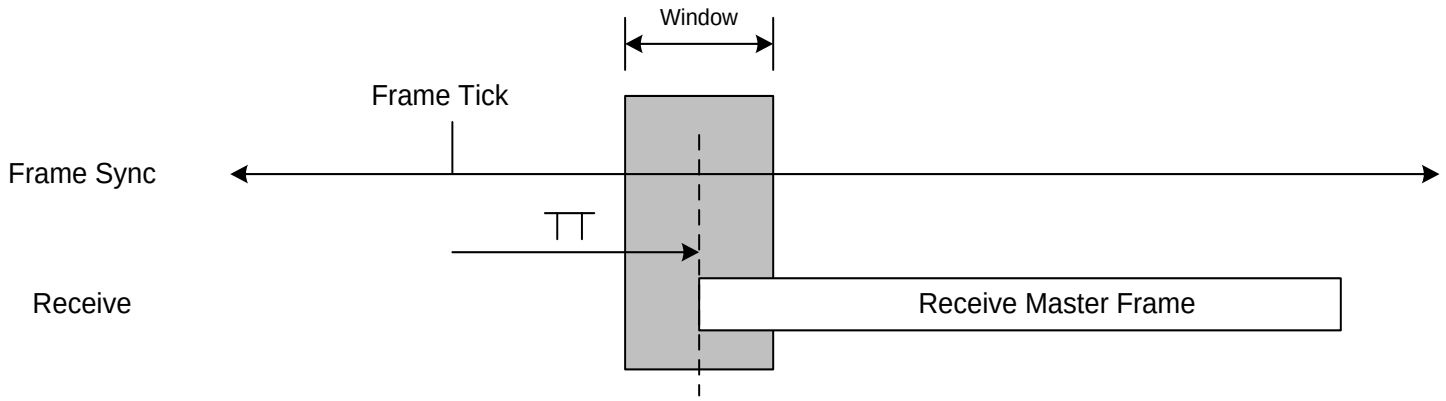
SERDES Module

- Two Macros (B8, B4)
  - B8 support link 0,1,2,3 and B4 support link 4, 5
  - Maximum line rate is 6.144 Gbps with data scrambling (8x speed)
  - Special PLL circuit to support 5x speed for CPRI
- Clock disable for each link
  - Clock disable configuration register is used to save power by closing gate off of the unused link.
- Digital Loopback Mode
  - Supports internal loopback for test and debug
  - Does not support bump pad loop back anymore
- Line Rates
  - 8x: Half rate - Two data samples taken per PLL output clock cycle
  - 4x, 5x: Quarter rate - One data sample taken per PLL output clock cycle
  - 2x: Eighth rate - One data sample taken every two PLL output clock cycles

RM(RX Mac) Module

- **Pi Measurement (RM)**



  - Receive Frame Synchronization provides a single pulse for the AT module that indicates the beginning of a master frame
  - Pi variable is used by the AT module to perform Pi measurement

- **Pi offset is controlled by AT**
  - Support Pi max, min register

TM (TX Mac) Module

- **TM FIFO**
  - The Transmit FIFO of Tx Mac link provides an interface between the steady transmit rate of the two byte interface of the Serdes macro.
  - Terminates alignment side band signals and creates K character indications for each byte stored in the FIFO.

- **TM CPRI L1 Inband Control**
  - TM L1 inband configuration register allow to choose the source of L1 Inband data from any of 6 RM link or TM itself
  - LOF, LOS, SDI, RAI is supported

- **Delta and PE1, PE2 Preparation Offset is Controlled by AT**
  - Supports Delta modulo and offset register
  - AT also has two PE preparation event modulo and offset registers

CI, CO (CPRI Input and Output) Module

- Provides conversion between CPRI frame format and internal data format
- IQ data bit interleave/de-interleave within antenna carrier samples
- Byte aligns 7- and 15-bit IQ data to internal 32-bit data bus
- For 7-bit format, IQ data sign extension to yield 8 bits
- For 15-bit format, IQ data sign extension to yield 16 bits
- Supports pass-through of ‘r’ bits in 8-bit UL and 16-bit DL at 2x link rate
- Provides ‘I’ or ‘Q’ saturation for the transmitter

RT (Re-transmitter) Module

Insertion Mode:

- OBSAI packet message insertion
- OFDM DL where each node may insert an entire DL stream
- WCDMA DL (first node in the daisy chain)

Redirection Mode: When the link is used for UL

Addition mode:

- WCDMA DL daisy chain aggregation
- same function as 64x+

Combiner/De-combiner:

- AIF2 does not support combiner/de-combiner any more

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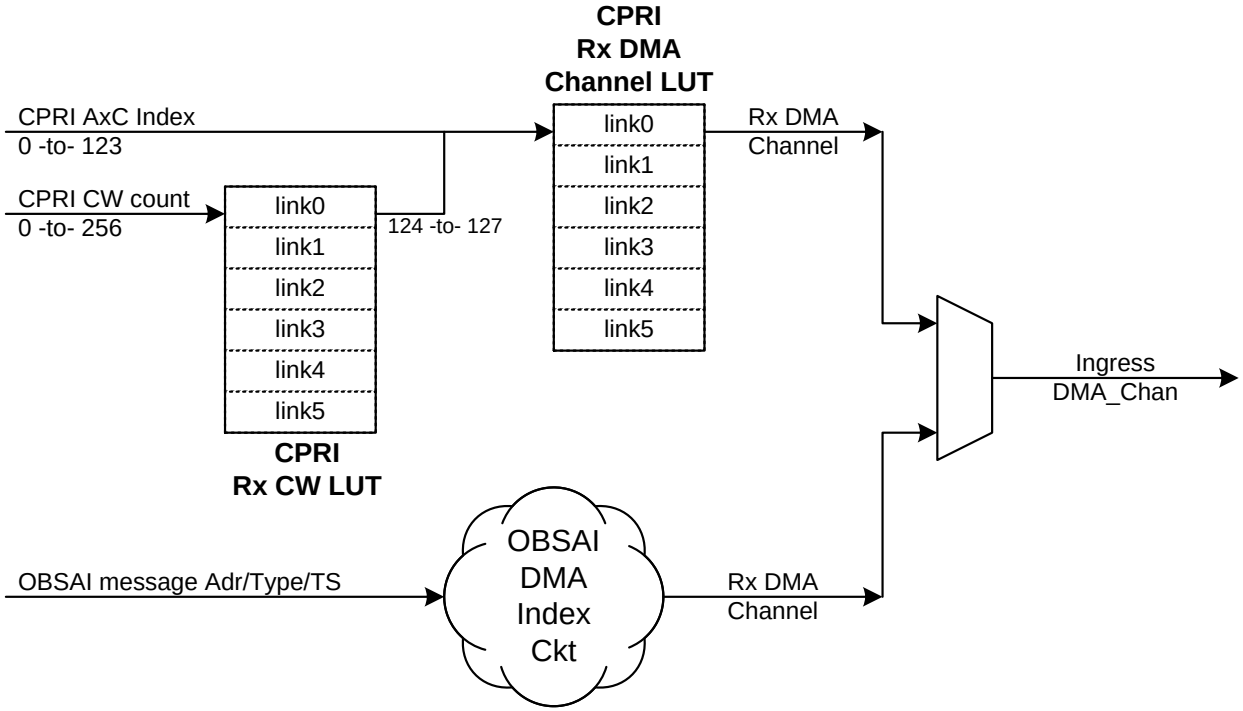
CPRI/OBSAI DMA Channel Addressing



- OBSAI message has Addr/Type/TS data and it is used to make a decision for incoming data routing.
- CPRI uses positional based predefined position for different streams of data.
- CPRI uses four channels per link to transfer control data.

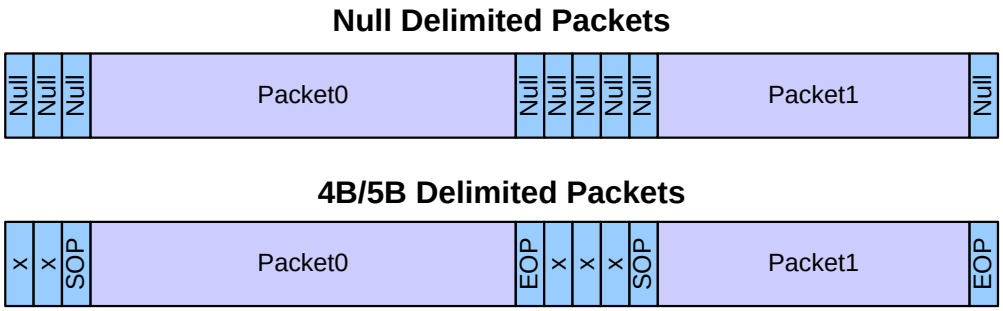
CPRI Protocol Specific

CPRI Control Data

- Slow C&M (HDLC) ← Not Supported by AIF2
- Fast C&M (Fast Ethernet) ← Supported and extended by AIF2
- CPRI supports 4b/5b encoding, decoding and Ethernet packet inserting and parsing
- Adding or stripping SOP (start of packet) data from/into the frame data
- Using four channels to support CPRI control stream

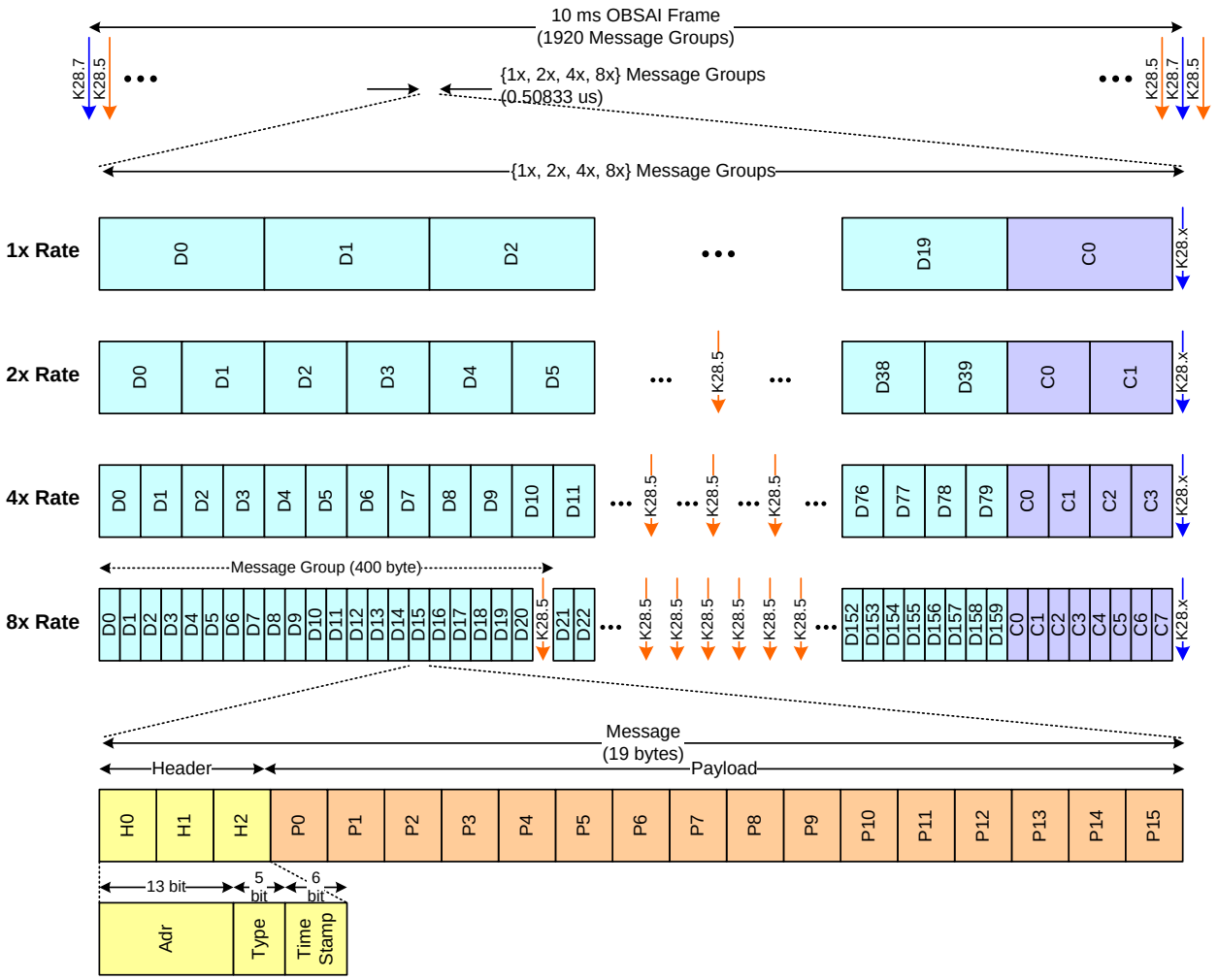
Packet Parsing

- Two mechanisms for packet parsing:
  - Programmable Null delimiter (eg. K27.7 or K29.7)
  - 4B/5B encoding/decoding
- Each of four possible (per link) control streams are configured as to which of the two options is used for that stream .



OBSAI Protocol Specific

OBSAI Frame/Message structure



Linkrate	*i* Message Groups	Data Messages	Control Messages
2x	2	40	2
4x	4	80	4
8x	8	160	8

- There is a special OBSAI address 0x1FFF for empty message slot.
- 8x link requires scrambler .
- CRC error check is provided for the following types:
  - Control Messages: 16bit CRC
  - Generic Packet Type: 16-bit CRC
  - Ethernet Type: 32-bit CRC

OBSAI Protocol Specific: Time Stamp

AxC Data Time Stamp

The 6 bits of time stamp start at 6'b000000 at the radio frame boundary and increment by +1 every OBSAI message. The time stamp value ranges from 0-to-63.

Ethernet Time Stamp

SOP: 6'b100000
MOP: 6'b000000
EOP: 6'b1XXXXX (XXXXX: indicates the number of bytes from the start of RP3 payload containing MAC frame data (counting started from the byte after the header)

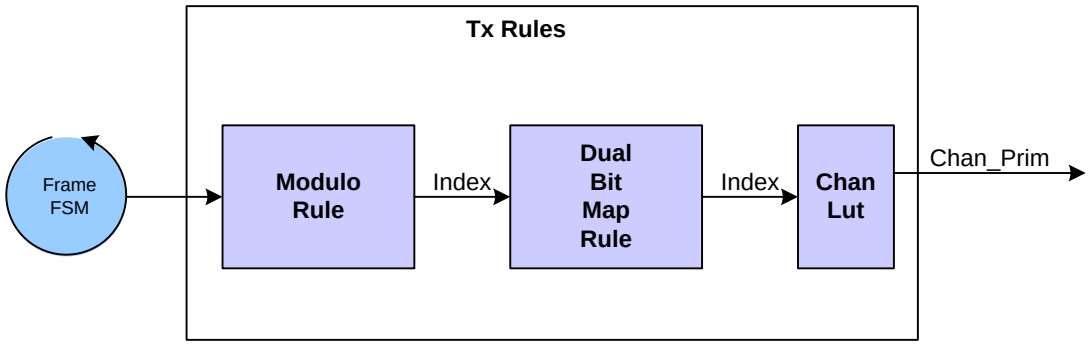
Generic Packet Time Stamp

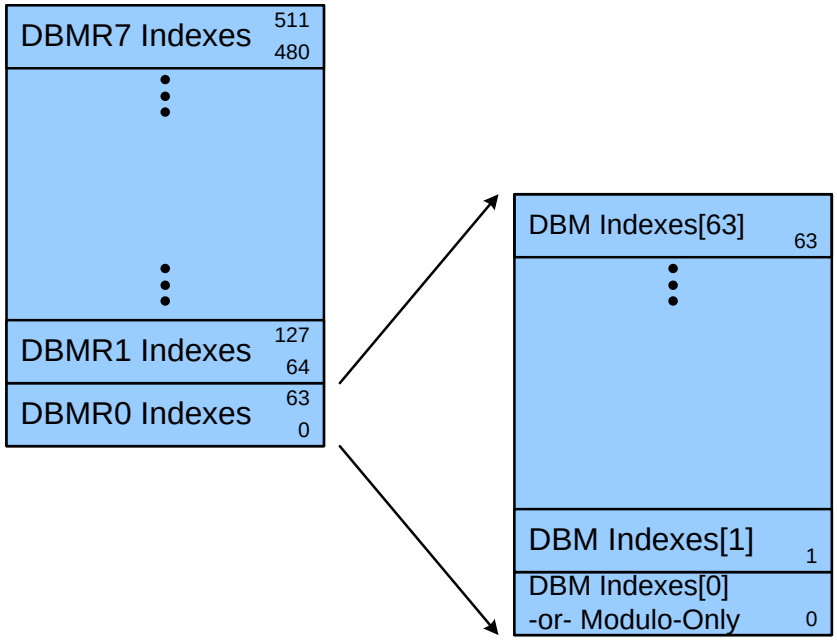
SOP: 6'b10XXXX
MOP: 6'b00XXXX
EOP: 6'b11XXXX (XXXX: is an extension of OBSAI address and is the same for all elements within the packet)

PE (Protocol Encoder) Module: OBSAI

The AIF2 PE Transmission Rule implementation has three parts:

1. 64 Modulo rules
   - User can assign one modulo rule per link OR
   - Multiple rules per link for generic mode
2. 64 Dual Bit Map Rules
   - One DBMR can control a maximum of 64 channels.
   - Channel 0 could be used for Modulo-only mode.
3. 4096 Channel Lookup Tables
   - The channel LUT used mapping transmission rule indexes from the 64 rules into DB channel.
   - Split across eight different RAMs





PE (Protocol Encoder) Module: CPRI

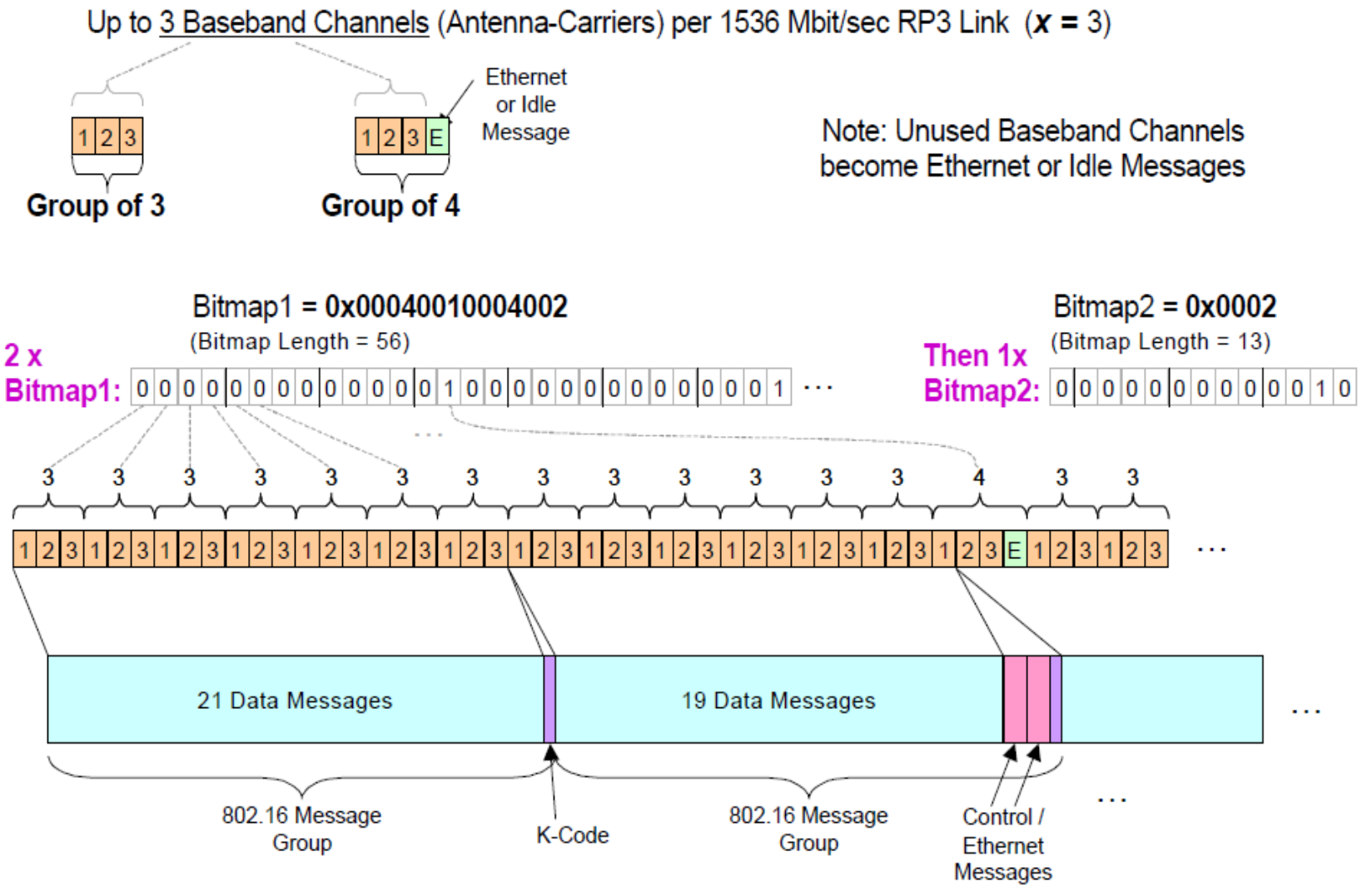
- AIF2 uses the OBSAI Dual-Bit Map FSM (DBMF) concept for configuring the use of CPRI bandwidth between AxC.
- The DBMF is essentially a simple round robin TDM of AxC with the addition of a programmable bubble insertion at the end of each cycle of round robin.

- One Dual Bit Map Rule per Link
  - One DBMR can control a maximum of 128 channels per link.
  - No Modulo rule concept for CPRI.
  - Bubble base unit is the size of sample (1/4 size of OBSAI bubble).

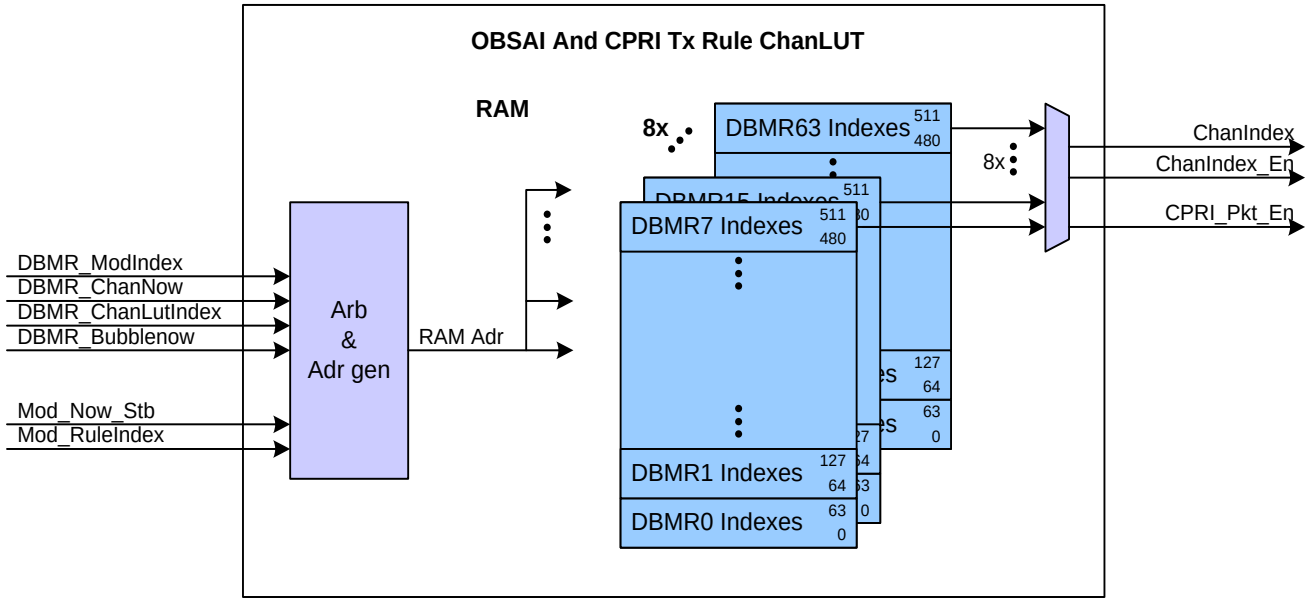
- 128 Channel lookup tables per Link
  - The channel LUT used mapping transmission rule indexes from the DBMR into real DB DMA channels.
  - User can choose between packet mode or circuit mode for each channel LUT.

PD, PE Module: Dual-Bit Map Rule

Illustration of OFDM data transmission through OBSAI link (2x link speed)

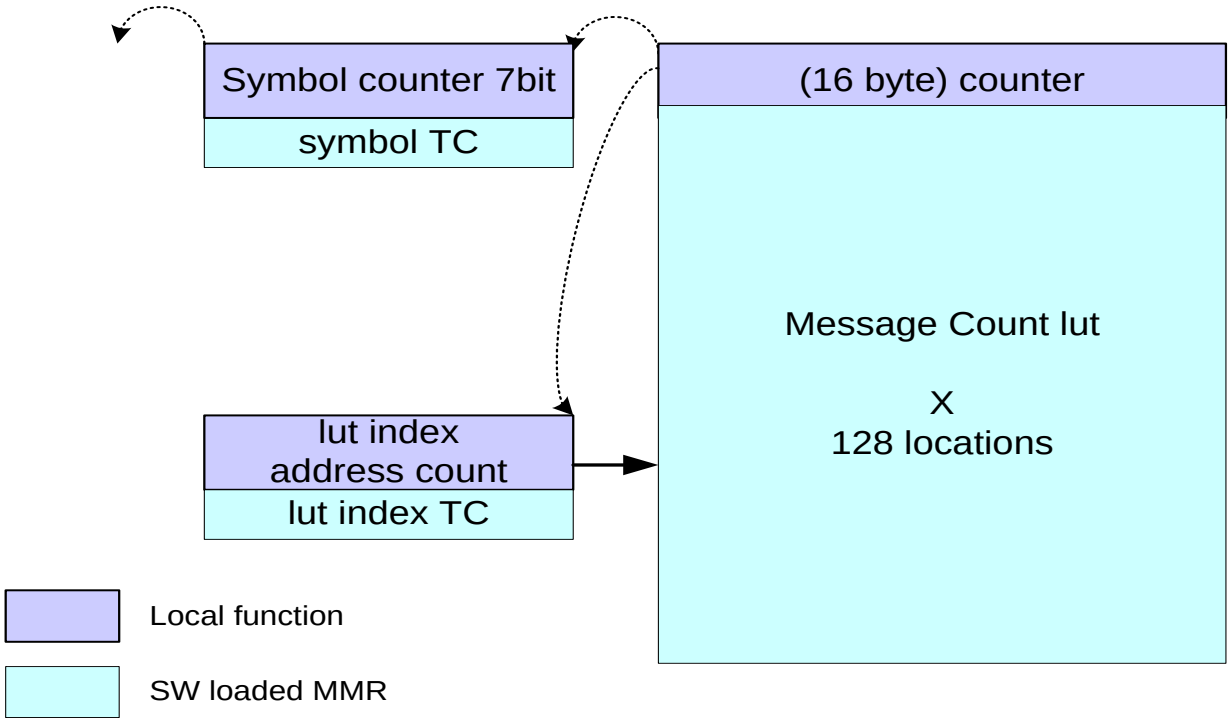


PD, PE Module: Channel Lookup Table



- CPRI uses channel LUT 0 ~ 5 for each link and only uses 128 rules from each LUT instead of using 512 rules like OBSAI.
- CPRI RAM usage:
  - Link0: Ram0, 0-127 (address 128-511 unused)
  - Link1: Ram1, 0-127
  - …
  - Link5 Ram5, 0-127

PD, PE Module: AxC Framing Counter



- PD/PE timers increment based on samples received:
  - AT: counts clock cycles
  - PD & PE: OBSAI: count groups of 16 bytes (ie. 4 samples)
    CPRI: count groups of 4 bytes for PD and 16 bytes for PE

- PD/PE simultaneously supports six different sets of terminal counts for LTE
  - AT: supports only one set of terminal counts

DB (Data Buffer) Module

- 16-byte (quad word) interface
- Supports mix of FIFO (Packet data) and circular buffers (DirectIO)
- Supports up to 128 buffer channels (AxC's and packet mode flows)
  - Ingress and egress has its own 128 buffers
- FIFO size is programmable per-buffer channel (with limitations)
- Circular Buffer for DIO size is selectable between 128 and 256 bytes
  - 28 bytes for WCDMA
  - 256 bytes for LTE
- Buffer channel programmable data swapping
- Buffer channel programmable IQ ordering
- DB debug Data RAM – 1K x 16 byte
- DB debug sideband data RAM – 1K x 24 bit
- Data Trace Support formats data trace data and framing data from RM into 128-bit quad words
- Data Trace RAM - 160 x 16 byte

DMA Modules (AD, PKTDMA)

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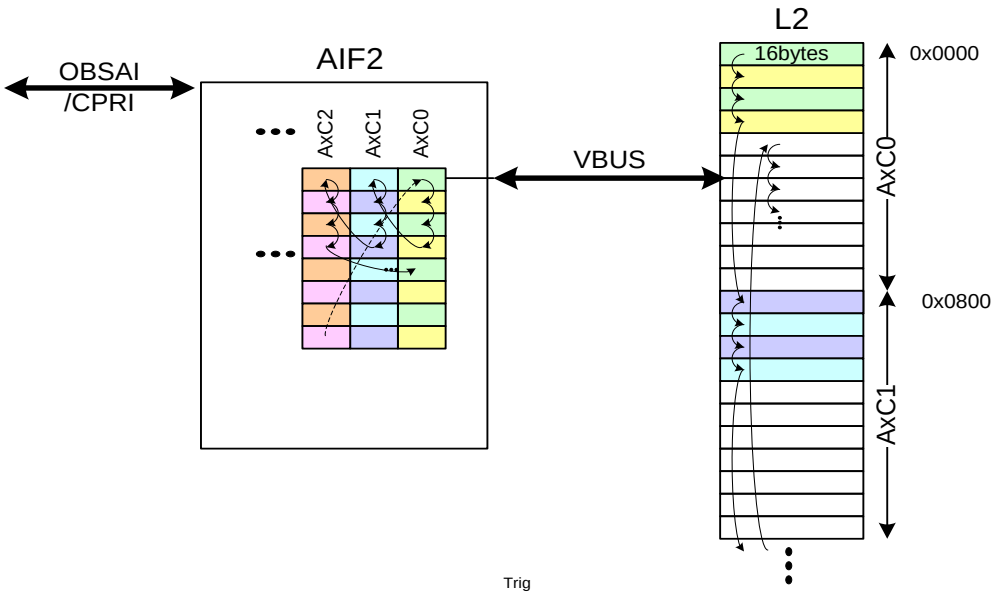
AD (AIF2 DMA) Module

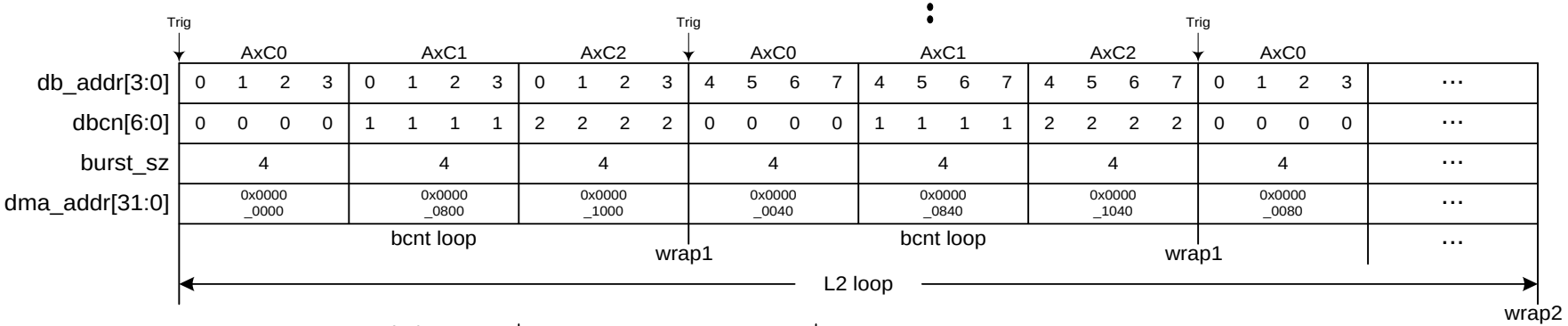
- Supports separate ingress scheduler and egress scheduler
- Supports direct IO, AxC packet, non-AxC packet, data trace
- Supports EOP counter for both directions
- Supports three DIO engines for both directions
- User can add or delete AxC channel on-the-fly (dynamic configuration).

<u>DIO configuration</u>

- DBCN (Dio Buffer Channel Number) table selection
- Number of quad words
- Number of AxC
- Number of max burst size (1,2,4 QW)
- Number of blocks
- DIO base address (source, destination)
- Burst address stride
- Block address stride
- DBCN (max 64 channels)

DIO Example : L2/RSA





num_qw = 4 Qwords / AxC
num_axc = 3 AxCs (up to 64)
dma_num_blks = N blocks (up to 32)

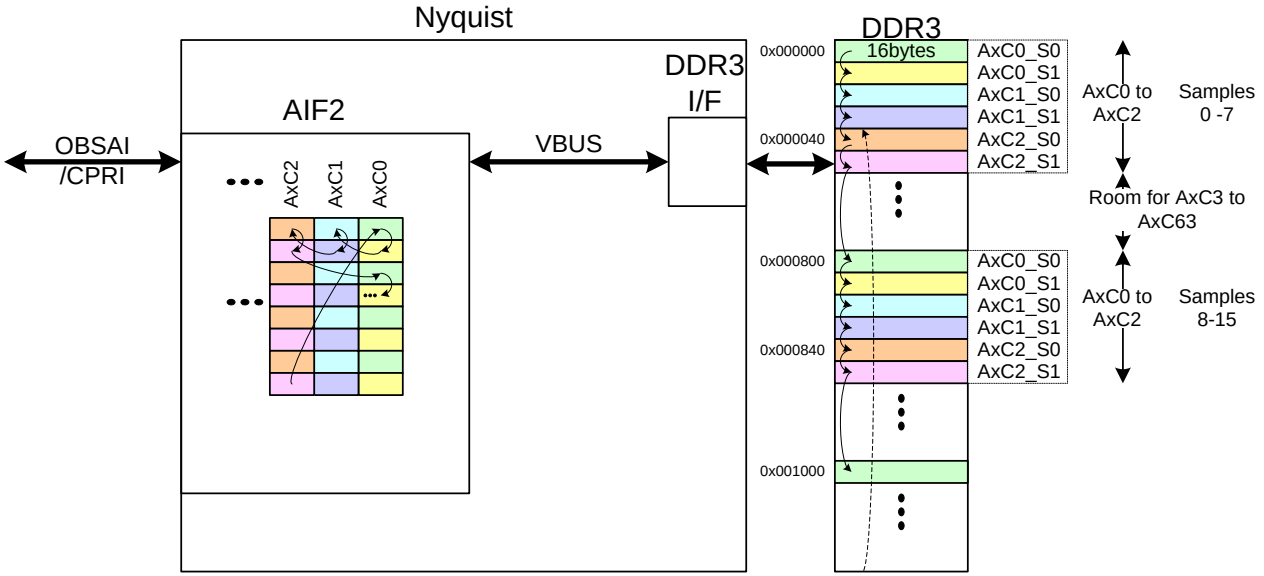
wrap1 = num_qw x num_axc

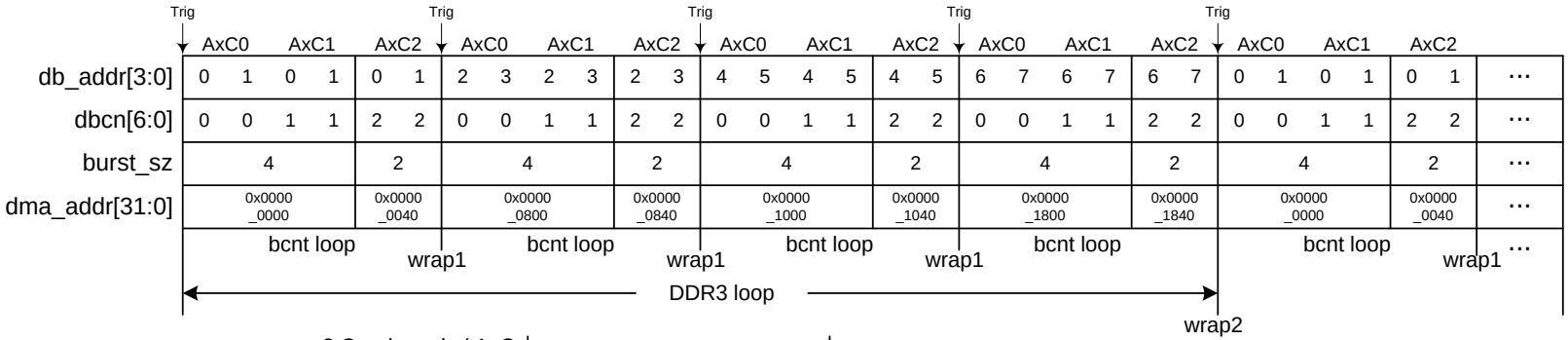
wrap2 = num_qw x num_axc x dma_num_blks

dma_brst_ln = 4

dma_base_addr = 0x0000_0000
dma_brst_addr_stride = 0x080 x 0x10
dma_blk_addr_stride = 0x004 x 0x10

DIO Example : DDR3





num_qw = 2 Quad words / AxC
num_axc = 3 AxCs (up to 64)
dma_num_blks = N blocks (up to 16 x 320 = 5,120)

wrap1 = num_qw x num_axc

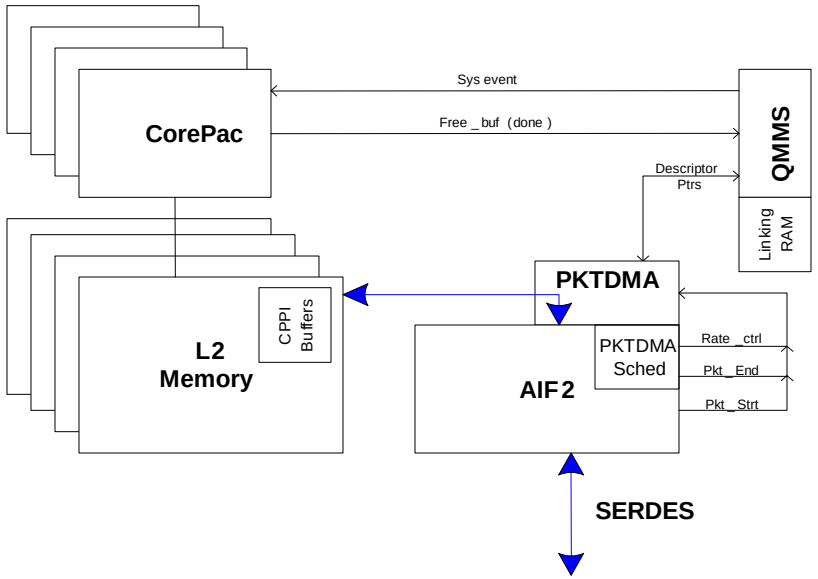
wrap2 = num_qw x _num_axc x num_blks

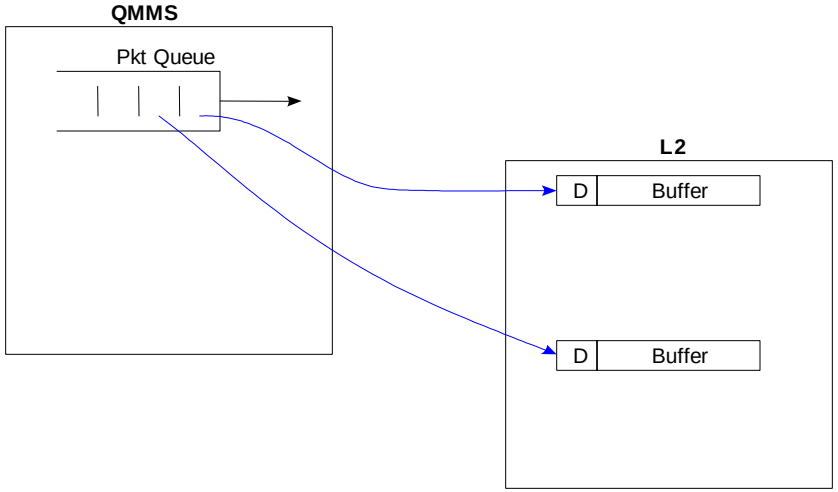
dma_brst_ln = 4

dma_base_addr = 0x0000_0000
dma_brst_addr_stride = 0x004 x 0x10
dma_blk_addr_stride = 0x080 x 0x10

PKTDMA (Packet DMA) Module

- PKTDMA supports AxC packet, non-AxC packet, Ethernet packet.
- DIO use only PKTDMA channel 128 to transfer all AxC data.
- AIF2 PKTDMA supports host descriptor and Monolithic descriptor.
  - Host: Used for control, Ethernet generic traffic (CPRI should use Monolithic for this)
  - Monolithic: Used for LTE, WiMax, TD-SCDMA, GSM antenna data
- Multicore Navigator queues:
  - Free queue (Rx, Tx)
  - Tx queue, Rx queue
  - Tx completion queue (recycled to Tx free queue)





Protocol-Specific Field in Descriptor

Bits	Name	Description
31:16	Reserved	
15	Ingress/Egress	0: Ingress 1: Egress
14:7	Symbol Number	Symbol number (0x00 – 0xFF)
6:0	AxC Number	AxC number (0x00 – 0x7F)

- The Monolithic packet descriptor header for AIF2 is exactly 16 bytes (one VBUS 128 data phase)
- Many of the fields are required by Navigator, some of the remaining bits (4 bytes) are allocated for protocol specific use. The Monolithic packet type uses some of the protocol specific bits for Radio Standard specific information:
  - Ingress/Egress selection
  - AxC number
  - Symbol Number (or GSM Time Slot Number)

Multicore Navigator Example

Ingress: AIF2 Reception – DMA-to-L2 RAM

1. CorePac initializes Navigator (PKTDMA, QM)
   - Buffer initialization
   - Fill out descriptors
   - Make buffer region and Link RAM
2. Queue setup:
   - Free Queue
   - Rx Queue
   - CorePac pushes descriptors into the Free Queue
3. AIF2 starts receiving packets through OBSAI or CPRI and AD starts transferring burst data to PKTDMA (use same channel number).
4. PKTDMA pops descriptor from Free Queue and fill incoming data into it, then pushes the populated descriptor into the Rx Queue.
5. QMMS creates system event to CorePac.
6. CorePac pops descriptor from Rx queue, reads the data, and pushes the descriptor into the Rx Free Queue for recycling.

Egress: L2 RAM – DMA-to-AIF2 Transmission

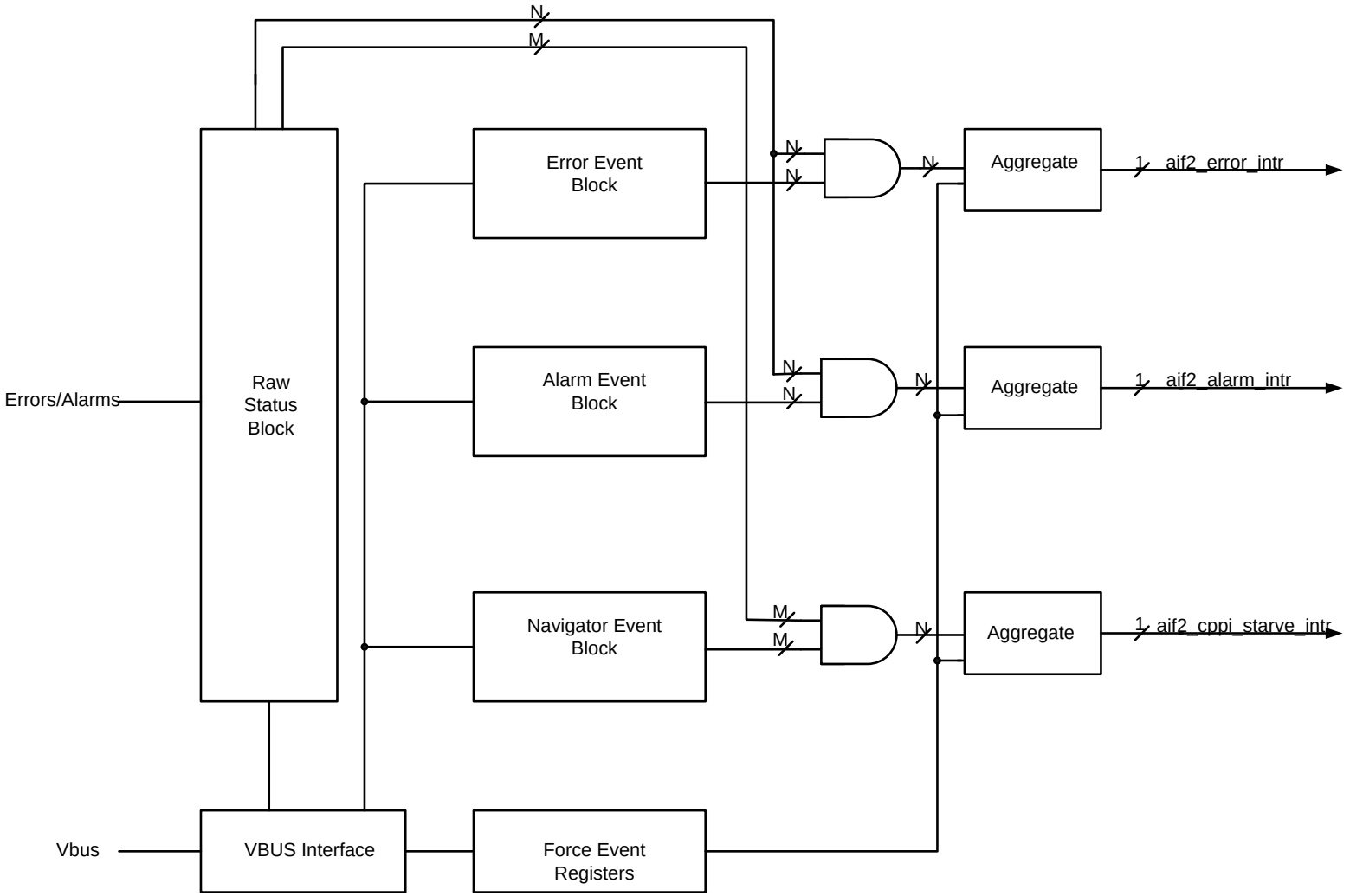
1. CorePac initializes Multicore Navigator (PKTDMA, QMSS)
   - Buffer initialization
   - Push empty descriptors into free queue
   - Make buffer region and Link RAM
2. CorePac creates packet
   - CorePac pops a descriptor from the free queue and fills in
   - CorePac pushes the descriptor into the Tx Queue
3. AIF2 DMA Scheduler controls PKTDMA to transfer packet.
4. PKTDMA pops descriptor from Tx Queue and fills buffer data into it.
5. PKTDMA transfers data to AIF2 AD.
6. PKTDMA pushes the used descriptor into the Free Queue for recycling (or pushes it into the Tx complete queue if user wants to do something else).
7. AIF2 starts sending packets through OBSAI or CPRI.

Error and Exception Handling (EE)

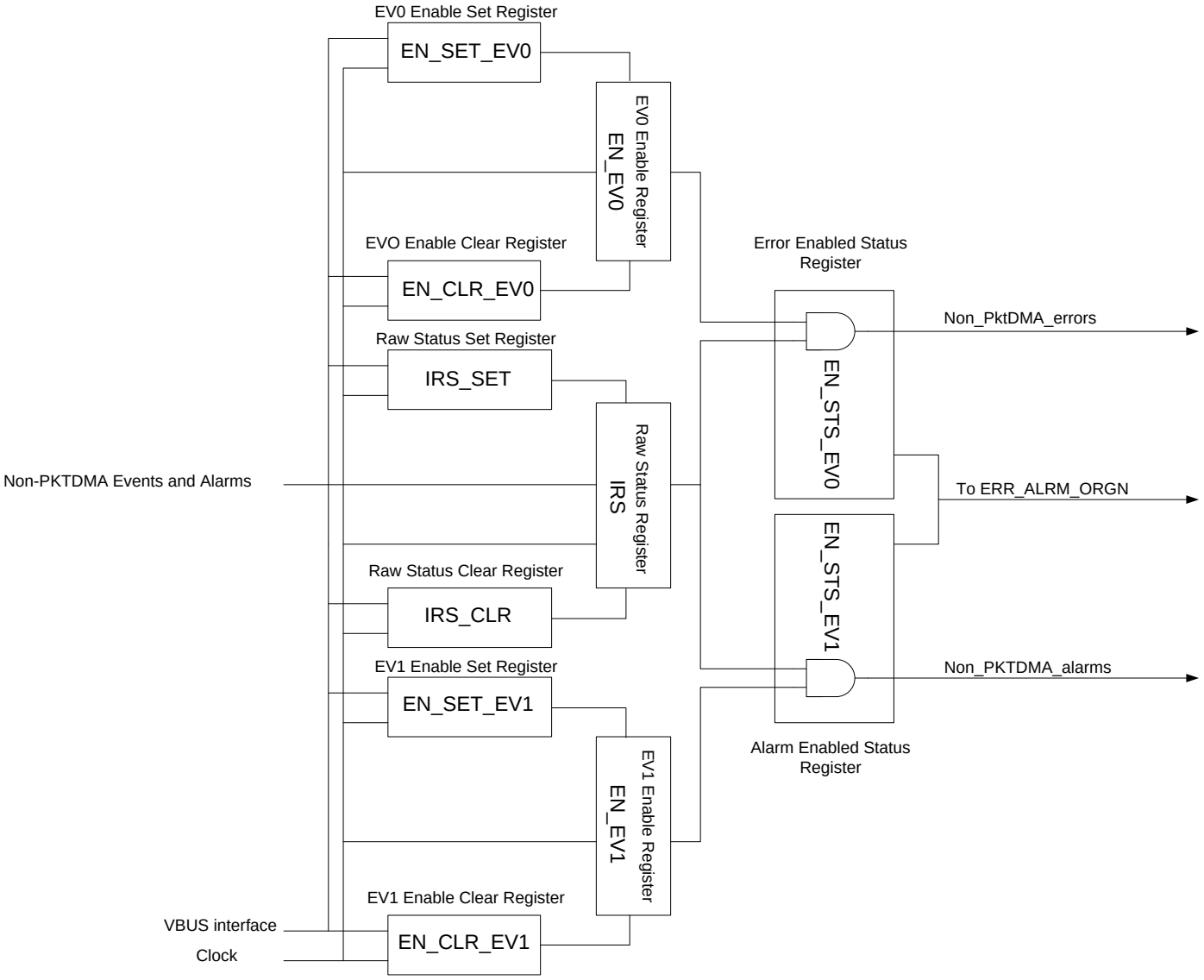
- Evolution from AIF1 to AIF2
- AIF2 Timer (AT)
- Physical Layer Modules (SD, RM, TM, RT)
- Protocol Layer Modules (PD, PE, DB)
- DMA Modules (AD, PKTDMA)
- Error and Exception Handling (EE)

EE (Error and Exception Handler) Module

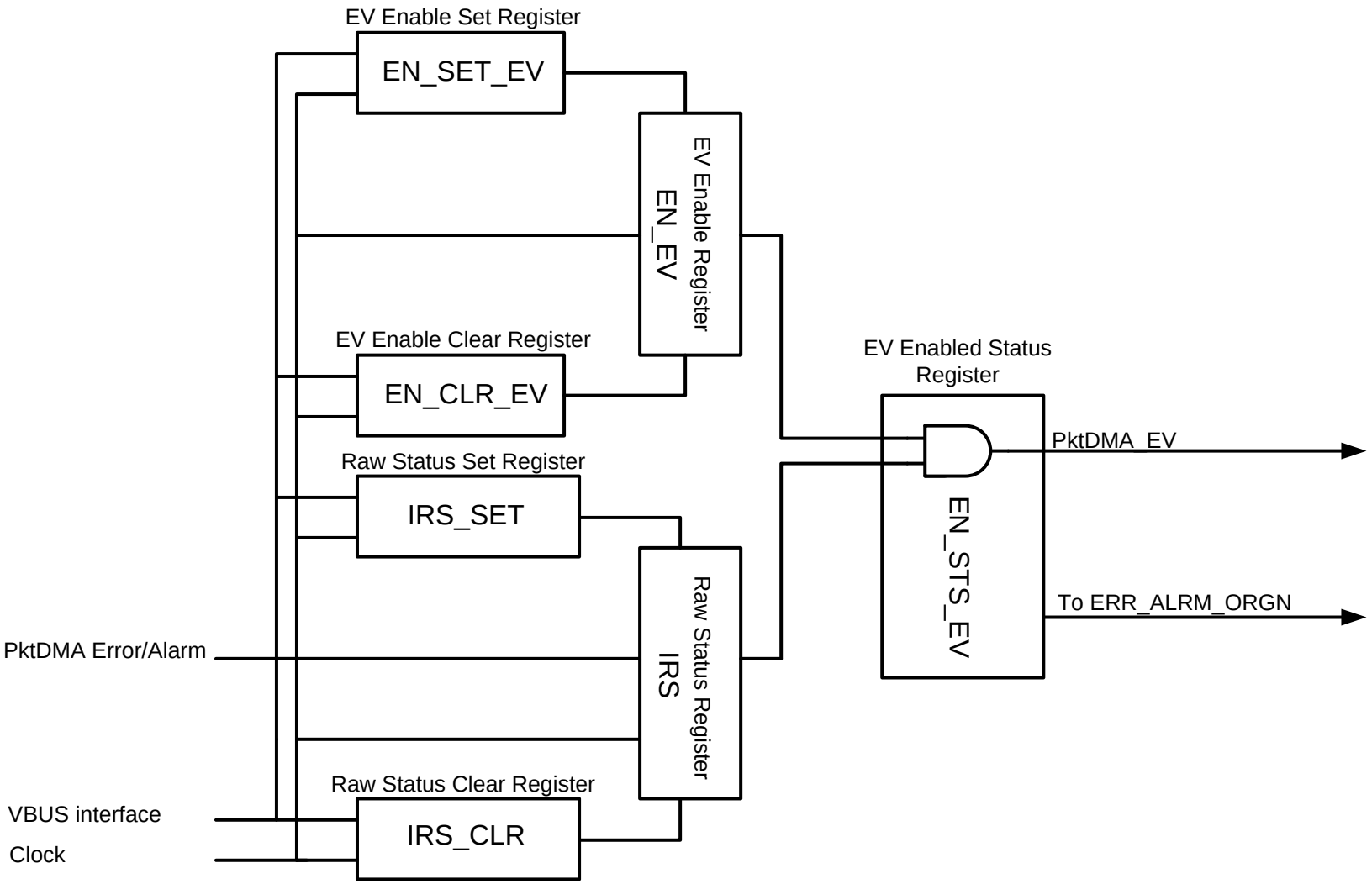
EE Functional Block Diagram



EE Non-PKTDMA Error/Alarm Condition



EE PKTDMA Error/Alarm Condition



For More Information

- For more information, refer to the Antenna Interface 2 (AIF2) User Guide http://www.ti.com/lit/SPRUGV7
- For questions regarding topics covered in this training, visit the support forums at the TI E2E Community website.