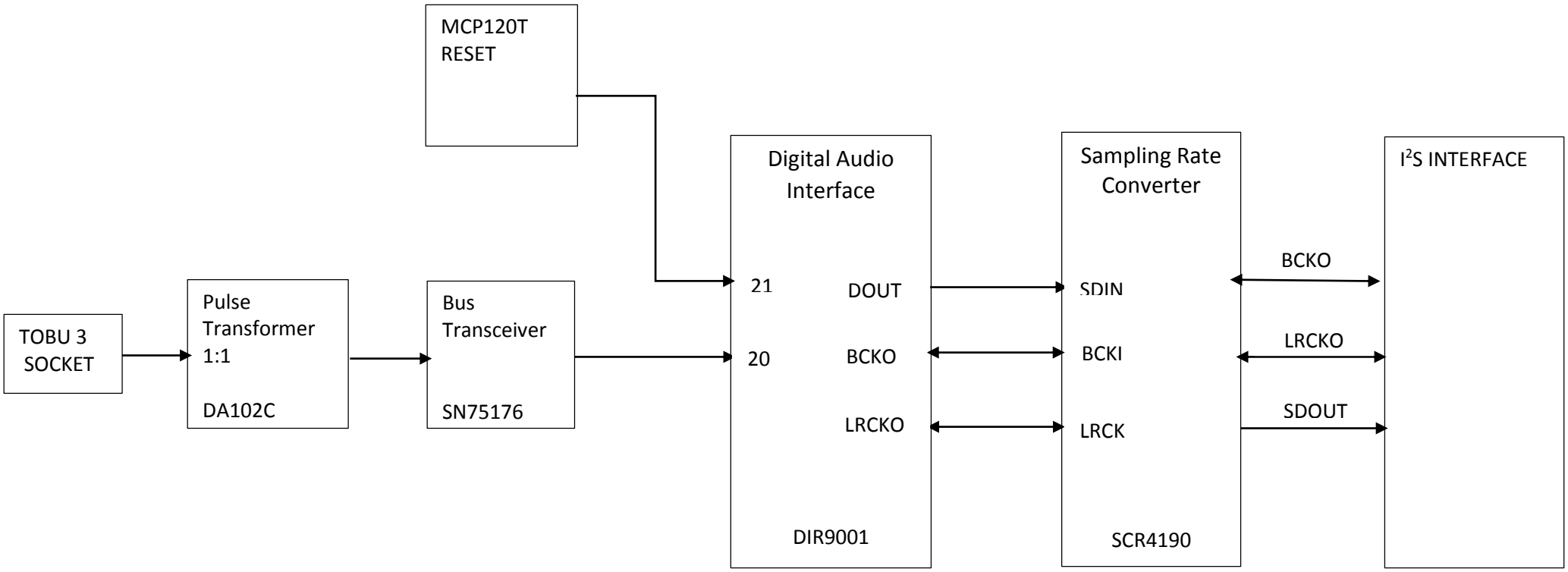
ARCHITECTURE FOR S/PDIF TO I2S CONVERTER



TOBU 2 SOCKET

It is used to connect the S/PDIF input for digital audio

TRANSFORMER

This is used for isolation to avoid ground loop problem

BUS TRANSCEIVER

Used to convert the input voltage from the transformer to TTL since Pin RXIN20 of the Digital Audio Interface chip (DIR9001) accepts only level voltages of 3.3 V or 5 V.

DIGITAL AUDIO INTERFACE

It accepts the output of the transceiver and converts it to I^2S format. It has maximum sample rate of 96 KHz

SAMPLING RATE CONVERTER

It is used to convert the sample rate from 96 KHz to 192 KHz to match up with the Sampling frequency of the input ADC converter.

I^2S INTERFACE