

Guidelines for configuring the AIC1x:

Please make sure to follow this procedure when resetting the codec (necessary for the automatic cascade detection (ACD) mechanism). For stand-alone slave it is best if the codec is programmed for Turbo Mode (e.g. BCLK into codec is  $>16 \times FS \times mode$ ):

- 1) Tristate the serial port of the host processor (provide SCLK and MCLK and keep DIN low for stand alone slave) and apply a low going pulse to the /RESET pin (**synchronized with MCLK if in master or cascade modes**). We recommend 10ms.
- 2) Wait **at least 132 MCLK periods after releasing the /RESET pin (from low to high)** before setting the serial port to normal operation.
- 3) At this instant, the master codec will generate an  $FS = MCLK / (16 \times M \times N \times P)$  where  $P=8$ ,  $M=16$  and  $N=6$ .  $SCLK = 16 \times FS \times (\# \text{ of codecs}) \times (2 = \text{prg. mode})$ . This does not apply for stand alone slave configuration.
- 4) Wait at least two FS frames before programming the codec. **Please make sure that 0x0000 is sent to every command time slot if not programming any registers in programming mode (any random data might change the register values).**
- 5) In a general sense, it is recommended to program the codec in the following order. Clearing the overflow flags is not required if the host code does not implement any algorithm that depends on ADC or DAC overflow.

CONFIGURATION STEP	FUNCTION
1	Reset the AIC by set D5=1 at the CR#3
2	Read back from CR#1 (to reset possible overflow flags).
3	Configure CR#2
4	Configure CR#4
5	Configure CR#5
6	Configure CR#6
7	Configure CR#3
8	Configure CR#1

- 6) Registers 1, 2, 3 and 4 can be programmed in broadcast mode, by setting bit D11 of the master codec's secondary communication time slot to 1. If broadcasting, the rest of the control data time slots can be kept low. The reason CR#1 is shown as the last register in the table above is to give the flexibility to set the codec in 'Continuous Data Transfer mode'.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address				RW	BC	1	1	1	Control Register Content						

If using i2c, a broadcast write can be achieved by sending 11111xxx as the register address, where xxx denotes the register address in binary.