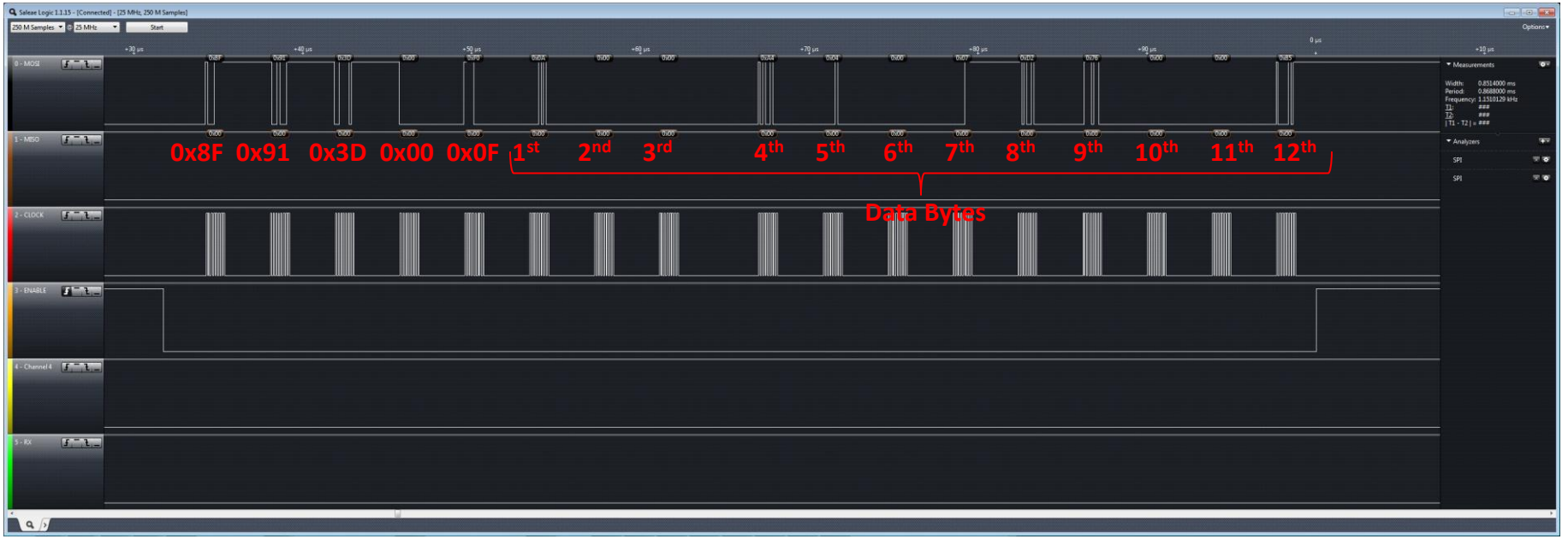
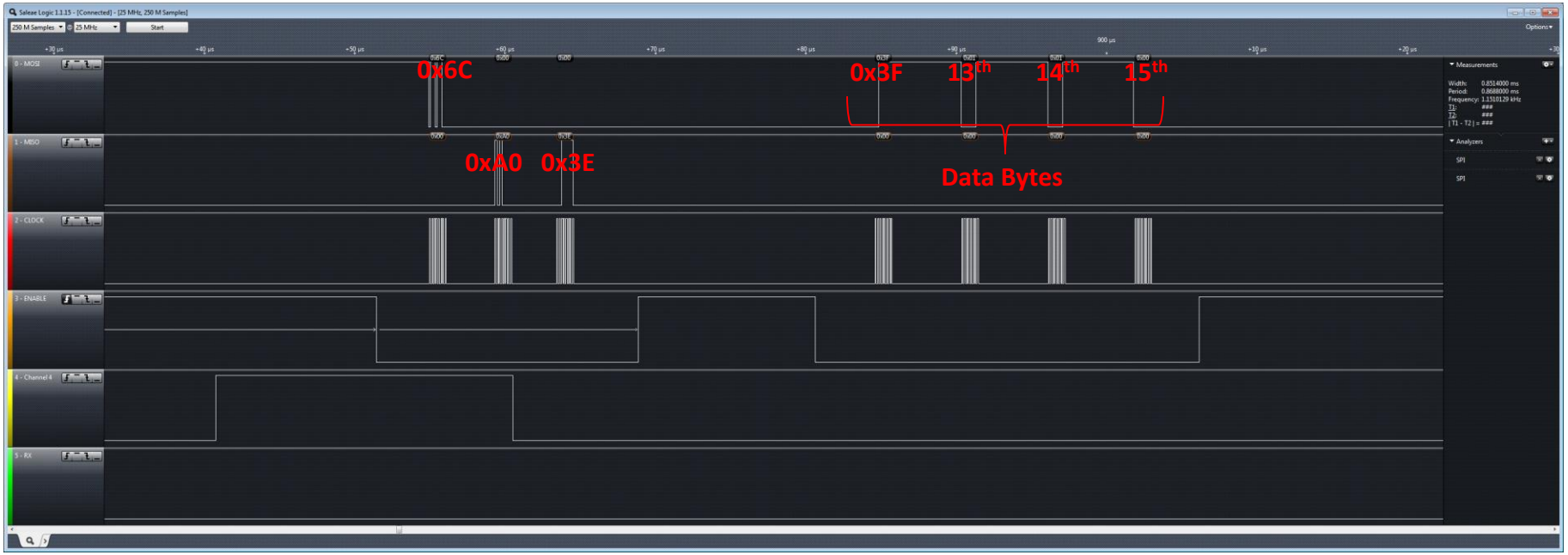
Sending Header Packet



FIFO Interrupt

- 851uS after we sent the first 12 bytes an IRQ interrupt was triggered.
- IRQ register = **0x0A** ➔ TX ongoing and FIFO low interrupt.



TX Complete

- IRQ Register = 0x80 ➔ TX Complete