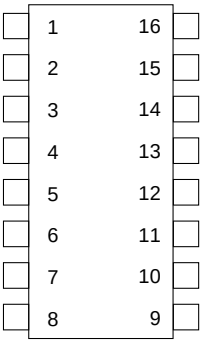
TMS3705A
TRANSPONDER BASE STATION IC

REV.1.0 - JUNE 1999

- **Base Station IC for RF Identification Systems built on TIRIS Transponder Technology**
- **Drives Antenna**
- **Sends Modulated Data to Antenna**
- **Detects and Demodulates Transponder Response (FSK)**
- **Short Circuit Protection**
- **Diagnosis**
- **Sleep Mode Supply Current 0.2 mA**
- **Designed for Automotive Requirements**
- **Package SO 16**

D Package
(Top View)



TMS3705AD

description

The transponder base station IC is used to drive the antenna of a TIRIS (**T**exas **I**nstruments **R**egistration and **I**dentification **S**ystem) transponder system, to send data modulated on the antenna signal, and to detect and demodulate the response of the transponder. The response of the transponder is a FSK signal (frequency shift keyed). The high or low bits are coded in two different high-frequency signals (134,2 kHz for low bits and 123 kHz for high bits, nominal). The transponder induces these signals in the antenna coil according an internally stored code. The energy the transponder needs to send out the data is stored in a charge capacitor in the transponder. The antenna field charges this capacitor in a preceding charge phase. The IC has an interface to an external microcontroller.

The interface pins are protected against overcurrent due to short-circuit at the interconnections, e. g. by using external components and internal clipping diodes.

There are two configurations for the clock supply to both the microcontroller and the base station IC:

1) Microcontroller and base station IC are supplied with a clock signal derived from only one resonator: The resonator is attached to the microcontroller. The base station IC is supplied with a clock signal driven by the digital clock output of the microcontroller. The clock frequency is either 4 MHz or 2 MHz depending on the selected microcontroller type.

2) Both the microcontroller and the base station have their own resonator.

The base station IC has a PLL on-chip that generates a clock frequency of 16 MHz for internal clock supply only.

Circuit Description

Power Supply

The IC is supplied with 5 V by an external voltage regulator via two pairs of supply lines, one for providing the driver current for the antenna and for supplying the analog part in front of the digital demodulator and one for supplying the other blocks.

The power supply supplies a power-on reset that brings the control logic into idle mode as soon as the supply voltage drops under a certain value.

In sleep mode the sum of both supply currents is reduced to 0.2 mA. The base station IC falls into sleep mode 100 ms after TXCT has changed to high. When TXCT changes to low or is low, the base station IC immediately goes into and remains in normal operation.

Oscillator

The oscillator generates the clock of the base station IC of which all timing signals are derived. Between its input and output a crystal or ceramic resonator is connected that oscillates at a typical frequency of 4 MHz. If a digital clock signal with a frequency of 4 MHz or 2 MHz is supplied to pin OSC1, the signal can be used to generate the internal operation frequency of 16 MHz.

The oscillator block contains a PLL that generates the internal clock frequency of 16 MHz from the input clock signal. The PLL multiplies the input clock frequency depending on the logic state of the input pin F_SEL by a factor of 4 (F_SEL is high) or by a factor of 8 (F_SEL is low).

In sleep mode the oscillator is switched off.

Predrivers

The predrivers generate the signals for the four power transistors of the full bridge using the carrier frequency generated by the frequency divider. The gate signals of the p-channel power transistors (active low) have the same width (± 1 cycle of the 16 MHz clock), the delay between one p-channel MOSFET being switched off and the other one being switched on is defined to be 12 cycles of the 16 MHz clock. In write mode the first activation of a gate signal after a bit pause is synchronized to the received transponder signal by a phase shift of 180°.

Full Bridge

The full bridge drives the antenna current at the carrier frequency during the charge phase and the active time of the write phase. The minimal load resistance the full bridge sees between its outputs in normal operation at the resonance frequency of the antenna is 43.3 Ω. When the full bridge is not active, the two driver outputs are switched to ground.

Both outputs of the full bridge are protected independently against short-circuits to ground.

In case of an occurring short-circuit, the full bridge is switched off in less than 10 µs in order to avoid a drop of the supply voltage. After a delay time of less than 10 ms the full bridge is switched on again to test if the short-circuit is still there. An overcurrent due to a resistive short to ground that is higher than the maximum current in normal operation but lower than the current threshold for overcurrent protection does not need to be considered.

RF Amplifier

The RF amplifier is an operational amplifier with a fixed internal voltage reference and a voltage gain of 5 defined by external resistors. It has a high gain-bandwidth product of at least 2 MHz in order to show a phase shift of less than 16° for the desired signal and to give the possibility to use it as a low-pass filter by adapting additional external components.

The input signal of the RF amplifier is DC coupled to the antenna. The amplitude of the output signal of the RF amplifier is higher than 5 mV peak-to-peak.

Band-Pass Filter and Limiter

The band-pass filter provides amplification and filtering without external components. The lower cut-off frequency is about a factor of 2 lower than the average signal frequency of 130 kHz, the higher cut-off frequency is about a factor of 2 higher than 130 kHz.

The limiter converts the analog sine-wave signal to a digital signal. It provides a hysteresis depending on the minimal amplitude of its input signal. The duty cycle of its digital output signal is between 40 % and 60 %. The band-pass filter and the limiter together have a high gain of at least 1000.

Diagnosis

The diagnosis is carried out during the charge phase to detect whether the full bridge and the antenna are working. When the full bridge drives the antenna, the voltage across the coil exceeds the supply voltage so that the voltage at the input of the RF amplifier is clamped by the ESD-protection diodes. For diagnosis, the SENSE pin is loaded on-chip with a switchable resistor to ground so that the internal switchable resistor and the external SENSE resistor form a voltage divider, while the internal resistor is switched off in read mode. When the voltage drop across the internal resistor exceeds a certain value, the diagnosis block passes the frequency of its input signal to the digital demodulator. The frequency of the diagnosis signal is accepted, if eight subsequent time can be detected, all with their counter state within the range of 112 ... 125, during the diagnosis time (at most 0.1 ms). The output signal is used during the charge phase only else it is ignored.

When the short-circuit protection switches off one of the full-bridge drivers, the diagnosis also indicates an improper operation of the antenna by sending the same diagnostic byte to the microcontroller as for the other failure mode.

During diagnosis, the antenna drivers are active. In synchronous mode the antenna drivers remain active up to 1 ms after the diagnosis is performed, without any respect to the logic state of the signal at TXCT (thus enabling the microcontroller to clock out the diagnosis byte).

Power-On Reset

The power-on reset generates an internal reset signal to allow the control logic to start up in the defined way.

Frequency Divider

The frequency divider is a programmable divider that generates the carrier frequency for the full-bridge antenna drivers. The default value for the division factor is the value 119 needed to provide the nominal carrier frequency of 134.7 kHz generated from 16 MHz. The resolution for programming the division factor is one divider step that corresponds to a frequency shift of about 1.1 kHz. The different division factors needed to cover the range of frequencies for meeting the resonance frequency of the transponder are 114 to 124.

Digital Demodulator

The input signal of the digital demodulator comes from the limiter and is frequency-coded according to the high- and low-bit sequence of the transmitted transponder code. The frequency of the input signal is measured by counting the oscillation clock for the time period of the input signal. As the high-bit and low-bit frequencies are specified with wide tolerances, the demodulator is designed to distinguish the high-bit and the low-bit frequency by the shift between the two frequencies and not by the absolute values. The threshold between the high-bit and the low-bit frequency is defined to be 6.5 kHz lower than the measured low-bit frequency and has a hysteresis of ±0.55 kHz.

The demodulator is controlled by the control logic. After the charge phase (that is during read or write phase) it measures the time period of its input signal and waits for the transponder resonance-frequency measurement to determine the counter state for the threshold between high-bit and low-bit frequency. Then the demodulator waits for the occurrence of the start bit. For that purpose, the results of the comparisons between the measured time periods and the threshold are shifted in a 12-bit shift register. The detection of the start bit comes into effect when the contents of the shift register matches a specific pattern, indicating 8 subsequent periods below the threshold immediately followed by 4 subsequent periods above the threshold. A 2-period digital filter is inserted in front of the 12-bit shift register to make a start bit detection possible in case of a non-monotonous progression of the time periods during a transition from low- to high-bit frequency.

The bit stream detected by the input stage of the digital demodulator passes a digital filter before being evaluated. After demodulation, the serial bit flow received from the transponder is buffered bytewise before being sent to the microcontroller by SCI encoding.

Transponder Resonance-Frequency Measurement

During the pre-bit reception phase, the bits the transponder transmits show the low-bit frequency, which is the resonance frequency of the transponder. The time periods of the pre-bits are evaluated by the demodulator counter. Based on the counter states, an algorithm is implemented that guarantees a correct measurement of the transponder's resonance frequency:

1) A time period of the low-bit frequency has a counter state between 112 and 125.

2) The measurement of the low-bit frequency (the average of eight subsequent counter states) is accepted during the write mode, when the eight time periods have counter states in the defined range. The measurement during write mode is started with the falling edge at TXCT using the fixed delay time at which end the full bridge is switched on again.

3) The counter state of the measured low-bit frequency results in the average counter state of an accepted measurement and can be used to update the register of the programmable frequency divider.

4) The measurement of the low-bit frequency (the average of eight subsequent counter states) is accepted during the read mode, when the eight time periods have counter states in the defined range. The start of the measurement during read mode is delayed in order to use a stable input signal for the measurement.

5) The threshold to distinguish between high-bit and low-bit frequency is calculated to be by a value of 5 or 7 (see hysteresis in threshold) higher than the counter state of the measured low-bit frequency.

SCI Encoder

An SCI encoder performs the data transmission to the microcontroller. As the transmission rate of the transponder is lower than the SCI transmission rate, the serial bit flow received from the transponder is buffered after demodulation and before SCI encoding.

The SCI encoder uses an 8-bit shift register to send the received data bytewise (least significant bit first) to the microcontroller with a transmission rate of 15.625 kbaud (± 1.5 %), one start bit (high) and one stop bit (low), but no parity bit (asynchronous mode indicated by the SYNC bit of the mode control register permanently low). The data bits at the SCIO output are inverted with respect to the corresponding bits sent by the transponder.

The transmission starts after the reception of the start bit. The start byte detection is initialized with the first rising edge. Typical values for the start byte are 81_H or 01_H (at SCIO). The start byte is the first byte to be sent to the microcontroller. The transmission stops and the base station returns to idle state when TXCT becomes low or 20 ms after the beginning of the read phase. TXCT remains low for at least 128 µs to stop the read phase and less than 900 µs to avoid starting the next transmission cycle.

The SCI encoder also sends the diagnostic byte 2 ms after beginning of the charge phase. In case of a normal operation of the antenna, the diagnostic byte AF_H is sent. If no antenna oscillation can be measured or if at least one of the full-bridge drivers is switched off due to a detected short-circuit, the diagnostic byte FF_H is sent to indicate the failure mode.

The SCI encoder can be switched into a synchronous data transmission mode by setting the mode control register bit SYNC to high. In this mode, the output SCIO indicates by a high state that a new byte is ready to be transmitted. The microcontroller can receive the eight bits at SCIO when sending the eight clock signals (falling edge means active) for the synchronous data transmission via pin TXCT to the SCI encoder.

Control Logic

The control logic is the core of the TMS3705 circuit. It contains a sequencer or a state machine that controls the global operations of the base station. This block has a default mode configuration but can also be controlled by the microcontroller via the TXCT serial input pin to change the configuration and to control the programmable frequency divider. For that purpose a mode control register is implemented in this module that can be written by the microcontroller.

The default mode is a read-only mode that uses the default frequency as the carrier frequency for the full bridge. Therefore the mode control register does not need to be written (it is filled with low states), and the communication sequence between microcontroller and base station starts with TXCT being low for a fixed time to initiate the charge phase. When TXCT becomes high again, the module enters the read phase and the data transmission via the SCIO pin to the microcontroller starts.

There is another read-only mode that differs from the default mode only in the writing of the mode control register before the start of the charge phase. The way that the mode control register is filled and the meaning of its contents is described below.

The write-read mode starts with the programming of the mode control register. Then the charge phase starts with TXCT being low for a fixed time. When TXCT becomes high again, the write phase begins in which the data are transmitted from the microcontroller to the transponder via the TXCT pin, the control logic, the predrivers, and the full bridge by amplitude modulation of 100 % with a fixed delay time. After the write phase TXCT goes low again to start another charge or program phase. When TXCT becomes high again, the read phase begins.

The contents of the mode control register define the mode and the way that the carrier frequency generated by the frequency divider is selected in order to meet the transponder resonance frequency as good as possible.

Mode control register: 7-bit register

START_BIT	BIT 0	START_BIT=0	THE START BIT IS ALWAYS LOW AND DOES NOT NEED TO BE
reset=0			stored
DATA_BIT1	Bit 1	BIT4...1=0000	Microcontroller selects division factor 119
reset=0		BIT4...1=1111	Division factor is adapted automatically
DATA_BIT2	Bit 2	BIT4...1=0001	Microcontroller selects division factor 114
reset=0		BIT4...1=0010	Microcontroller selects division factor 115
DATA_BIT3	Bit 3	...	...
reset=0		BIT4...1=0110	Microcontroller selects division factor 119
DATA_BIT4	Bit 4	...	...
reset=0		BIT4...1=1011	Microcontroller selects division factor 124
SCI_SYNC	Bit 5	SCI_SYNC=0	Asynchronous data transmission to the μC
reset=0		SCI_SYNC=1	Synchronous data transmission to the μC
RX_AFC	Bit 6	RX_AFC=0	Demodulator threshold is adapted automatically
reset=0		RX_AFC=1	Demodulator threshold is defined by BIT4...1
TEST_BIT	Bit 7	TEST_BIT=0	No further test bytes
reset=0		TEST_BIT=1	Further test byte follows for special test modes

The first 4 bits in high state enable the base station to adjust the carrier frequency to the transponder resonance frequency automatically by giving the counter state of the transponder resonance-frequency measurement directly to the frequency divider. The other combinations of the first 4 bits allow the microcontroller to select the default carrier frequency or to use another frequency. The division factor can be selected to be between 114 and 124.

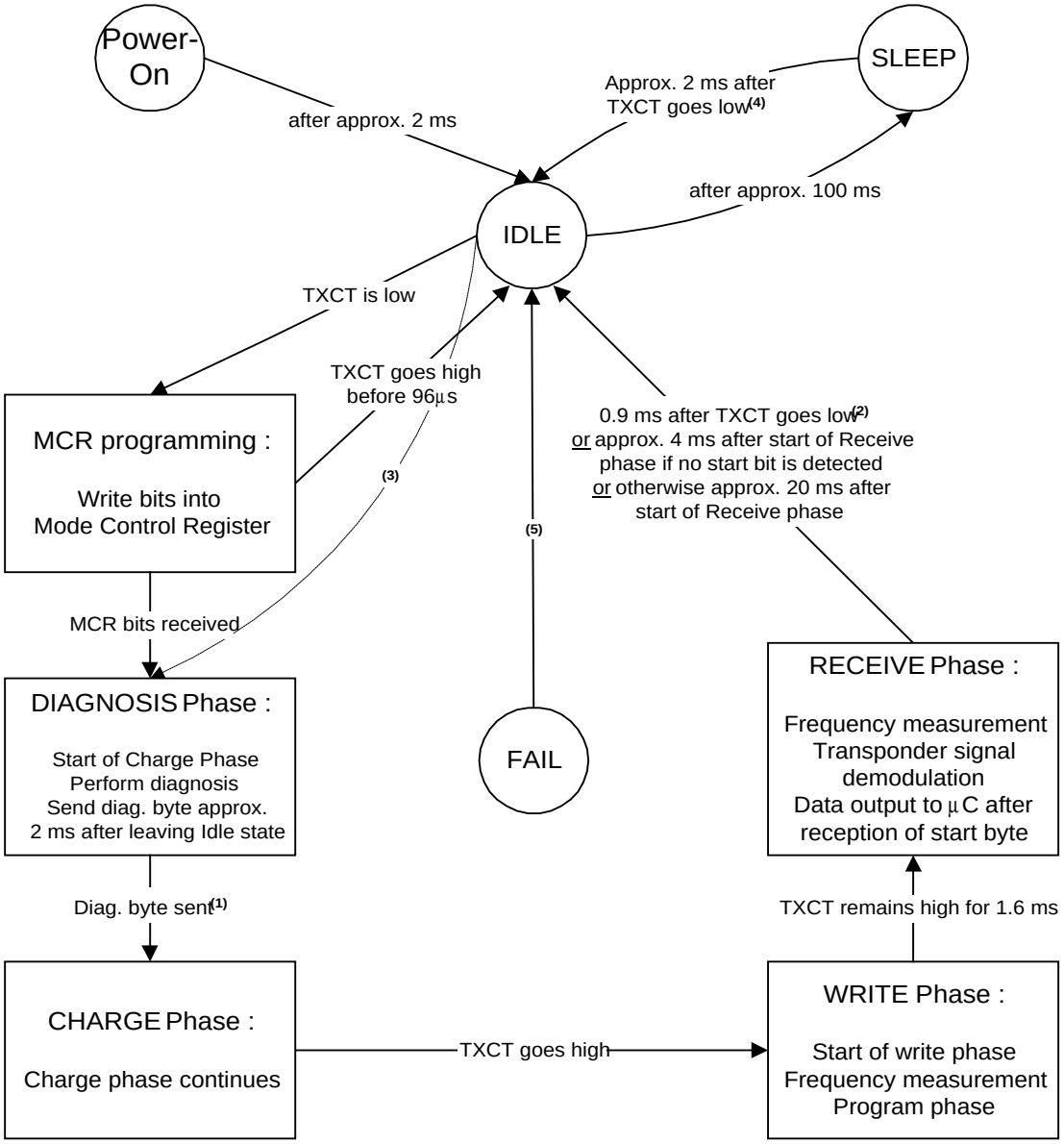
Some bits for testability reasons can be added. The default value of these test bits for normal operation is Low. Especially the bit 7 called TEST_BIT is Low for normal operation; otherwise the base station may enter one of the test modes.

The control logic also controls the demodulator, the SCI encoder, the diagnosis, and especially the transmission of the diagnosis byte during the charge phase.

The state diagram in figure 1 shows the general behavior of the state machine (note that the state blocks drawn can contain more than one state). All given times are measured from the moment when the state is entered if not specified otherwise.

Test Pins

The IC has an analog test pin A_TST for the analog part of the receiver. For the output of digital signals (for testing the state machine and to make register contents visible at the outside), the digital test output D_TST is used. In all operation modes, the internal reset signal of the digital blocks (active low) is output at the D_TST pin.



Notes :

(1) In SCI synchronous mode, this transition always occurs approx. 3 ms after leaving Idle state (diag. byte transmiss should be completed before).

(2) A falling edge on TXCT interrupts the Receive phase after a delay of 0.9 ms. TXCT must remain low for at least 1 µs. If TXCT is still low after the 0.9 ms delay, the basestation will go to Idle and directly to the Diagnosis phase one c cycle later (Dotted line(3)). No MCR can be written, only default mode is fully supported in this case.
Otherwise, if TXCT returns to high and remains high during the delay, the basestation will stay in Idle and wait for TX to go low (this will start properly a new MCR programming) or wait for 100 ms to go to Sleep.

(3) This transition only occurs in a special case (see note (2))

(4) A falling edge on TXCT interrupts the Sleep state. Only default mode is fully supported when starting an operation from Sleep with only one falling edge on TXCT (because of the 2 ms delay). For a proper MCR programming, TXCT to return to high and remain high during this delay.

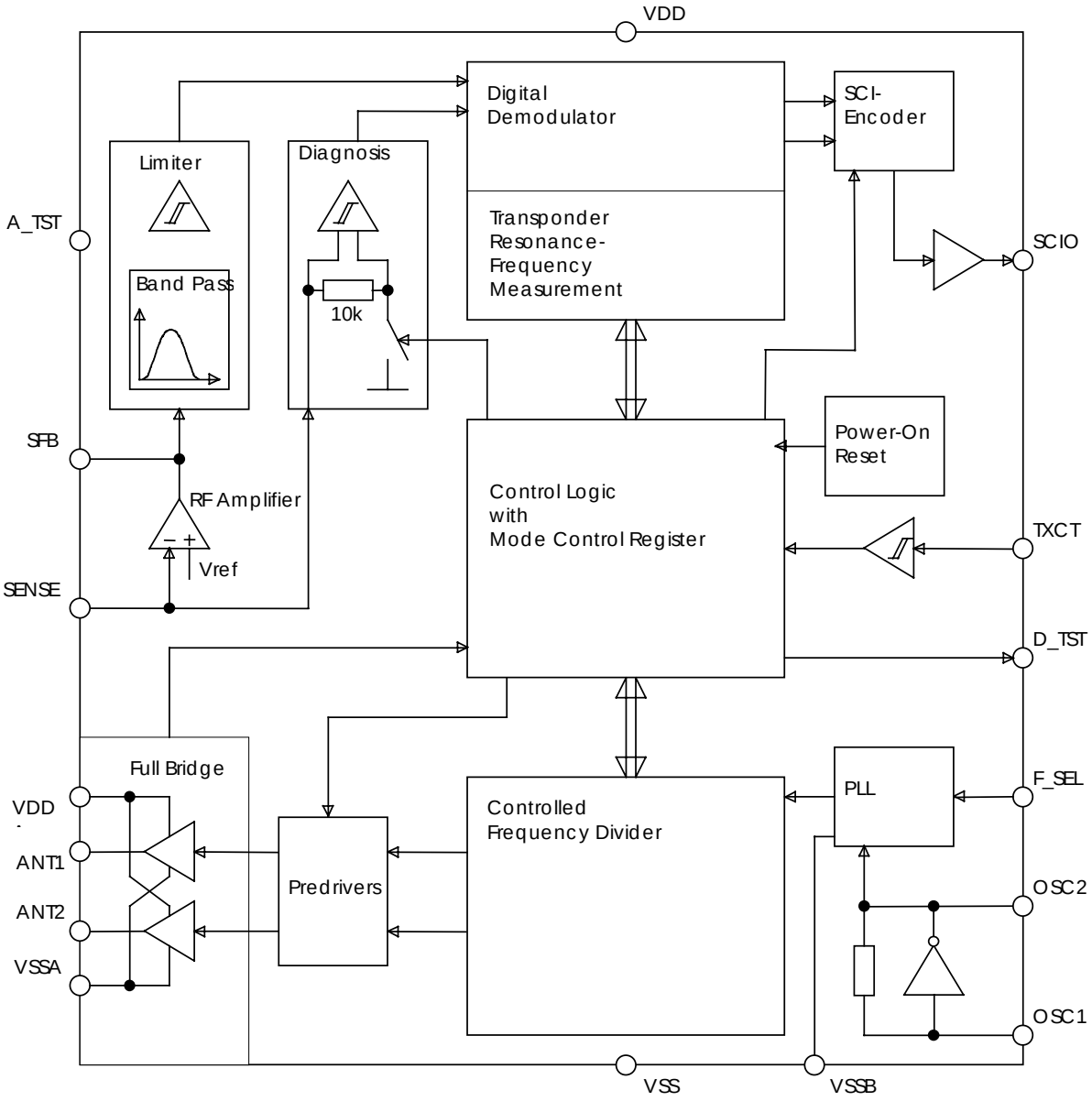
(5) Idle mode is the next state in case of undefined sataes ('fail safe state machine')

Figure 1: Operational State Diagram for the Control Logic

Pin Names and Functions

PIN	NAME	SIGNAL TYPE	FUNCTION
1	SENSE	analog input	Input of the RF amplifier
2	SFB	analog output	Output of the RF amplifier
3	D_TST	digital output	Test output for digital signals
4	A_TST	analog output	Test output for analog signals
5	ANT1	driver output	Antenna output 1
6	VSSA	supply input	Ground for the full bridge drivers
7	ANT2	driver output	Antenna output 2
8	VDDA	supply input	Voltage supply for the full bridge drivers
9	VDD	supply input	Voltage supply for non-power blocks
10	OSC2	analog output	Oscillator output
11	OSC1	analog input	Oscillator input
12	VSS	supply input	Ground for non-power blocks
13	VSSB	supply input	Ground for PLL
14	SCIO	digital output	Data output to the µC
15	F_SEL	digital input	Control input for frequency selection (default value is high)
16	TXCT	digital input	Control input from the µC (default value is high)

Block Diagram



Maximum Ratings

NAME	SYMBOL	COMMENT	MIN.	MAX.	UNIT
Power Supply (VDD, VSS, VSSB, VDDA, VSSA)					
Supply Voltage	Vdd		-0.3	7	V
Oscillator (OSC1, OSC2)					
Voltage Range	Vosc		-0.3	Vdd+0.3	V
Logic Inputs and Outputs (SCIO, TXCT, F_SEL, D_TST)					
Voltage Range	V inout		-0.3	Vdd+0.3	V
Overload Clamping Current	I inout		-5	5	mA
Full-Bridge Outputs (ANT1, ANT2)		Protection against voltage peaks and short-circuits (in accordance to application)			
Output Voltage	Vant		-0.3	Vdd+0.3	V
Output Peak Current	Iant		-1.1	1.1	A
Analog Pins (SENSE, SFB, A_TST)					
Voltage Range	Vanalog		-0.3	Vdd+0.3	V
SENSE Input Current	Isense		-5	5	mA
SFB Input Current in Case of Overvoltage	Isfb		-5	5	mA
Power Dissipation					
Operating Ambient Temperature	Tamb		-40	+85	°C
Storage Temperature Range	Tsto		-55	+150	°C
Thermal Resistance Junction to Air	Rth_ja			130	K/W
Total Power Dissipation at Tamb = +85°C	Pd			0.5	W
ESD Protection (MIL STD 883)	VESD		-2000	2000	V

Characteristics

Temperature: Tamb = -40°C to +85°C
Supply Voltage: Vdd = 4.5 V to 5.5 V

PARAMETERS AND CONDITIONS	SYMBOL	NOTE	MIN.	TYP.	MAX.	UNIT
Power Supply (VDD, VSS, VSSB, VDDA, VSSA)						
Supply Voltage	Vdd		4.5	5	5.5	V
Supply Voltage	Vdda		4.5	5	5.5	V
Sum of Supply Currents in Charge Phase, without antenna load	Idd			8	20	mA
Sum of Supply Currents in Sleep Mode, without I/O currents	Isleep			0.015	0.2	mA
Oscillator (OSC1, OSC2)						
Oscillator Frequency	fosc	1)		4		MHz
Transconductance at fosc = 4 MHz, 0.5 V pp at OSC1	gosc		0.5	2	5	mA/V
Input Capacitance at OSC1	Cin	2)			10	pF
Output Capacitance at OSC2	Cout	2)			10	pF
Logic Inputs (TXCT, F_SEL, OSC1)						
Input High Voltage	Vih		0.7 Vdd			V
Input Low Voltage (TXCT, OSC1)	Vil				0.3 Vdd	V
Input Low Voltage (F_SEL)	Vil				0.2 Vdd	kΩ
Pull-up Resistor at TXCT	Rtxct		90		500	kΩ
Pull-up Resistor at F_SEL	Rf_sel		10		500	
Logic Outputs (SCIO, D_TST)						
Output High Voltage	Voh		0.8 Vdd			V
Output Current at Voh	Ioh		-1			mA
Output Low Voltage	Vol				0.2 Vdd	V
Output Current at Vol	Iol				1	mA

Note 1): Application data, no test required.
Note 2): Guaranteed by design.

Characteristics (continued)

Temperature: Tamb = -40°C to +85°C
Supply Voltage: Vdd = 4.5 V to 5.5 V
Oscillator Frequency: fosc = 4 MHz with F_SEL = high

PARAMETERS AND CONDITIONS	SYMBOL	NOTE	MIN.	TYP.	MAX.	UNIT
Full-Bridge Outputs (ANT1, ANT2)						
Sum of Drain-Source Resistances of Full-Bridge n- and p-Channel MOSFETs at driver current Iant = 50 mA	ΣRds_on			7	14	Ω
Duty Cycle of p-Channel MOSFETs of Full Bridge	ton/T		38	40	42	%
Symmetry of Pulse Widths for the p-Channel MOSFETs of Full Bridge	ton1/ton2		96		104.5	%
Threshold for Overcurrent Protection	Ioc		140		1100	mA
Switch-Off Time of Overcurrent Protection (in case of short to ground with 3 Ω)	toc		0.25		10	µs
Delay for Switching on the Full Bridge after an Overcurrent	tdoc		2	2.05	2.1	ms
Leakage current (ANT1 / ANT2)	I leak				1	µA
Analog Part (SENSE, SFB, A_TST)						
Input Current Range at SENSE in Charge Phase	Isense	1)	-2		2	MA
DC Reference Voltage of RF Amplifier, related to Vdd	Vdc_rf/Vdd		9.25	10	11.0	%
Gain-Bandwidth Product of RF Amplifier, at 500 kHz with external components to achieve a voltage gain of min. 4 and 5 mV pp input signal	fg_bw		2			MHz

Note 1): Application data, no test required.

Characteristics (continued)

Temperature: Tamb = -40°C up to +85°C
Supply Voltage: Vdd = 4.5 V up to 5.5 V
Oscillator Frequency: fosc = 4 MHz with F_SEL = high

PARAMETERS AND CONDITIONS	SYMBOL	NOTE	MIN.	TYP.	MAX.	UNIT
Phase Shift of RF Amplifier, at 134 kHz with external components to achieve a voltage gain of 5 and 20 mV pp input signal	φo				16	°
Peak-to-Peak Input Voltage of Band Pass at which the limiter comparator should toggle, at 134 kHz (corresponds to a minimal total gain of 1000)	Vsfb	11)	5			mV
Lower Cut-Off Frequency of Band-Pass Filter	f low	12)	24	60	100	kHz
Higher Cut-Off Frequency of Band-Pass Filter	f high	12)	160	270	540	kHz
Hysteresis of Limiter, A_TST pin used as input, resp. D_TST pin as output, offset level determined by bandpass stage	ΔVhyst		25	50	135	mV
Diagnosis (SENSE)						
Current Threshold for Operating Antenna	Idiag	3)	80		240	μA

Note 3): Internal resistance switched on and much lower than external SENSE resistance.
Note 11): Guaranteed by design; functional test done for input voltage of 90 mV pp.
Note 12): BP filter tested @ 3 different frequencies: fmid=134 kHz and gain > 30db; flow=24 kHz, fhigh=500 kHz and attenuation < -3dB (reference = measured gain @fmid=134kHz)

Characteristics (continued)

Temperature: Tamb = -40°C up to +85°C
Supply Voltage: Vdd = 4.5 V up to 5.5 V
Oscillator Frequency: fosc = 4 MHz with F_SEL = high (for pos. 8 and 9)

PARAMETERS AND CONDITIONS	SYMBOL	NOTE	MIN.	TYP.	MAX.	UNIT
Timing Requirements						
Time for TXCT high to initialize a new transmission, from start of the oscillator after power-on or waking up until reaching the idle mode	t init min	4)	2	2.05	2.2	ms
Delay between leaving idle mode and start of diagnosis byte at SCIO in normal operation	Tdiag	4)	2	2.14	2.2	Ms
Charge phase duration	tch	1),4)	15	50		ms
Delay between end of charge or end of program and start of transponder data Tx on SCIO	tR	1),4)		3		ms
Program phase duration	tprog	1),5)	15			ms
Write pulse on / High bit	tonH	1)		0.62		ms
Write pulse on / Low bit	tonL	1)		0.38		ms
Write pulse pause / High bit	toffH	1),7)	0.46	0.48	0.5	ms
Write pulse pause / Low bit	toffL	1),7)	0.1	0.12	0.14	ms
Write High bit duration	tbitH	1),7)		1		ms
Write Low bit duration	tbitL	1),7)		0.5		ms
Signal Delay on TXCT for controlling the full bridge in write mode	tdwrite		73	79	85	µs
NRZ bit duration for mode control register	tmcr	6)	121	128	135	µs
NRZ bit duration on SCIO in asynchronous mode	tsci	8)	63	64	65	µs
Low Signal Delay on TXCT to stop synchronous mode	tdstop		128		800	µs

Note 1): Application data, no test required.
Note 4): see Timing Diagrams, figures 1,2, and 3.
Note 5): see Timing Diagrams, figure 3.
Note 6): see Timing Diagrams, figure 4.
Note 7): see Timing Diagrams, figure 5.
Note 8): see Timing Diagrams, figure 6.

Characteristics (continued)

Temperature: Tamb = -40°C up to +85°C
Supply Voltage: Vdd = 4.5 V up to 5.5 V
Oscillator Frequency: fosc = 4 MHz with F_SEL = high

PARAMETERS AND CONDITIONS	SYMBOL	NOTE	MIN.	TYP.	MAX.	UNIT
Timing Requirements (cont'd)						
Total TXCT time for reading data on SCIO in synchronous mode	tt_sync	1),10)			900	µs
TXCT period for shifting data on SCIO in synchronous mode	tsync	10)	4	64	100	µs
Low phase on TXCT in synchronous mode	tL_sync	10)	2	32	tsync-2	µs
Phase-Locked Loop (D_TST)						
PLL Frequency	fpll		15.984	16	16.016	MHz
Jitter of the PLL Frequency	Δf/fpll				6	%
Power-on Reset (POR)						
POR threshold voltage, Vdd rising with low slope	Vpor_r		1.9		2.6	V
POR threshold voltage, Vdd falling with low slope	Vpor_f		1.3		2.6	V

Note 1): Application data, no test required.
Note 10): see Timing Diagrams, figure 7.

Timing Diagrams

Protocol on TXCT pin

DEFAULT mode (read-only, no writing into mode control register):

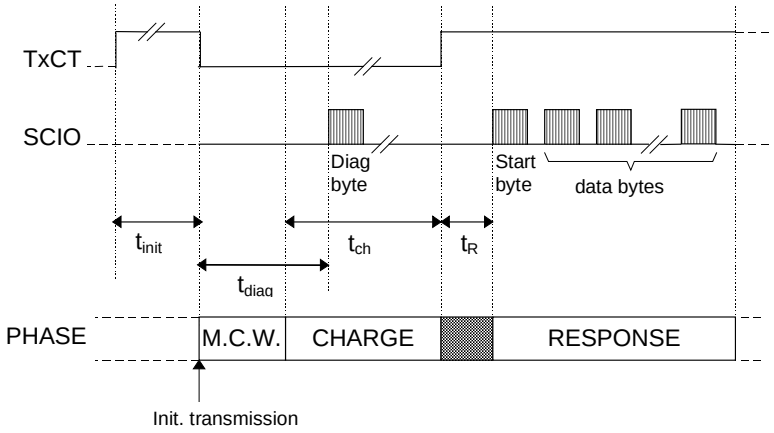
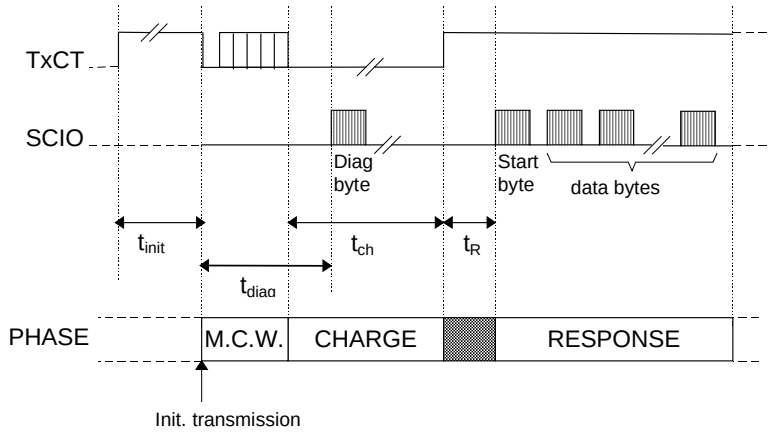


Figure 1: Default Mode

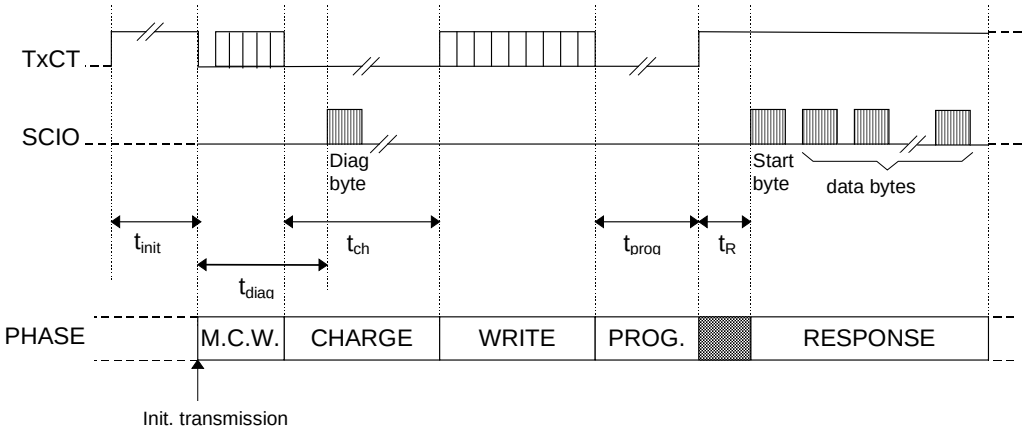
READ-ONLY mode with writing into mode control register:



M. C. W.: Mode Control Write (to write into the mode control register)

Figure 2: Read-Only Mode

WRITE/READ mode with writing into mode control register:



M. C. W.: Mode Control Write (to write into the mode control register)

PROG.: Program Phase of Transponder

Figure 3: Write/Read Mode

MODE CONTROL WRITE protocol (NRZ coding)

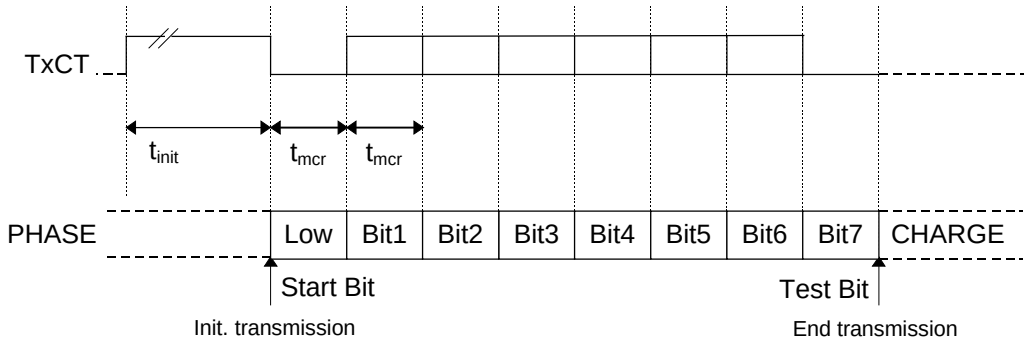


Figure 4: Mode Control Write Protocol

TRANSPONDER WRITE protocol:

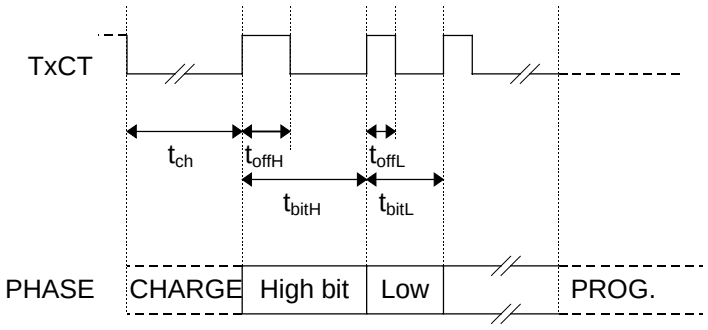


Figure 5: Transponder Write Protocol

4.7.2 Transmission on SCIO Pin (NRZ coding)

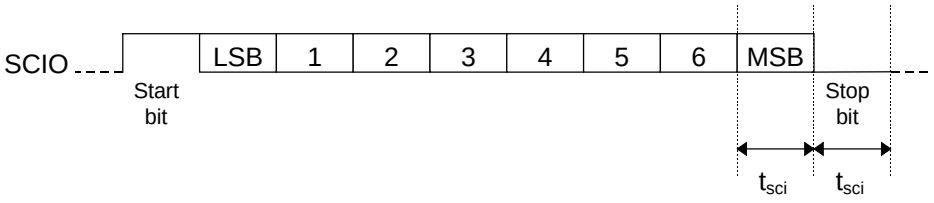


Figure 6: Transmission on SCIO Pin in Asynchronous Mode

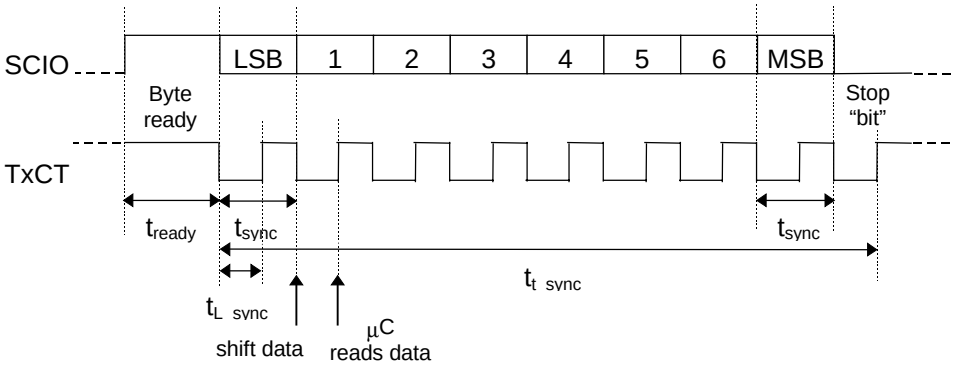


Figure 7: Transmission on SCIO Pin in Synchronous Mode
(for diagnosis byte and data bytes)

Application diagram