

# AFE7070 Dual clock settings

**AFE7070 GUI v2p5.vi**  
**TEXAS INSTRUMENTS**  
**AFE7070 EVM Software Control**  
Version 2.5

AFE7070 CDCM7005 [Reset USB Port] [Exit]

**Power Control**

- Sleep  Awake
- Power Down Fuses  Powered
- Power Down Clock Receiver  Powered
- LVDS Power Down  Powered
- RF Out Power Down  Powered
- DAC Power Down  Powered
- Analog Out Power Down  Powered
- Pwr Dn Clock Receiver on SLEEP  No
- LVDS Pwr Dn when SLEEP  No
- RF out Pwr Dn when SLEEP  No
- DAC Pwr Dn when SLEEP  No
- Analog out Pwr Dn when SLEEP  No

**FIFO Settings**

- FIFO Enable  Disabled
- FIFO Offset: -4 -2 0 2 3
- Mask 2-Away Alarm  Not masked
- Mask 1-Away Alarm  Not masked
- Enable 2-Away Alarm  Enabled
- Enable 1-Away Alarm  Enabled
- Mask FIFO Sync  Not masked
- FIFO 2 away
- FIFO 1 away

**QMC Settings**

- QMC Corr Enable  Disabled
- QMC Offset Enable  Disabled
- QMC Offset A: -2560
- QMC Offset B: -646
- QMC Gain A: 1349
- QMC Gain B: 538
- QMC Phase: -490

**Analog Output Settings**

- TX Enable  TX enabled
- DAC A Complement  Not complemented
- DAC B Complement  Not complemented
- DAC Current Control: 15
- Trim Analog Filters: 0

**Digital Input Settings**

- Binary Rep  2's comp
- IQ Swap  Swapped
- Data Type  IQ

**Mixer/NCO Settings**

- Mixer Enable  Bypassed
- Mixer Gain  x1
- Fdac (MHz): 500
- Frequency [MHz]: 0.016354
- NCO: 140486
- Phase: 0

**SYNC Settings**

- SYNC bit: 0
- Sync on I or Q: I
- Sync / Sleep / TX Enable Selection: All controlled by SIF bit

**Clock Settings**

- Clock Mode: Dual Output Clock
- Trim CLK RC Filter: 0 1 2 3

**Misc. Digital Signals**

- Enable 4-pin SIF  4-pin mode disabled
- ALARM\_SDO Enable  Disabled
- Output MSB on ALARM  No

**AFE7070 Register Data**

x00	xC0	1100 0000
x01	xC2	1100 0010
x02	xFF	1111 1111
x03	x10	0001 0000
x04	x0F	0000 1111
x05	x00	0000 0000
x06	x00	0000 0000
x07	x13	0001 0011
x08	x00	0000 0000
x09	x7A	0111 1010
x0A	xB6	1011 0110
x0B	xEA	1110 1010
x0C	x45	0100 0101
x0D	x1A	0001 1010
x0E	x16	0001 0110
x0F	xAA	1010 1010
x10	xC6	1100 0110
x11	x24	0010 0100
x12	x02	0000 0010
x13	x00	0000 0000
x14	x00	0000 0000
x15	x00	0000 0000
x16	x00	0000 0000
x17	x00	0000 0000
x18	x00	0000 0000

**CDCM7005 Register Data**

Reg	Value
00	0x005FF1F0
01	0x0282AAA1
02	0xD00000A2
03	0x00000027

**Register Controls**

- Send All
- Read All
- Load Regs
- Save All Regs
- Save AFE Regs
- Save CDC Regs

LVDS Clock Divider: /4

# AFE7070 Dual Clock CDCM settings

The screenshot displays the AFE7070 EVM Software Control GUI, Version 2.5, with the CDCM7005 tab selected. The interface is divided into several sections for configuring the CDCM7005 Operation in Buffer Mode.

**Advanced Options:**

- Progr. Delay M: 0ps
- Progr. Delay N: 0ps
- Lock Detect Cycle: 64
- Lock Window: ±8ns
- Fast Lock: mode off
- Charge Pump: 2.0mA
- PFD Pulse: +1.5ns
- Lock: Digital
- Ref. Clk: Manual
- Ref. Detection: Off
- Status\_Ref: FRE\_DET\_REF
- Status\_VCXO: FRE\_DET\_VCXO
- CP Direction: positive
- Reset (Off)/Hold (On):
- Power Dwn Mode:
- Frequency Hold-Over Fcn:
- Cycle Slip Mode:
- Preset CP to Vcc/2:
- Frequency Hold-Over Fcn1:
- Reset all Dividers:
- CP 3-State:
- Hold Fcn always activated:

**Clock & PLL Options:**

- Clock Settings: M & N Selection: Auto, Ref. Freq (MHz): 10, VCXO Freq (MHz): 983.04
- PLL Settings: M Divider: 125, N Divider: 1536, FB\_MUX: 1, Phase Shift: /16
- PLL Output: Output Freq (MHz): 983.04

**Output Options:**

- Y0 Output (Unused): 1, 3-state, LVCMOS
- Y1 Output (AFE7070's CLK\_IO): 1, 3-state, LVCMOS
- Y2 Output (Unused): 1, 3-state, LVCMOS
- Y3 Output (AFE7070's DACCLK): 1, active, LVPECL
- Y4 Output (CDC OUT): 1, 3-state, LVCMOS

**AFE7070 Register Data:**

Reg	Value
x00	x00 1100 0000
x01	x02 1100 0010
x02	xFF 1111 1111
x03	x10 0001 0000
x04	x0F 0000 1111
x05	x00 0000 0000
x06	x00 0000 0000
x07	x13 0001 0011
x08	x00 0000 0000
x09	x7A 0111 1010
x0A	x86 1011 0110
x0B	xEA 1110 1010
x0C	x45 0100 0101
x0D	x1A 0001 1010
x0E	x16 0001 0110
x0F	xAA 1010 1010
x10	xC6 1100 0110
x11	x24 0010 0100
x12	x02 0000 0010
x13	x00 0000 0000
x14	x00 0000 0000
x15	x00 0000 0000
x16	x00 0000 0000
x17	x00 0000 0000
x18	x00 0000 0000
x19	x00 0000 0000
x1A	x00 0000 0000
x1B	x00 0000 0000
x1C	x00 0000 0000
x1D	x00 0000 0000
x1E	x00 0000 0000
x1F	x00 0000 0000

**CDCM7005 Register Data:**

Reg	Value
00	0x005FF1F0
01	0x0282AAA1
02	0xD00000A2
03	0x00000027

**Register Controls:**

- Send All:
- Read All:
- Load Regs:
- Save All Regs:
- Save AFE Regs:
- Save CDC Regs: