Maximizing GSPS ADC SFDR Performance: Sources of Spurs and Methods of Mitigation

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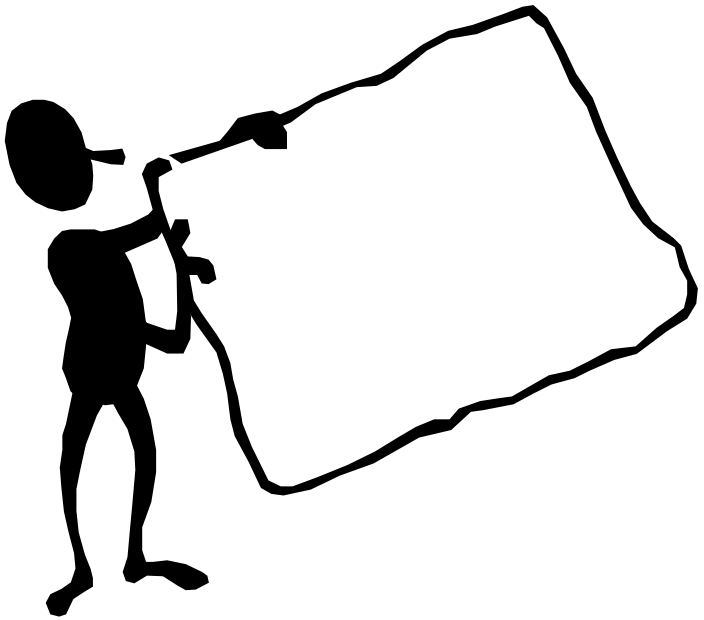
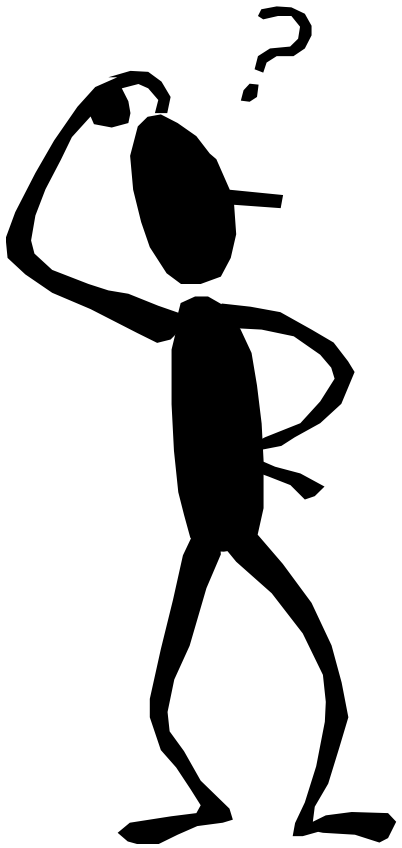
Outline



- Overview of the issue
- Sources of spurs
- Methods of mitigation
- Summary and recommendations

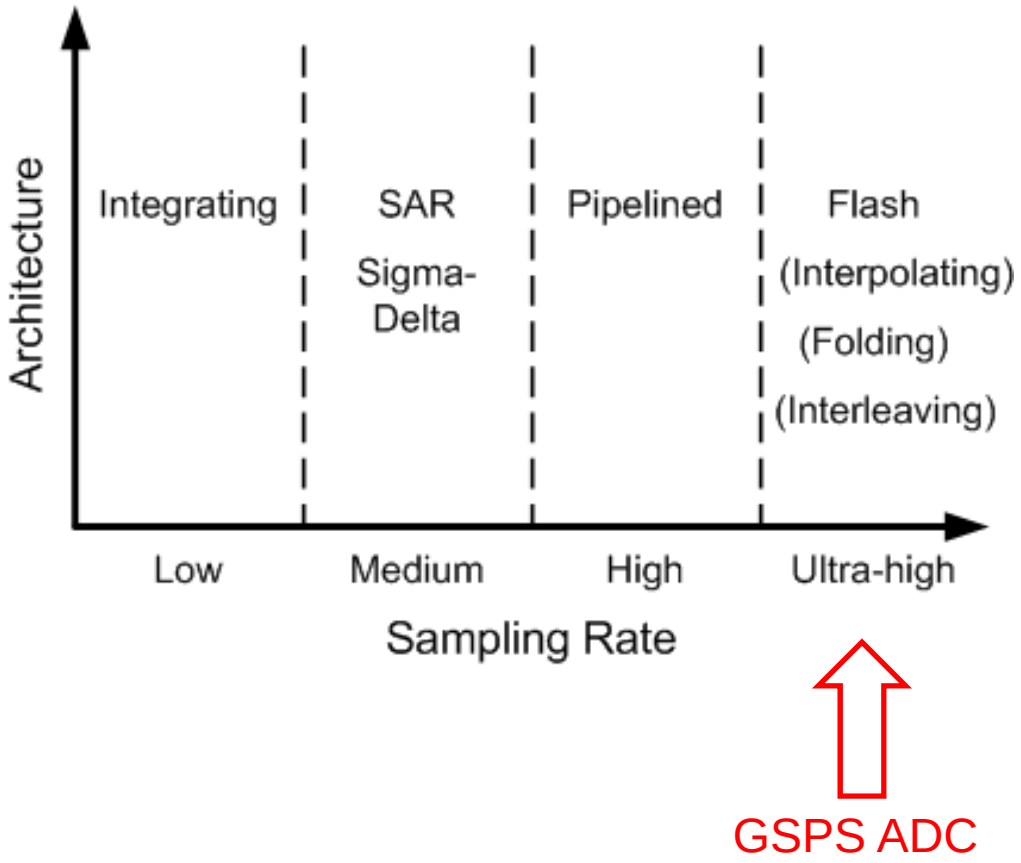
AN OVERVIEW OF THE ISSUE

Problem statement



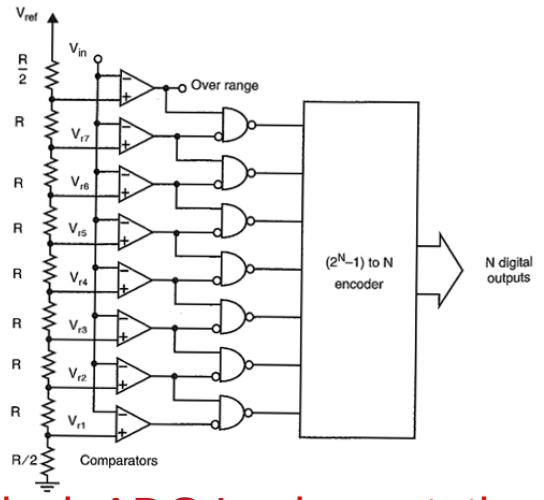
How to minimize spurs in the GSPS ADC family in order to maximize SFDR performance?

ADC Sampling Rate and Architecture

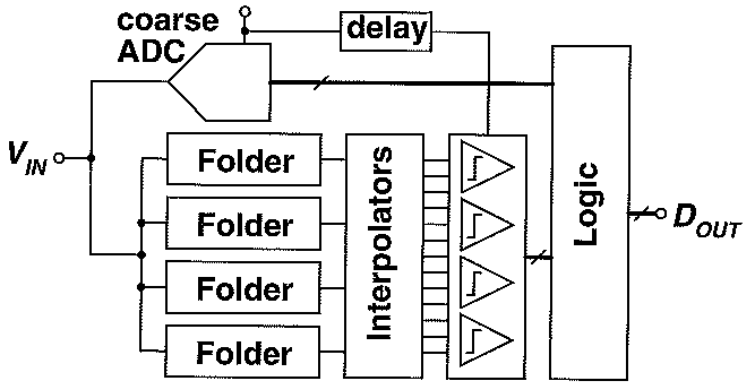


- The absolute rate of what “low” or “high” is, changes as process technology advances.
- Higher sampling rate architectures imply lower resolutions.
- Certain techniques may be applied to the basic flash architecture in order to improve its performance.

Ultra high-speed architecture design (2)



Flash ADC Implementation



Folding-Interpolating Architecture

- Basic Flash Architecture
  - Can achieve high sampling rates with low conversion latency
  - Basic design requires 2^N comparators and latches
  - Drawbacks are high power consumption, die area
- What techniques can make a 12-bit 3.6 GSPS ADC practically realizable?
  - Folding and interpolating to improve power consumption, reduce area

Diagrams are from “Analog Integrated Circuit Design” by Johns and Martin, 1997; “Circuit Techniques for Low-voltage and High-speed A/D Converters” by Waltari and Halonen, 2002.

GSPS ADC Functional Blocks

Block	Description	Pros	Cons
Track-and-hold	Track and hold analog input signal	Improve performance at low Fin	Can reduce max sampling rate
Folding	Fold transfer function into sub-ranges	Reduce number of latches to improve power, area	Introduces distortion
Interpolating	Interpolate conversion between series of amplifiers	Reduce number of amplifiers to improve power, area	Introduces distortion
Interleaving	Time-interleave multiple ADC cores	Achieve higher sampling rates	Introduce distortion from mismatch factors
Calibrating	Trim bias currents in linear amplifiers	Reduces distortion	Time off-line to calibrate

For more details on the GSPS ADC architecture, see “A 1.8V 1.0Gsps 10b Self-Calibrating Unified-Folding-Interpolating ADC with 9.1 ENOB at Nyquist Frequency” by R. Taft, et al. ISSCC 2009 / Session 4 / High-speed Data Converters.

SOURCES OF SPURS

Harmonic Distortion in an Amplifier

- What are the harmonic distortion terms for an amplifier? First, let us consider the non-linear system:

$$v_o(t) = a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^3(t) + a_4 v_{in}^4(t) + a_5 v_{in}^5(t) + \ldots$$

- For differential circuits, the even harmonics are ideally zero and $H_3 >> H_5$, so we can approximate:

$$v_o(t) \cong a_1 v_{in}(t) + a_3 v_{in}^3(t)$$

- For a sinusoidal input: $v_{in}(t) = A\cos(\omega t)$

$$v_o(t) = a_1 A\cos(\omega t) + a_3 A^3 \cos^3(\omega t)$$

$$= [\underbrace{a_1 A + \frac{3a^3A^3}{4}}_{HD_1}]\cos(\omega t) + [\underbrace{\frac{a^3A^3}{4}}_{HD_3}]\cos(3\omega t)$$

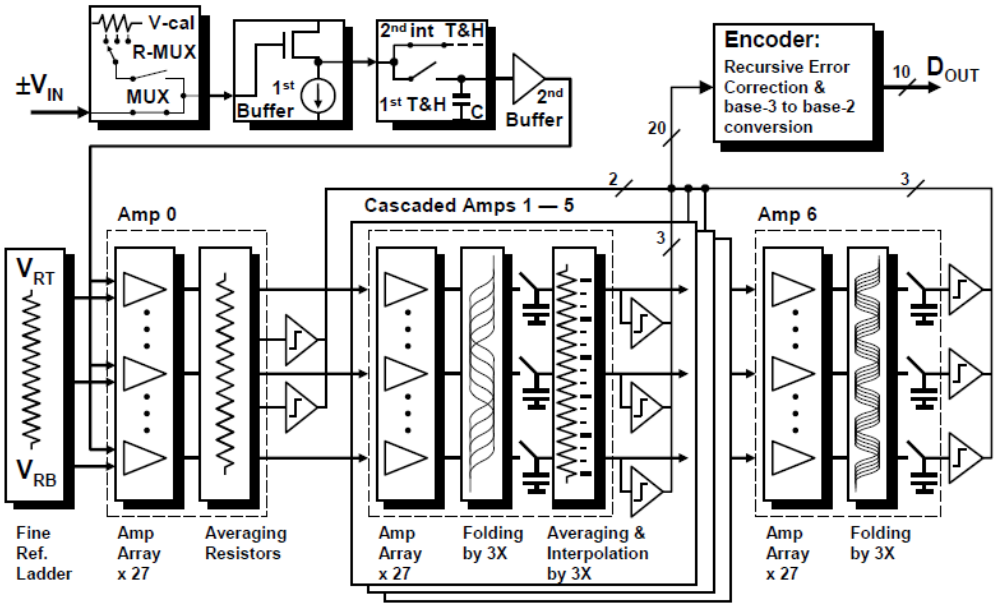
- If we define: $v_o(t) \equiv HD_1\cos(\omega t) + HD_3\cos(3\omega t)$

$$HD_1 = a_1 A \quad \text{and} \quad HD_3 = \frac{a_3 A^3}{4}$$

Example:

For a classic non-linear amplifier, if the input level, A, is decreased by 1dB, then HD_3 decreases by 3dB since HD_1 is proportional to A and HD_3 is proportional to A^3.

Harmonic Distortion due to Non-Linearity



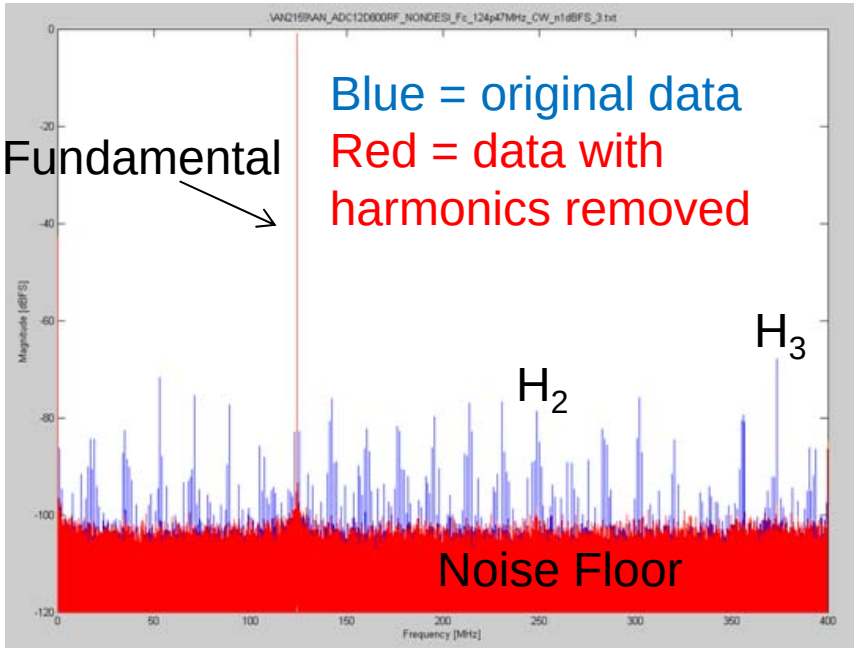
- Harmonic distortion contribution from all sources sum at ADC output
- Distortion location is easy to predict, but amplitude is not

Source of Distortion	Harmonics Produced	Rolls off with	Relationship to input power
Track-and-hold	Lower order harmonics	Analog input bandwidth	Classic relationship
Amplifiers in interpolating, folding architecture	Higher order harmonics	Folding-interpolating factor	Non-linear relationship

E.g.: Harmonic Distortion

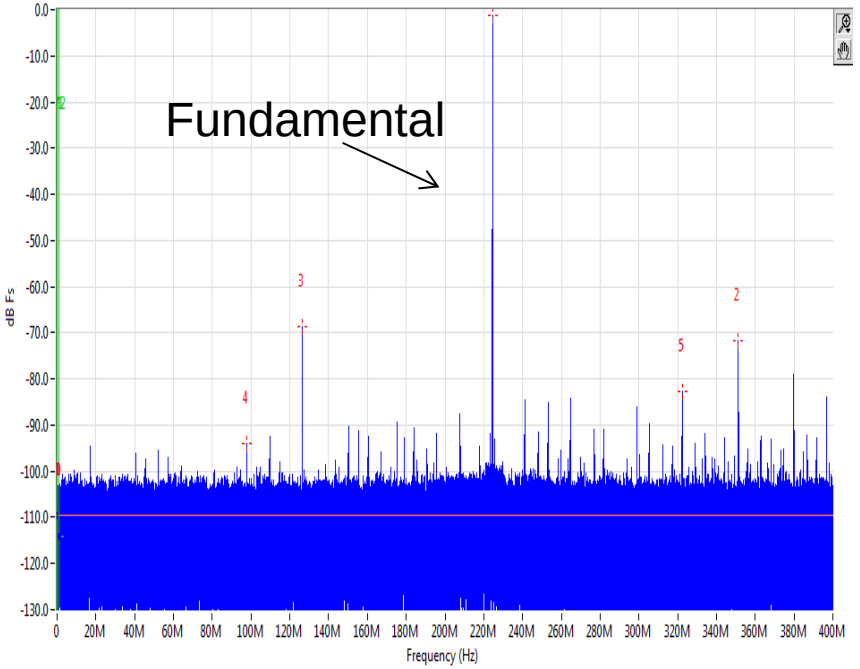
ADC12D800RF

(Folding-interpolating)

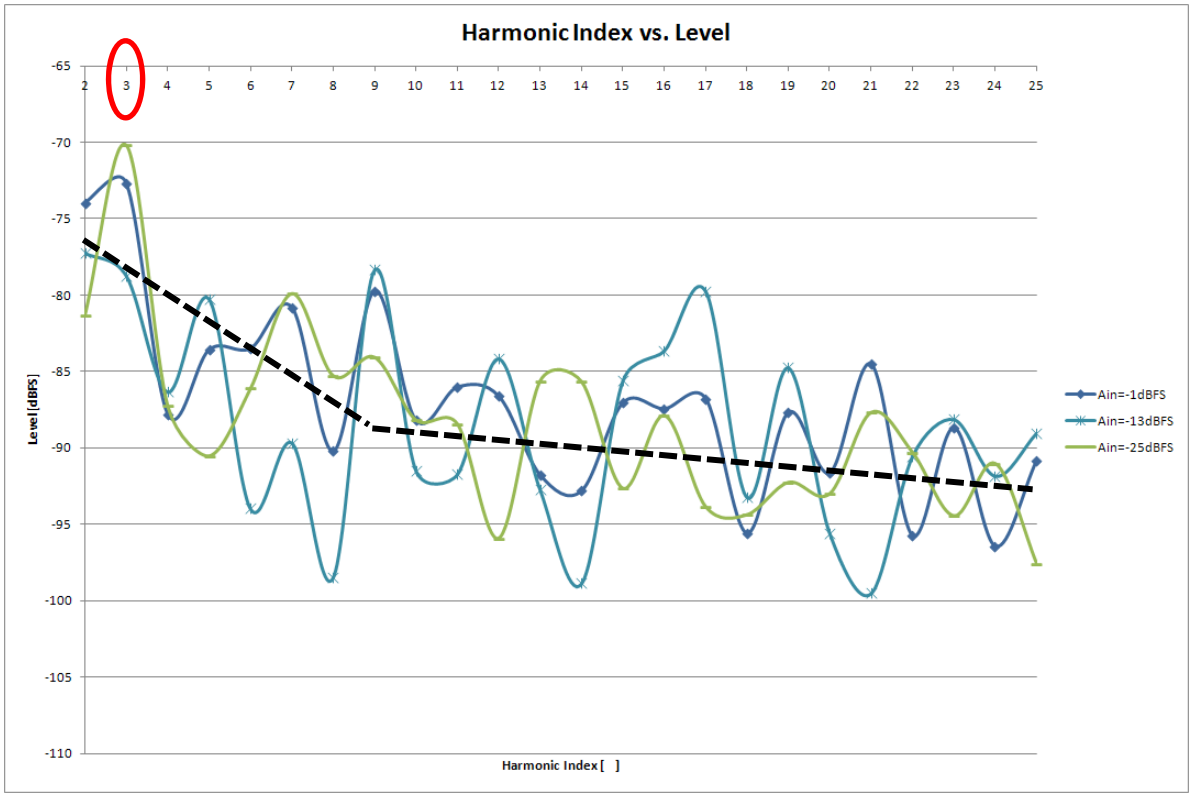


ADS5400

(Pipeline)



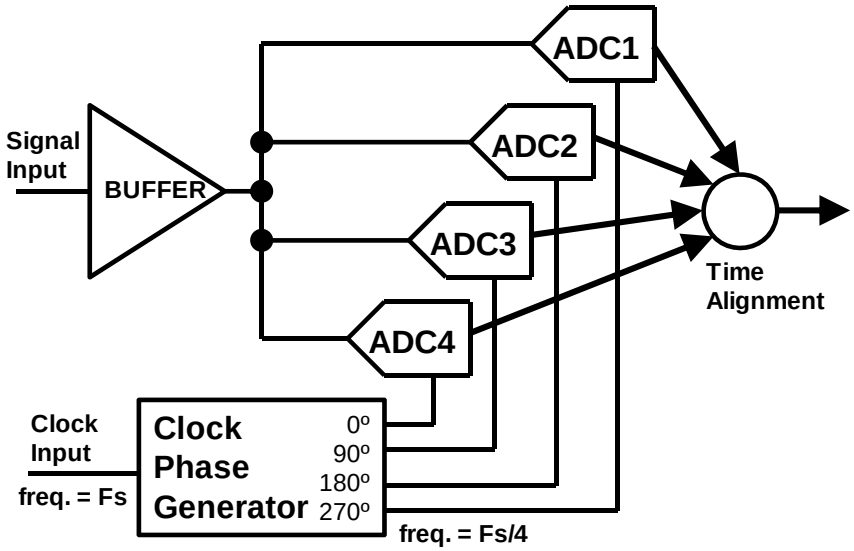
E.g.: ADC12D1600RF Harmonic Levels

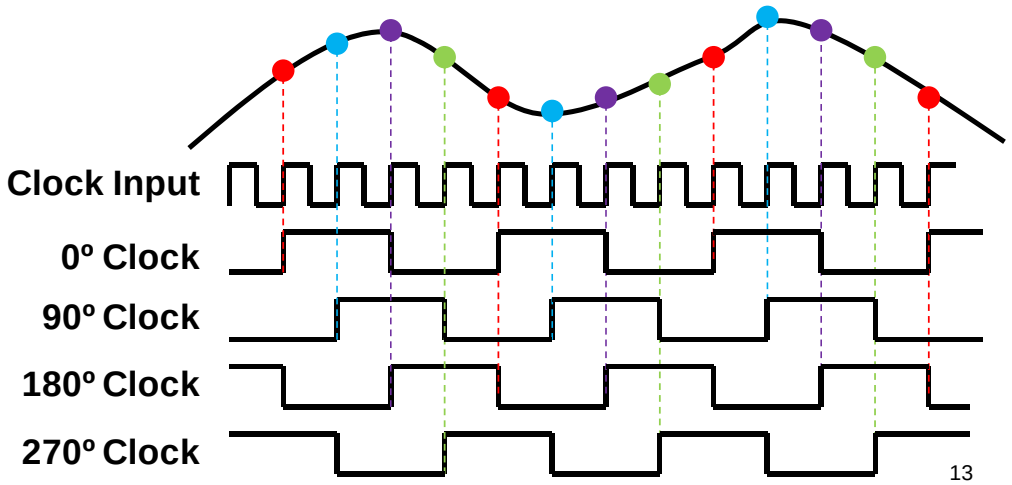


- H_3 is generally the highest level harmonic
- Lower index harmonics from the track-and-hold roll off with input bandwidth
- Higher index harmonics from the folding-interpolating architecture remain present and have highly non-linear level
- A reduction in the input level is not strongly related to the harmonics level

ADC Interleaving Basics

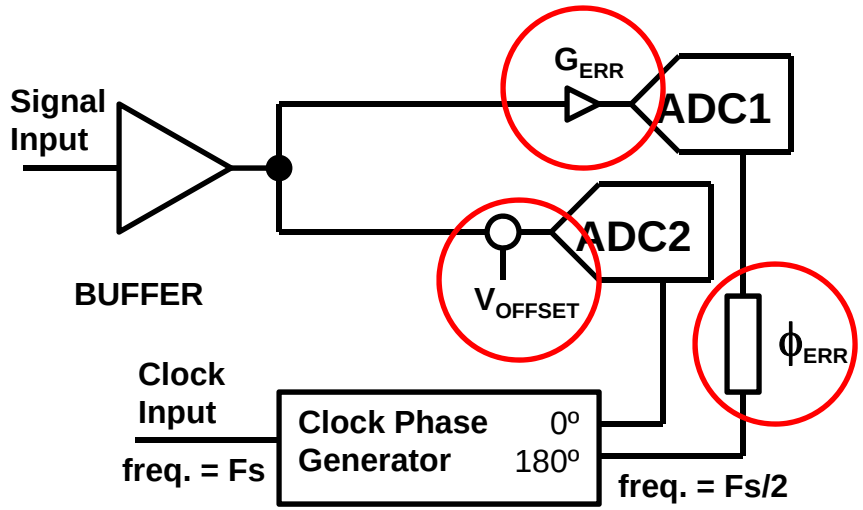
- Multiple ADC cores sample signal to increase total sampling rate
- ADC cores sample at same divided frequency but different phase offset
- Digital outputs are re-aligned in time
- Input buffer typically drives cores





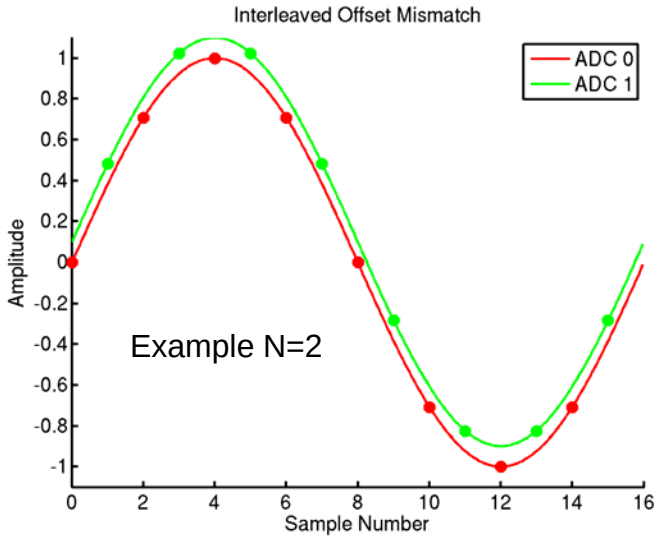
Non-Ideal Interleaving

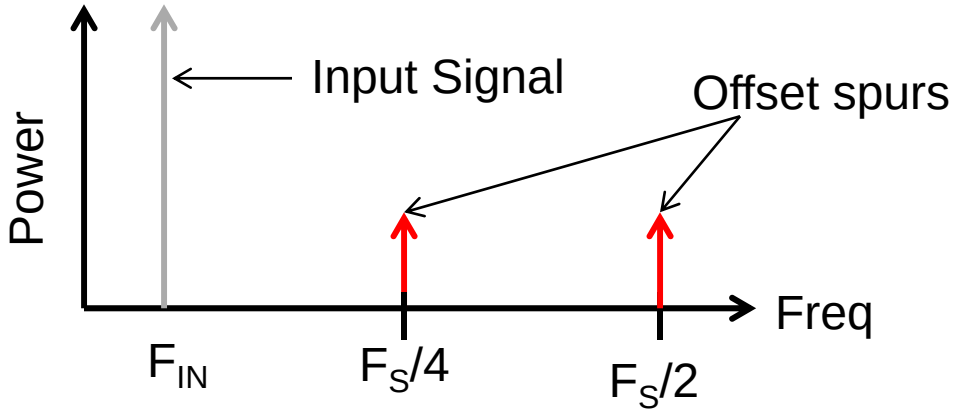
- Offset Errors
  - Mismatched ADC core voltage offset
- Amplitude Errors
  - ADC core gain error
  - ADC reference voltage error
- Phase Errors
  - Input routing delay
  - Input BW difference
  - Clock phase error
  - ADC sampling instant



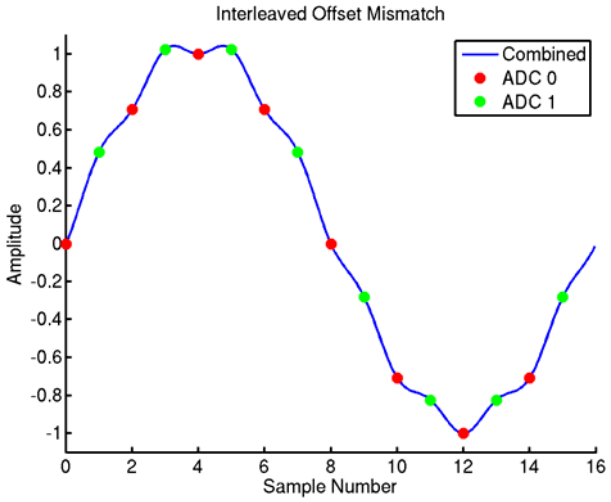
Non-Ideal Interleaving

- Offset Error
  - Different voltage offset at ADC input between different cores
- Alternating up/down in transient waveform
- Creates signal independent spurs in spectrum at Fs*n/N for n=1,2,…,N-1 where N is # of interleaved cores



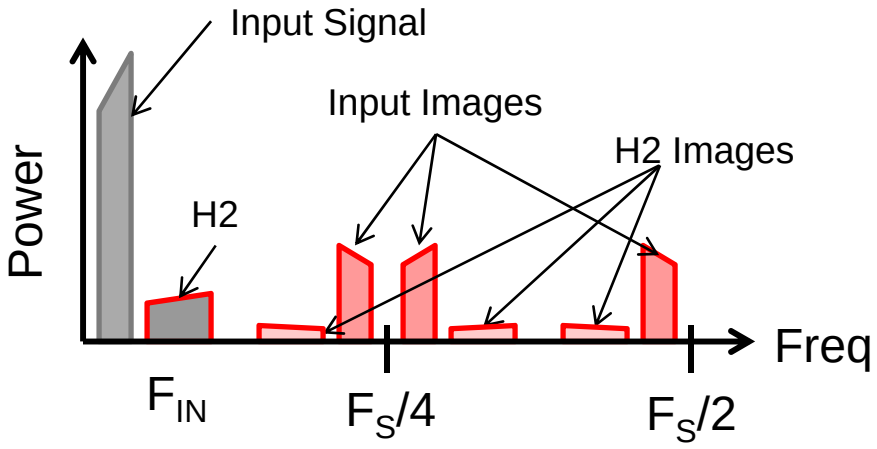


Example N=4

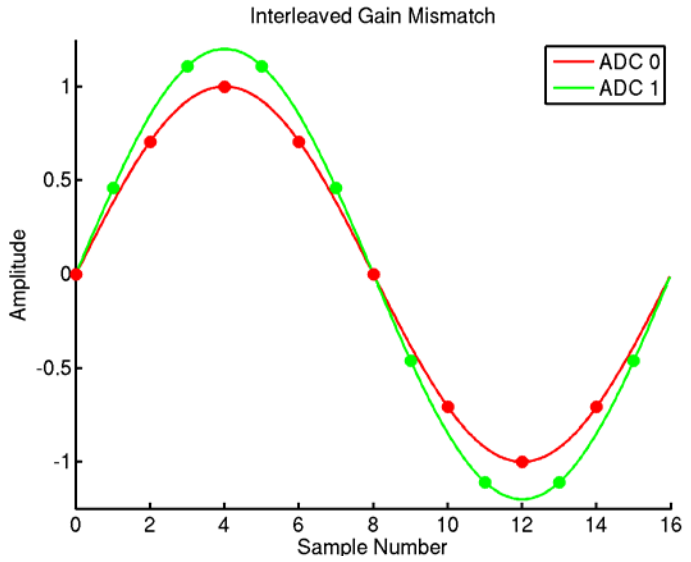


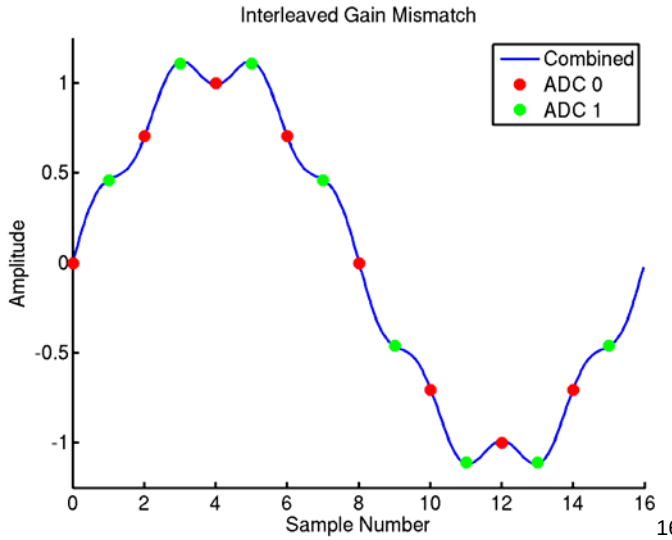
Non-Ideal Interleaving

- Amplitude and Phase errors
  - Gain difference between different cores
  - BW differences or transmission length differences result in phase difference
- Creates N-1 input signal dependent images from 0 to Fs/2 in a repetitive, mirror-image pattern where N is # of interleaved cores
- Also creates harmonic distortion images

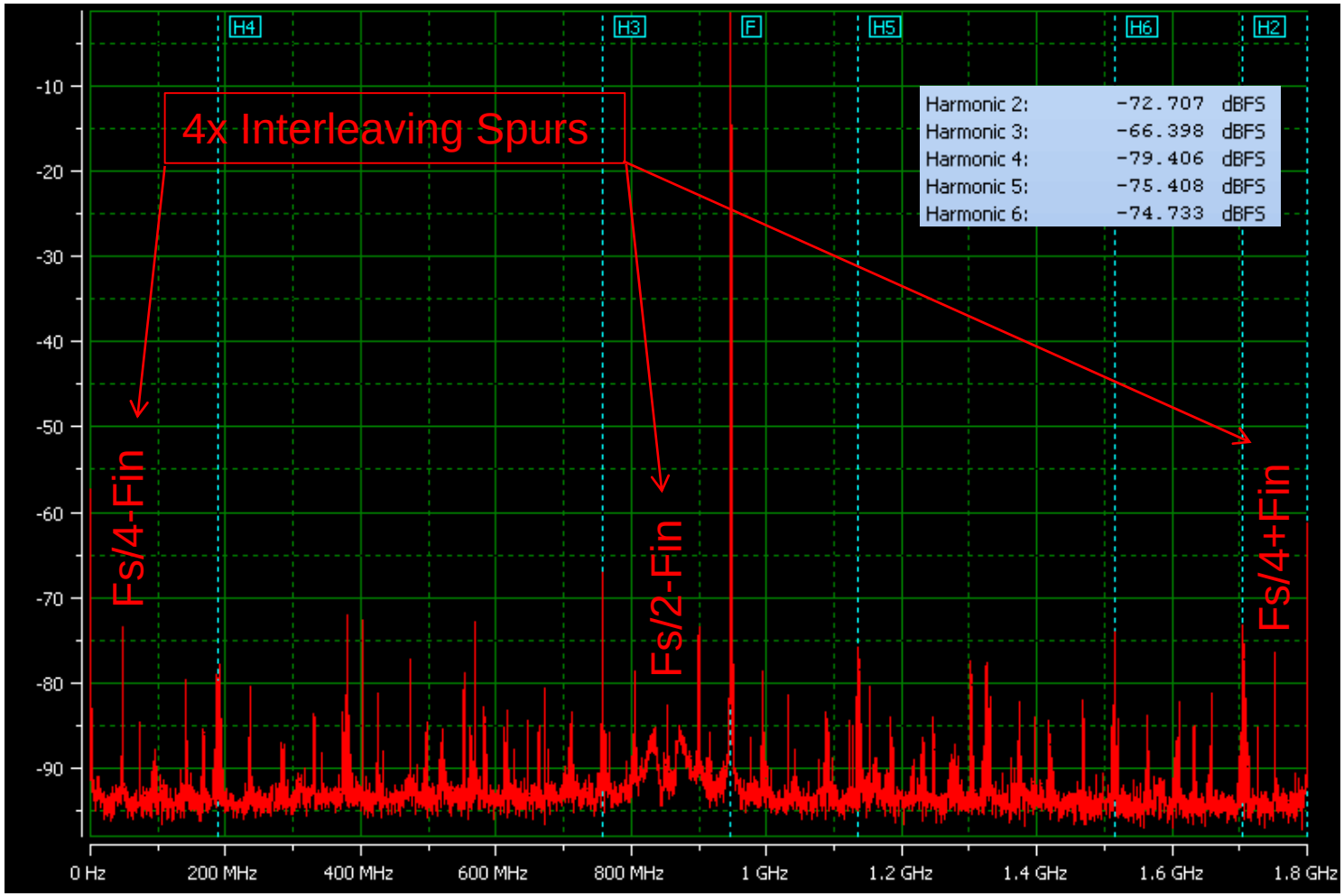


Example N=4





E.g.: ADC12D1800RF DES Mode Interleaving Spurs

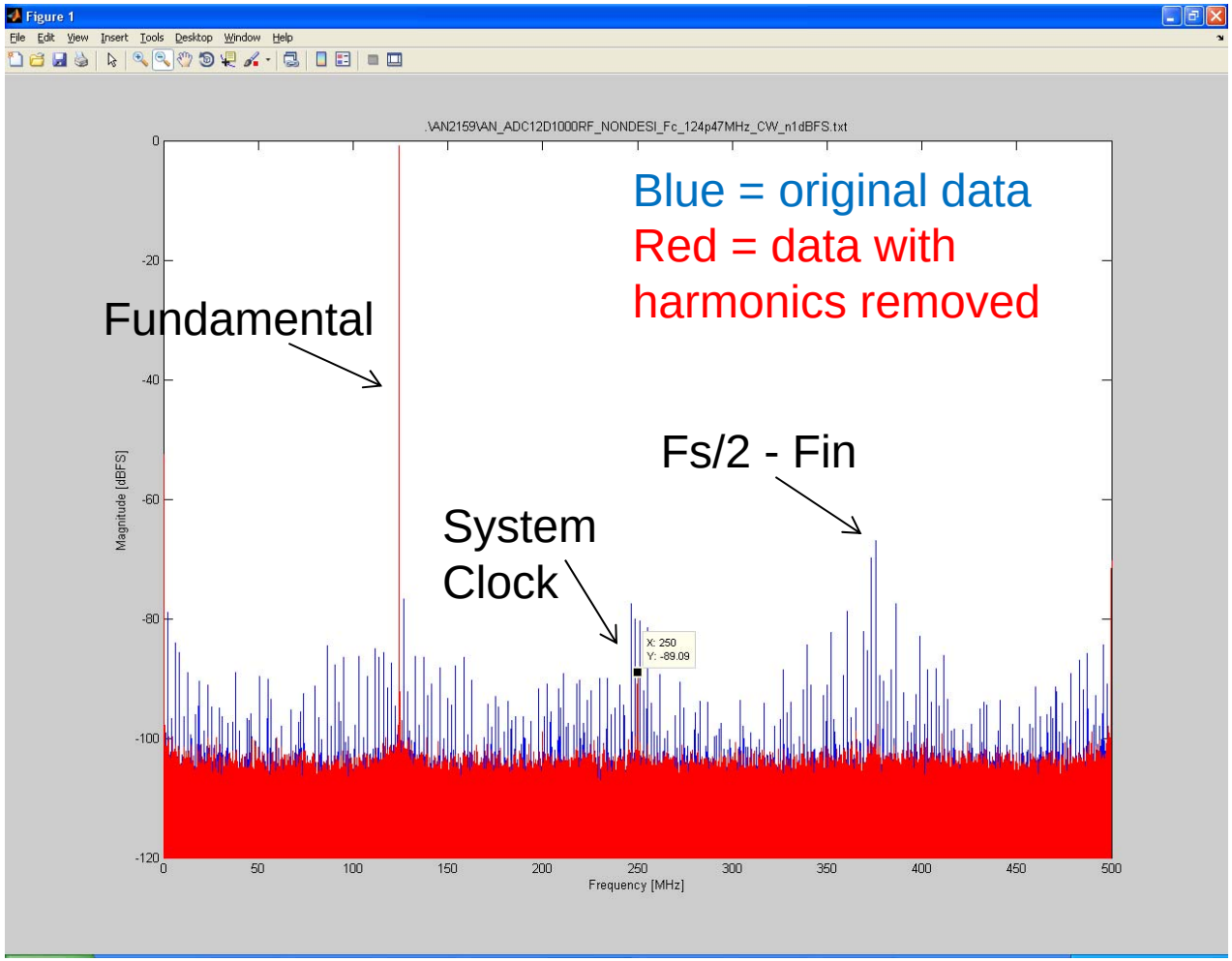


Interleaving by Product

Product	Number of sub-converters in Non-DES Mode	Number of sub-converters in DES Mode	Non-DES Mode Offset Spur Locations	DES Mode Offset Spur Locations
ADC10D1x00	2	4	DC, Fs/2	DC, Fs/4, Fs/2
ADC12D1x00	2	4	DC, Fs/2	DC, Fs/4, Fs/2
ADC12Dx00RF	1	2	DC	DC, Fs/2
ADC12Dxx00RF	2	4	DC, Fs/2	DC, Fs/4, Fs/2

- Dual-channel mode is “Non-DES Mode”; interleaved mode is “DES Mode.”
- The ADC12D800/500RF offer the possibility of one sub-converter per bank in Non-DES Mode.

E.g.: ADC12D1000RF Harmonic Distortion Interleaved

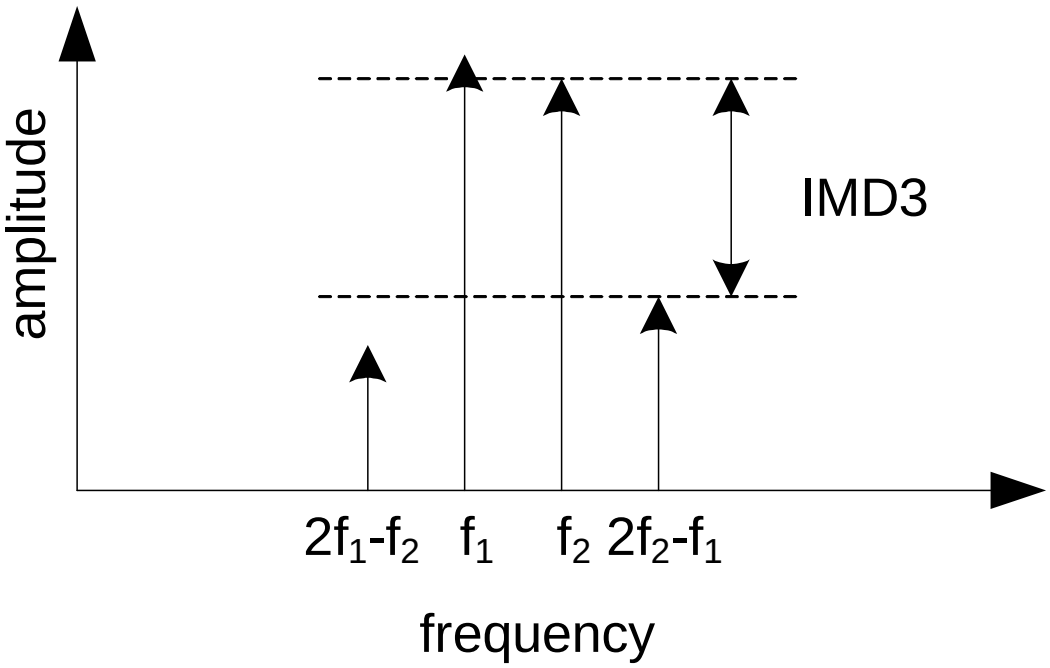


- Note the symmetrical appearance of the spurs around Fs/4 due to the 2x interleaving

<u>FFT Details:</u>

- ADC12D1800RF
- Non-DES Mode
- 2x interleaving
- NDM DDR clock
- Ain = 124.47MHz at -1dBFS

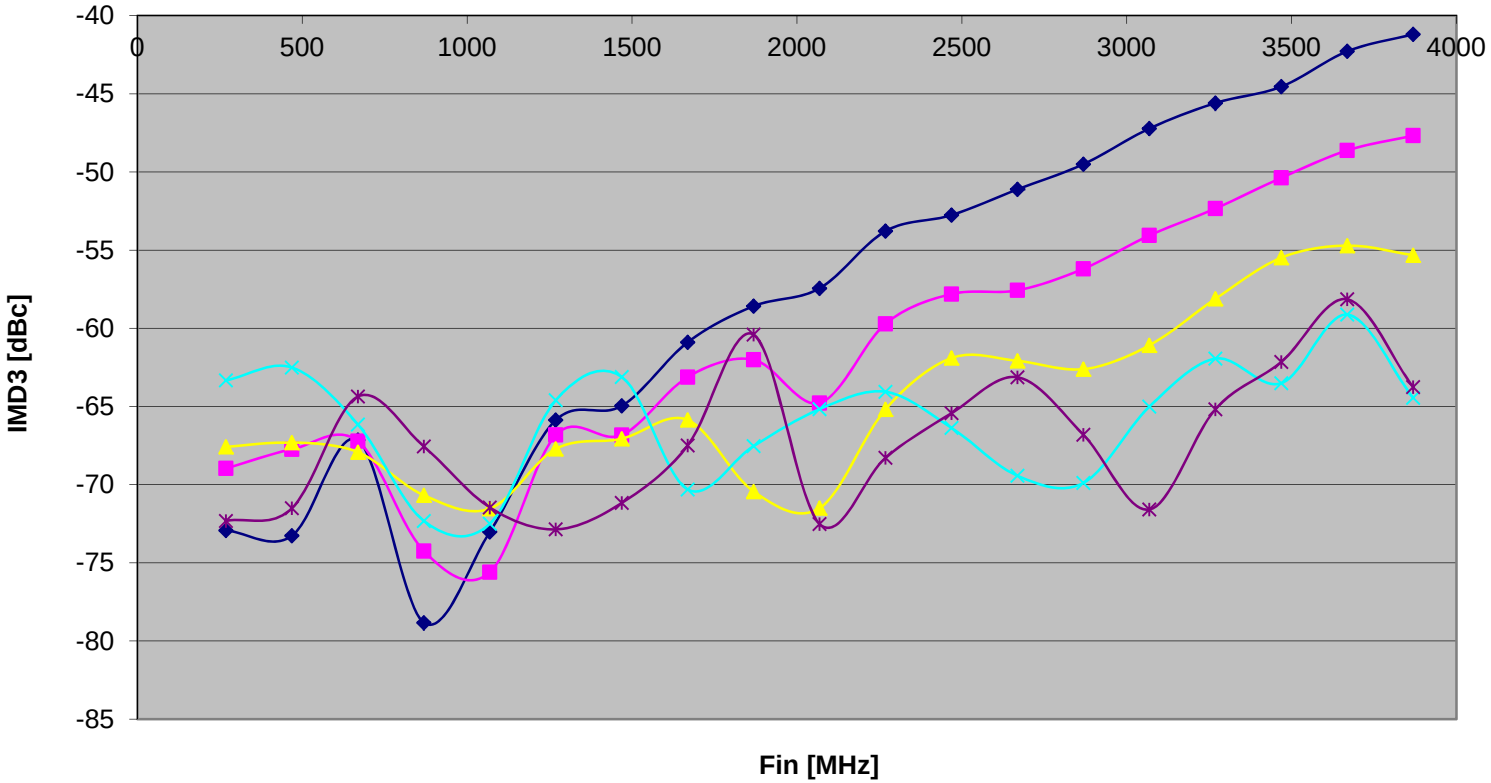
IMD_3 Concept



$$IMD_3 = \min(f_1, f_2) - \max(f_2 - f_1, f_1 - f_2)$$

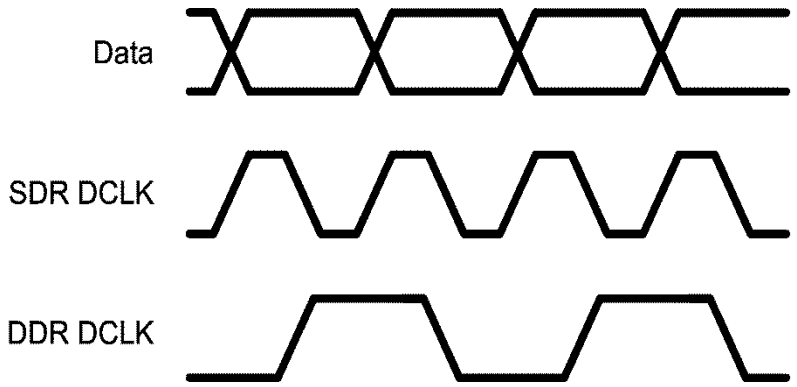
- Although there are 4 3rd order inter-modulation distortion products, only the 2 near-in ones are typically considered for an ADC: $2f_2$-f_1 and $2f_1$-f_2.
- The amplitude of the fundamentals, f_1 and f_2, should be set:
  - At, but not above -7dBFS
  - As close to each other as possible, preferably <0.1dB
- The difference between f_1 and f_2 in the diagram is exaggerated to show which is chosen to measure IMD_3.

E.g. ADC12D1800RF IMD_3



DCLK Spur

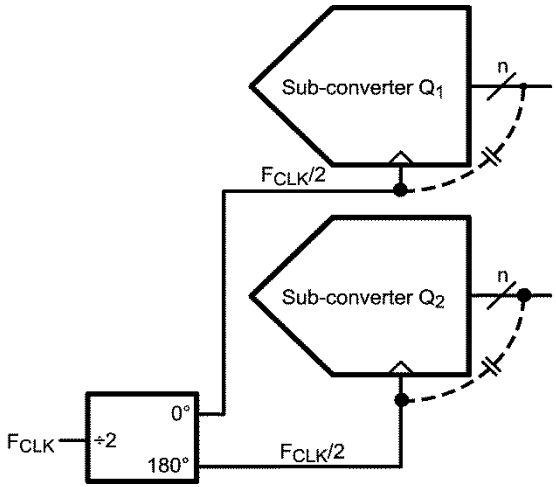
Product	NDM SDR DCLK (MHz)	NDM DDR DCLK (MHz)	Demux SDR DCLK (MHz)	Demux DDR DCLK (MHz)	DES Mode Spur Locations				Non-DES Mode Spur Locations			
ADC10D1500	N/A	500	N/A	250	N/A	Fs/4	N/A	Fs/8	N/A	Fs/2	N/A	Fs/4
ADC12D1800	N/A	900	N/A	450	N/A	Fs/4	N/A	Fs/8	N/A	Fs/2	N/A	Fs/4
ADC12D800RF	800	400	400	N/A	Fs/2	Fs/4	Fs/4	N/A	Fs	Fs/2	Fs/2	N/A
ADC12D1800RF	N/A	900	N/A	450	N/A	Fs/4	N/A	Fs/8	N/A	Fs/2	N/A	Fs/4

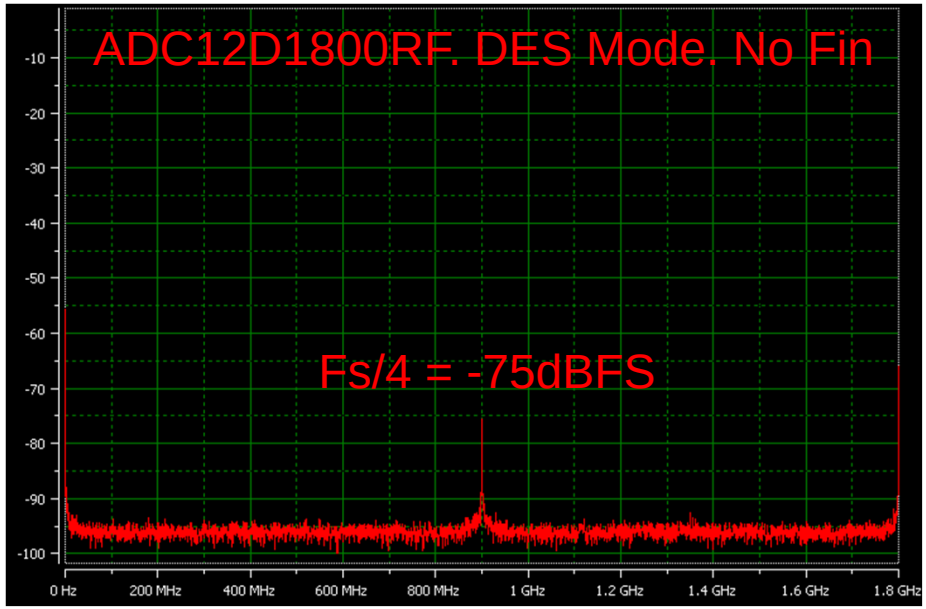


- Depending upon the mode, the Data Clock (DCLK) can couple back into the analog circuitry to appear in the output.

Sub-converter Clock Spur

Product	Fclk (MHz)	Sub-converters / Channel	Sub-converter Clock (MHz)	DES Mode Spur Location	Non-DES Mode Spur Location
ADC1xDxxxx	Fclk	N	Fclk / N	Fs / (2*N)	Fs / N
ADC12D1800RF	1800	2	900	Fs / 4	Fs / 2
ADC12D500RF	500	1	500	Fs / 2	Fs = DC



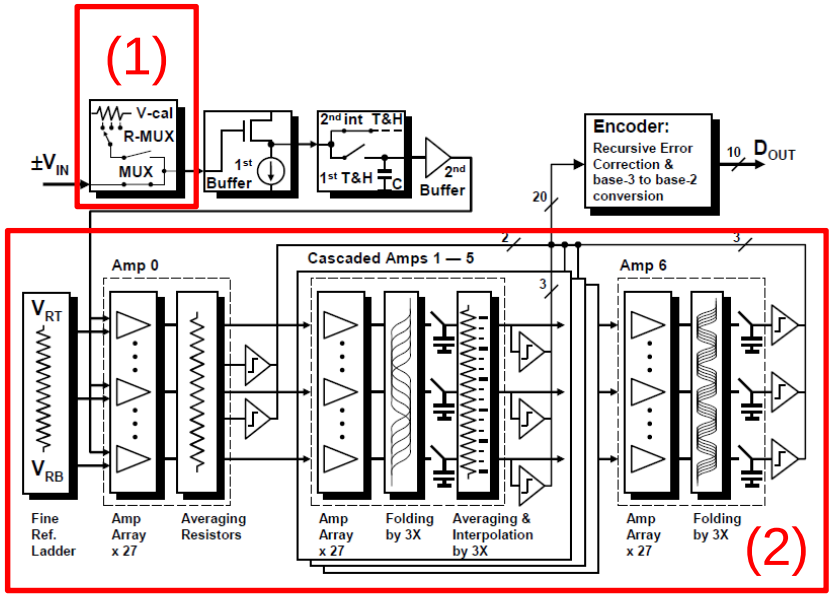


Spur Source Summary and Conclusions

- Spur sources
  - Non-linearities from the track-and-hold
  - Non-linearities from the folding-interpolating architecture
  - Interleaving images from gain mismatch and timing skew
  - Fixed frequency spurs: DCLK, offset mismatch in interleaving, sub-converter clock
- Conclusions
  - Testing with single tone inputs is the traditional method for assessing the non-linear performance of an ADC, but…
  - It may not be adequate or relevant for most real world applications
  - The next section illustrates how some non-linearities discussed in this section are either mitigated or reduced based on input signal type

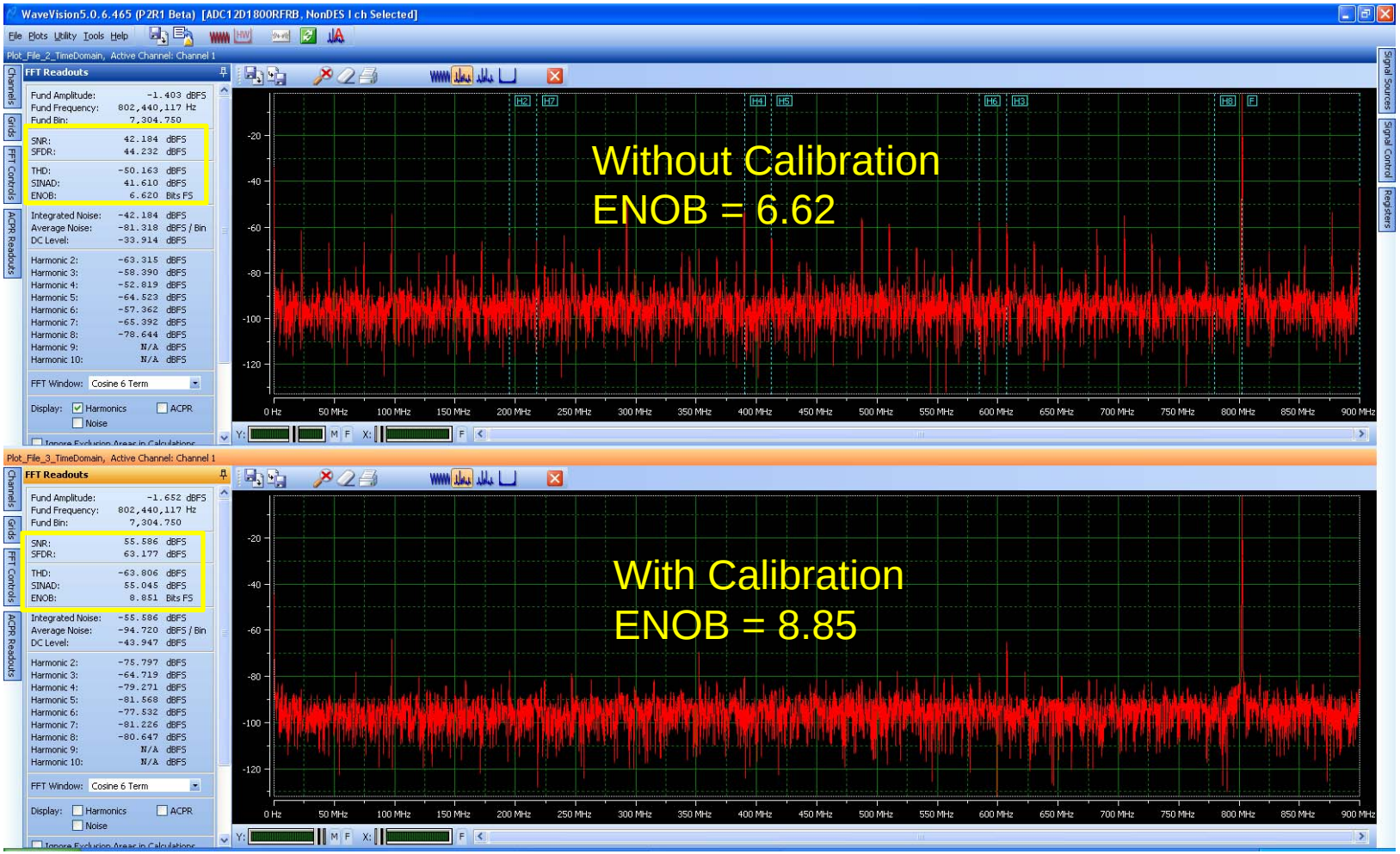
METHODS OF MITIGATION

Calibration



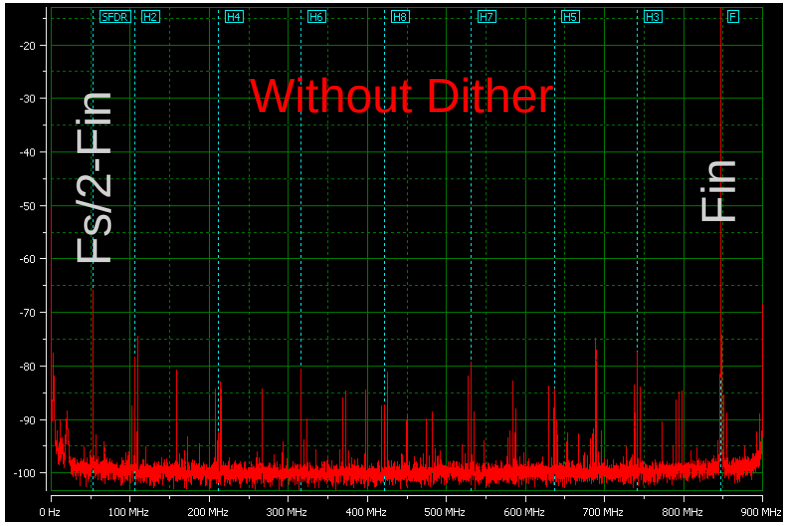
- Calibration is the primary way to address spurs due to non-linearities in the conversion process
- A foreground calibration addresses the following:
  - (1) trim the analog input resistance
  - (2) trim amplifier bias currents
- Minimize full-scale error, offset error, DNL and INL, which results in the maximum dynamic performance

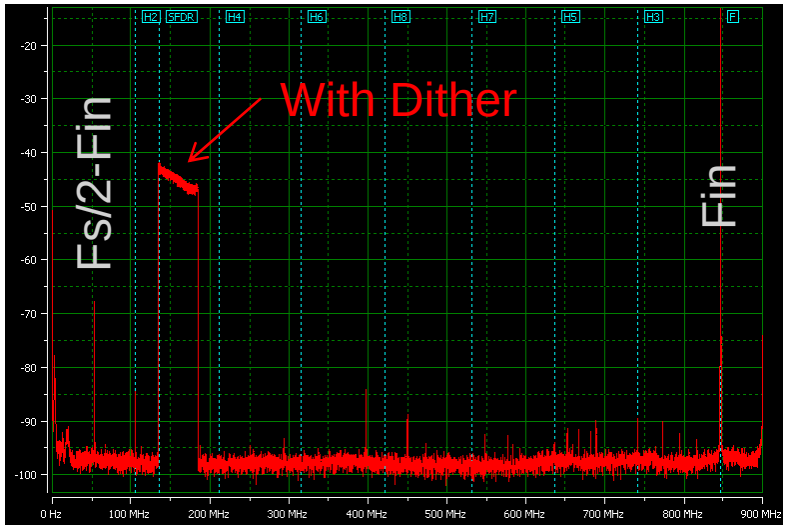
Before-and-After Calibration



ADC12D1800RF Fin = 997.47MHz Non-DESI Mode

Dithering to Improve Harmonics



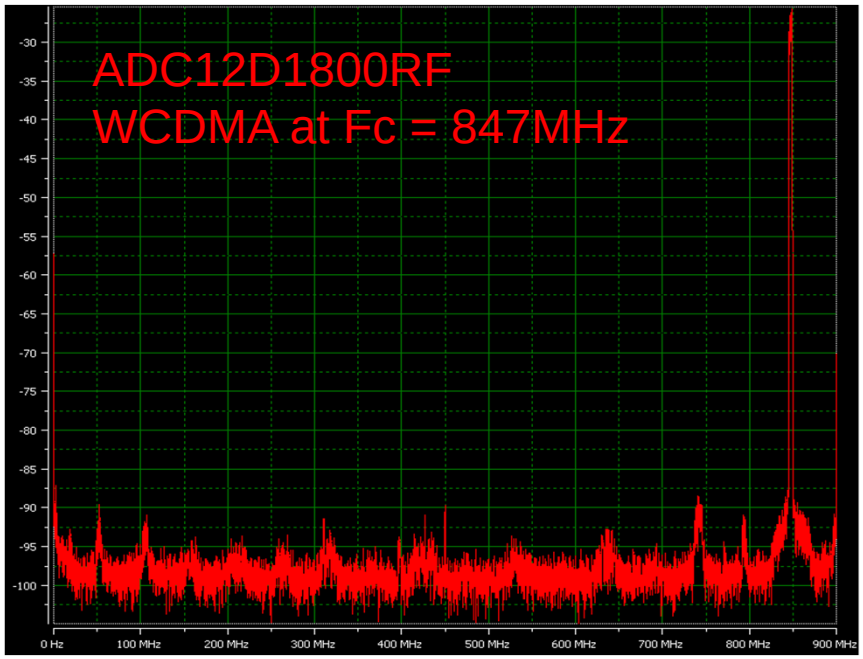


- Adding dither or band-limited noise improves harmonic performance

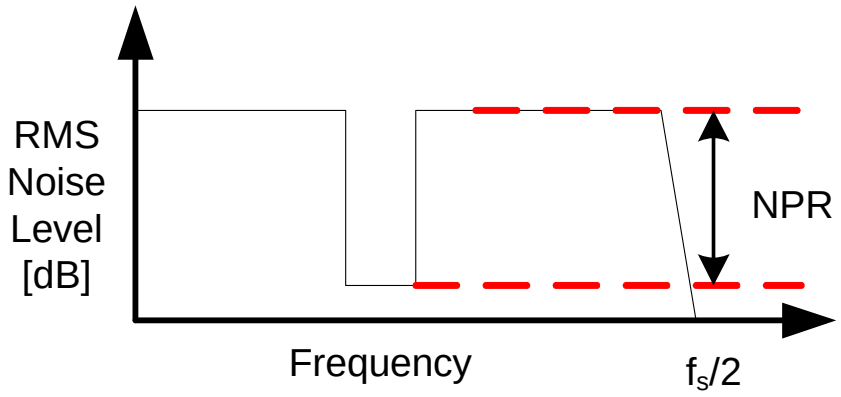
E.g. ADC12D1800RF Ain=-13dBFS

Harmonic	No Dither (dBc)	With Dither (dBc)	Improvement (dB)
H2	-65	-70	5
H3	-64	-74	10
H4	-77	-77	0
H5	-70	-75	5
H6	-67	-77	10
H7	-66	-78	12

Wideband Input Signals behave like dither



- In an application with wideband input signals, each signal will act as “dither” on the others and improve its harmonics
- Noise Power Ratio (NPR) can be used to measure how quiet one unused channel in a wideband system remains in the presence occupied channels

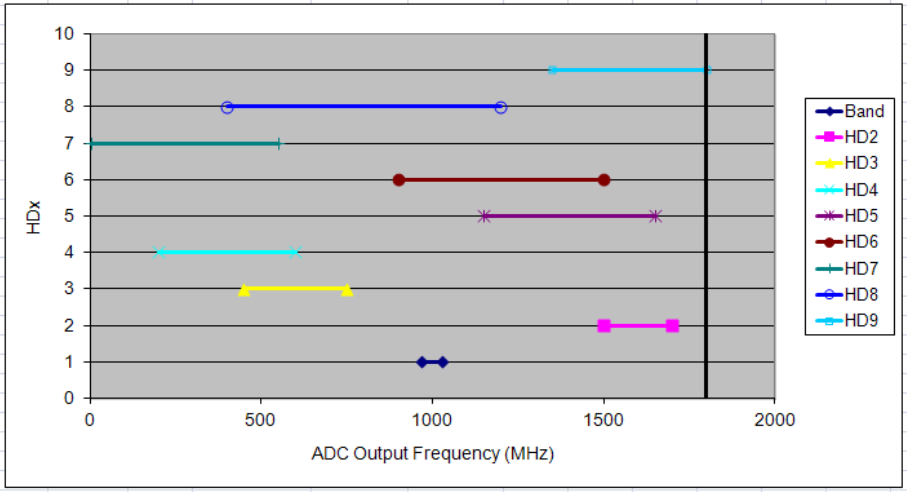


$$NPR = 10 * \log_{10} \frac{P_{Ni}}{P_{No}}$$

Frequency Planning

	Inputs Here
signal BW	60.00
Filter BW	100.00
Signal Center Freq	1000.00
ADC Sample Rate	3600.00

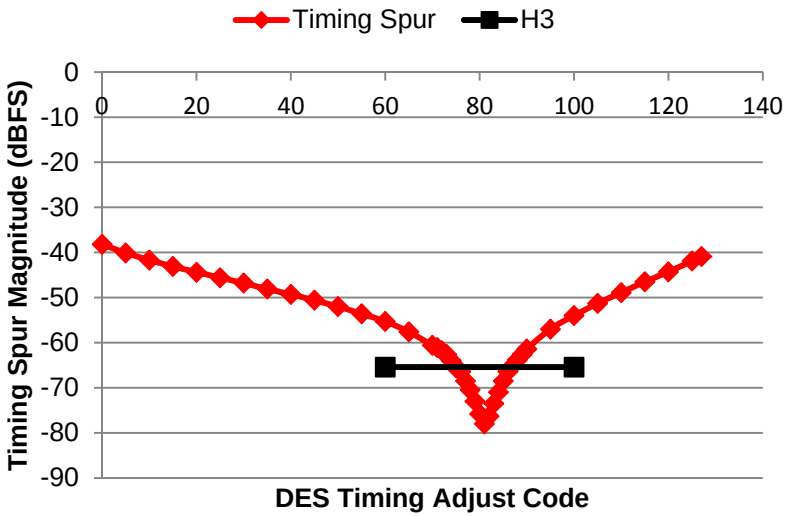
Results									
	Signal	HD2	HD3	HD4	HD5	HD6	HD7	HD8	HD9
Min Freq	1030	1700	750	600	1650	1500	550	1200	1800
Max Freq	970.6	1500	450	200	1150	900	3	400	1350
Overlaps signal		0	0	0	0	1	0	1	0



- Frequency planning can be used to make sure lower order harmonics do not interfere with the desired signal.
- The ***ADC Harmonic Calculator*** can be found at the link below.
- Please note that this tool does not yet include the effects of interleaved harmonics.

http://www.ti.com/lsds/ti/analog/dataconverters/tools.page

Analog Correction of Interleaving Spurs



- Example: Using the DES Timing Adjust on the ADC12D1800RF to adjust the level of the interleaving spur at Fs/2-Fin.
- At its relative minimum, the power in the spur is due to gain mismatch between the I/Q-channel

GSPS ADC Feature	DES Mode Spur Addressed	Spur Source
I/Q-ch Offset Adjust	Fs/2	I/Q-ch offset mismatch
I/Q-ch FSR Adjust	Fs/2 - Fin	I/Q-ch gain mismatch
Duty Cycle Correct	Fs/2 - Fin	I/Q-ch timing skew
DES Timing Adjust	Fs/2 - Fin	I/Q-ch timing skew

Digital Correction of Interleaving Spurs

- Interleave correction reduces spectrum offset spurs and images
- Dithering does not affect the level of interleaving spurs
- Correction in analog /digital domain
  - For resolution > 8 bits, achieving the level of matching required in the analog domain is extremely difficult
- Digital correction: *estimate* the errors and *correct* the data with coefficients
- Estimation
  - Detection in time-domain or frequency domain
  - Convergence
- Calibration time
  - Foreground: Calibration interrupts normal operation
  - Background: Calibration runs continuously

Reducing Fixed Frequency Spurs

- Fixed frequency spurs occur from the DCLK, offset mismatch, and sub-converter clock
- Example solutions include DCLK Mode choice, system architecture choices, and ADC selection

Example	Spur Source	Solution
A spectrum analyzer uses the ADC12D800RF interleaved and cannot tolerate a strong spur in the middle of the spectrum	• DCLK running in Demux SDR Mode causes a spur at Fs/4	• Choose instead the Non-Demux SDR DCLK, which moves the spur to Fs/2
A wideband communications application uses the ADC12D1800RF interleaved to achieve high sampling bandwidth	• DCLK produces spur at Fs/8 or Fs/4 • Offset mismatch spur at Fs/4 • Sub-converter clock spur at Fs/4	• Adjust the sampling clock so that the fixed-frequency spurs land on channel boundaries
A long-range tactical radar with Fs = 750Msps cannot tolerate interleave images	• Most members of the GSPS ADC family have interleaved channels, which produce image spurs	• Use the ADC12D800RF, which has only 1 converter per channel

SUMMARY AND RECOMMENDATIONS

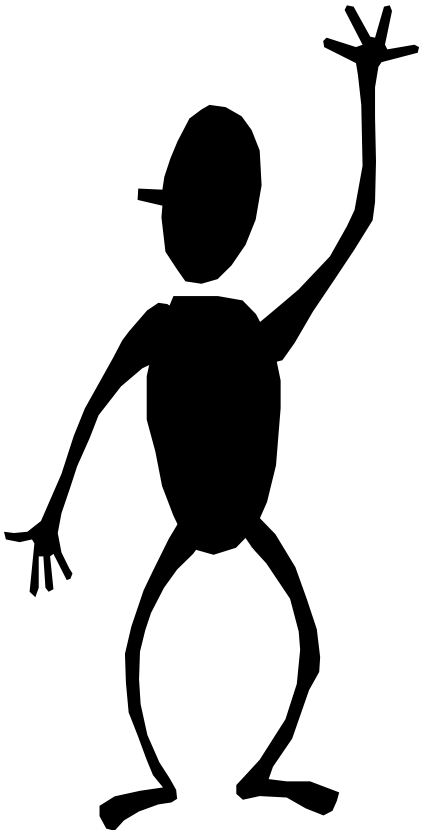
Summary and conclusions

- In order to achieve high-resolution, high-sampling rate ADCs, certain techniques were chosen which also generate spurious content.
- Spurs in the GSPS ADC family come from non-linearities, interleaving, and system clocks.
- Techniques to address these spurs include ADC features such as calibration, dithering, and frequency planning.
- Input signals that consist of multiple wideband signals or single tones act like dithering and reduce the impact of non-linearities.

Solutions Recommendation

Spur	Dominant Source	Solution
Lower order harmonics	Non-linearity in track-and-hold	• Calibration • Frequency planning
Higher order harmonics	Folding-interpolating architecture	• Calibration • Dithering
IMD_3	Non-linearity in track-and-hold, folding-interpolating architecture	
DC, Fs/4, Fs/2	Sub-converter offset mismatch in interleaving architecture	• ADC selection • ADC features • Digital correction
Fs/2 – Fin, Fs/4 ± Fin	Sub-converter gain mismatch and timing skew in interleaving architecture	
Fs/8, Fs/4, Fs/2	Coupling from DCLK	• DCLK selection
DC, Fs/2	Coupling from sub-converter clock	• ADC selection

Questions?



- Thank you for attending!
- Any questions?