BIG GIG REFERENCE PLATFORM

ADC08DL500

MANUFACTURING KIT / REFERENCE DESIGN (A1)

National Semiconductor 8 bit ADC + XILINX Virtex 4

SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.

Since this product is in development, the user of this document is strongly advised to check for the latest revision.

National Semiconductor reserves the right to make changes to this product.
ALL parts labeled "N/A" are NOT ASSEMBLED.

Print Instructions:
- To create a readable printout, we recommend to use A3 or 11x17" paper size.
- When printing from this PDF file, make sure to check the "Shrink to fit" box.

SYSTEM CONFIGURATION

Module	Configuration	Description
FRONT END	2 channel DIFFERENTIAL	AC COUPLING OF SIGNAL PATH ONLY
CLOCK SOURCE	DIFFERENTIAL	LMX2312 PLL
FPGA		XC4VLX15 - 363 PIN BGA
USB I/F		CY7C64613 EZ USB

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NATIONAL SEMICONDUCTOR CORPORATION
DVD PRODUCT LINE
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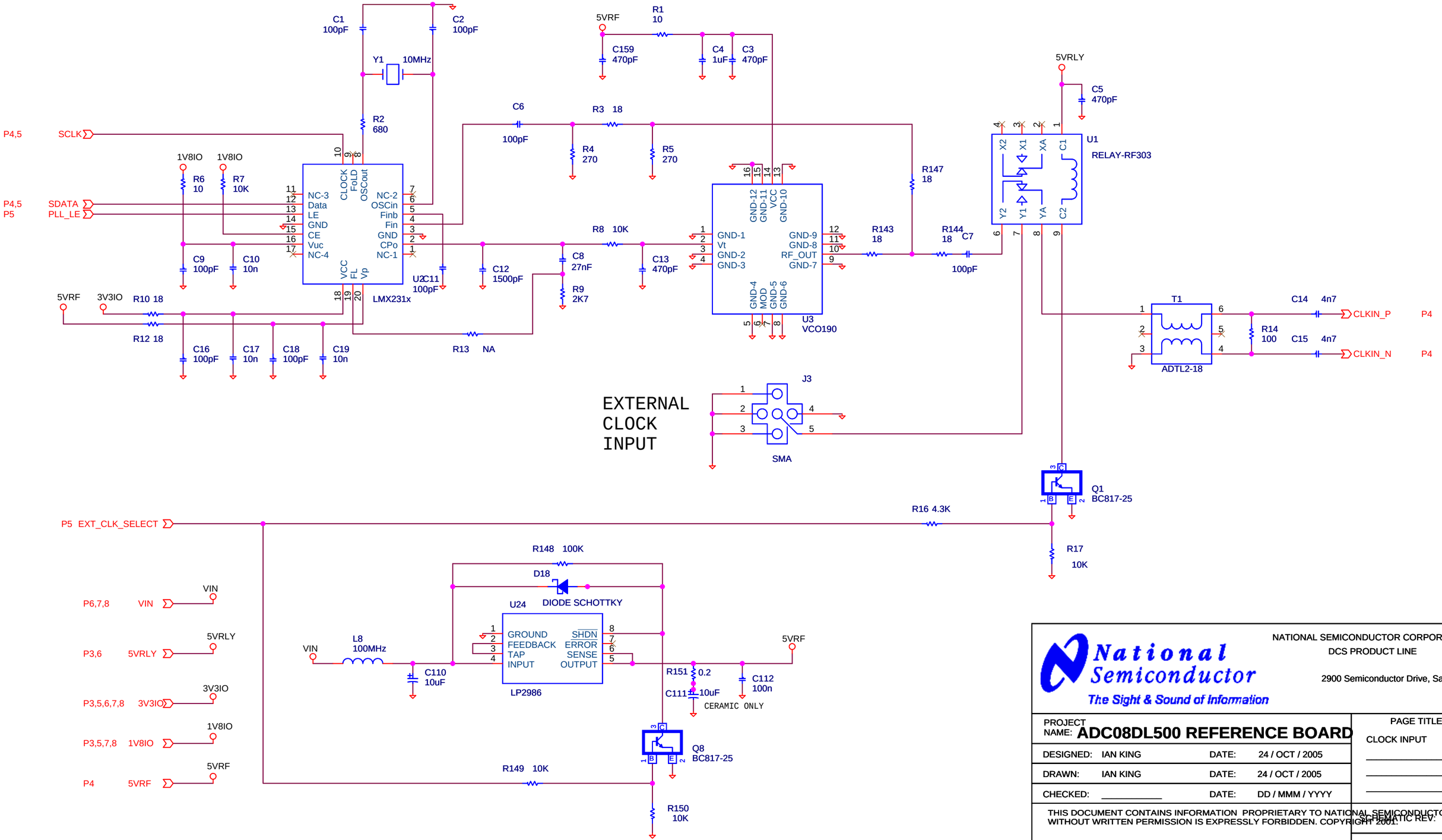
http://www.national.com/appinfo/dvd/

PROJECT NAME:	**ADC08DL500 REFERENCE BOARD**				
DESIGNED:	IAN KING	DATE:	Oct 24th 2005	LAYOUT JOB#:	xx
DRAWN:	IAN KING	DATE:	Oct 24th 2005	LAYOUT REV:	REV 2.0
CHECKED:	.	DATE:	April 12th, 2011	ASSEMBLY REV:	A1
				SCHEMATIC REV:	2.0
LAST MODIFIED:	Tuesday, April 12, 2011		DOC # : xx	Sheet	1 OF 8



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PROJECT NAME:	ADC08DL500 REFERENCE BOARD		
DESIGNED:	IAN KING	DATE:	24 / OCT / 2005
DRAWN:	IAN KING	DATE:	24 / OCT / 2005
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PAGE TITLE: CLOCK INPUT

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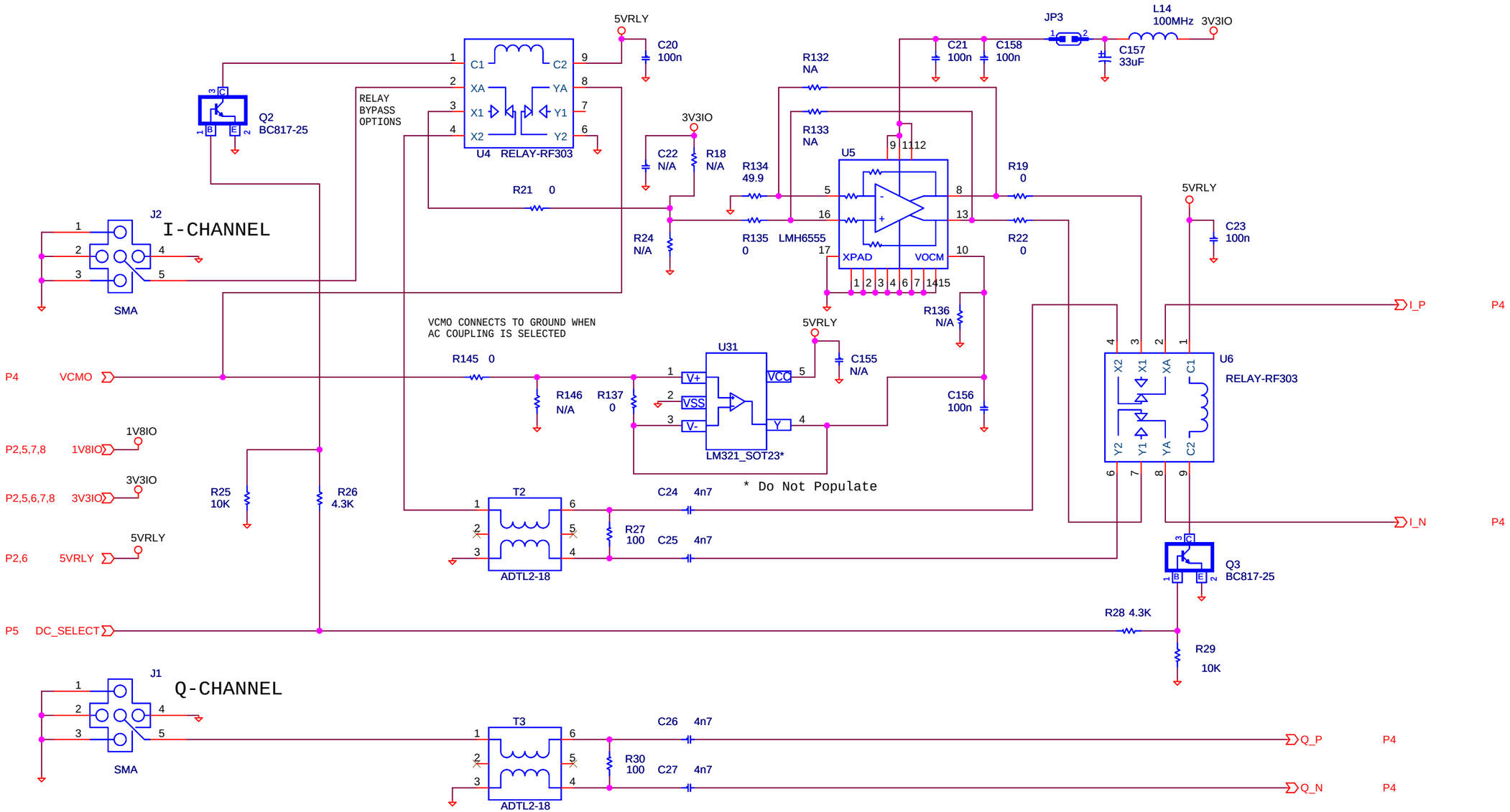
Sheet 2 OF 8



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PROJECT NAME:	**ADC08DL500 REFERENCE BOARD**		PAGE TITLE: ANALOG INPUTS
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U9D XC4VLX15_363FBGA

1.9V ADC SUPPLY MUST BE CONTROLLED BY FPGA SO THAT TRI STATE PINS ARE CONFIGURED CORRECTLY AT POWER UP

DCI RESISTORS FOR LVDS

U10A ADC08DL500

U10B ADC08DL500

U30 2MM_7PIN_HEADER

U33 2MM_7PIN_HEADER

test header

U9E XC4VLX15_363FBGA

DCI RESISTORS FOR LVDS

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PAGE TITLE
ADC08D1000
VIRTEX 4 LVDS

SCHEMATIC REV: 2.0

Sheet 4 OF 8

C50 100n C51 100n C52 100n C53 100n C54 100n C172 100n C173 100n C174 100n C175 100n

EEPROM

U15 24C02/SO8 — C63 100n, R73 2.2K, R74 2.2K, SCL, SDA

USB =>

J6 USB-B — C169 4.7n, R175 1M

Cypress CY7C68013A-100AXC

U12A

RDY0/SLRD, RDY1/SLWR, RDY2, RDY3, RDY4, RDY5, INT5_N, INT4, T0, T1, T2, TXD0, RXD0, TXD1, RXD1, CTL0/FLAGA, CTL1/FLAGB, CTL2/FLAGC, CTL3, CTL4, CTL5, NC1, NC2, NC3, WAKEUP, RESET_N, WR_N, RD_N, BKPT, SDA, SCL, IFCLK, AGND2, DMINUS, DPLUS, XTALIN, XTALOUT, CLKOUT

PE7/GPIFADR8 CONF_DONE; PE6/T2EX CY_VALID; PE5/INT6 R61 47 CY_REQ, R60 47 LOAD_STATE; PE4/RXD1OUT STATE3; PE3/RXD0OUT STATE2; PE2/T2OUT STATE1; PE1/T1OUT STATE0; PE0/T0OUT

PD7/FD15 CY_DATA15; PD6/FD14 CY_DATA14; PD5/FD13 CY_DATA13; PD4/FD12 CY_DATA12; PD3/FD11 CY_DATA11; PD2/FD10 CY_DATA10; PD1/FD9 CY_DATA9; PD0/FD8 CY_DATA8

PB7/FD7 CY_DATA7; PB6/FD6 CY_DATA6; PB5/FD5 CY_DATA5; PB4/FD4 CY_DATA4; PB3/FD3 CY_DATA3; PB2/FD2 CY_DATA2; PB1/FD1 CY_DATA1; PB0/FD0 CY_DATA0

PA7/FLGD/SLCS_N SLCS_N; PA6/PKTEND; PA5/FIFOADR1; PA4/FIFOADR0 FIFOADR0; PA3/WU2; PA2/SLOE; PA1/INT1_N; PA0/INT0_N

PC7/GPIFADR7 CONF_INITB; PC6/GPIFADR6 CONF_DIN; PC5/GPIFADR5 R67 47 CONF_CCLK; PC4/GPIFADR4 R66 47 PROGRAMB; PC3/GPIFADR3 R64 47 MSTR_SCLK; PC2/GPIFADR2 MSTR_SDATA; PC1/GPIFADR1; PC0/GPIFADR0

nPOWER_EN P6,8; FPGA_RESET P8; R69 3.3K, R70 3.3K

24MHz, Y2, C58 12pF, C59 12pF, TP3 TP_CY_CLK

CY_DATA[15:0]

USB D- and D+ lines should be controlled impedance lines, as described in the Cypress document high_speed_usb_pcb_layout_recommendations_9.pdf

USB POWER ON & PB RESET

U11 LM3722 — C55 100n, R57 0, R58 100k, SW1 RESET, RESETB

JTAG HEADER

J5 — C57 100n, R62 0 FIT IF CONFIG FLASH NOT INSTALLED

V4_TMS, V4_TDO, V4_TCK, FLSH_TDI, FLSH_TDO, V4_TDO P8

XC4VLX15_363FBGA

U9A

PROGRAM_B_0 F12; INIT_0 E12; DONE_0 F11; D_IN_0 E9; DOUT_BUSY_0 T11; CCLK0 E11; M0_0 R12; M1_0 T12; M2_0 R11; HSWAPEN_0 E13; CS_B_0 E8; RDWR_B_0 F9; VBATT_0 T13; PWRDWN_B_0 T10; TMS_0 T8; TDO_0 R10; TCK_0 T9; TDI_0 R9; TDN_0 E10; TDP_0 F10

R53 4.7K, P8 CONF_DONE, R55 0, R56 A/B 0, R59 A/B 10K, SLAVE SERIAL, MASTER SERIAL

Assembly instructions:
R56 = Position A
R59 = Position B

TEMP SENSOR

U13 LM95221CIMM — C154 N/A, C61 2.2n, C62 2.2n, C60 100n, P4 ADC_TD_P, P4 ADC_TD_N, SCL, SDA

SDA/SCL - CROSSED WIRES - LIFT PINS AND FIX WITH WIRE MODIFICATION

DO NOT FIT V4 CONFIG FLASH IF CYPRESS USB CONTROLLER IS INSTALLED

XC4VLX15_363FBGA

U9B

UPLOAD_Q F15; SAMPLE_Q E15; TRIGGER_Q E6; OVRANGE_Q F6; CLK_ACTIVE_Q D15; POWER_DOWN E14; POWER_DOWN_Q E7; PLL_LE D6; ADC_CS D13; SCLK C13; SDATA C8; ECM_FSR D8; CALIBRATE D12; TRIG_IN C12; READ C9; CAPTURE D9; CY_DATA9 V16; CY_REQ V15; CY_VALID V6; STATE0 V5; STATE1 T14; STATE2 U13; STATE3 U8; LOAD_STATE T7; FPGA_RESET V13; MSTR_SDATA V12; MSTR_SCLK V9; DC_SELECT V8; EXT_CLK_SELECT U12; nADC_1V9_EN V11; FIFO_FULL V10; FIFO_EMPTY U9

P4 POWER_DOWN; P4 POWER_DOWN_Q; P2 PLL_LE; P4 ADC_CS; P2,4 SCLK; P2,4 SDATA; P4 ECM_FSR; P4 CALIBRATE; P3 TRIG_IN; P8 READ; P8 CAPTURE; P8 FPGA_RESET; P8 MSTR_SDATA; P8 MSTR_SCLK; P3 DC_SELECT; P2 EXT_CLK_SELECT; P6 nADC_1V9_EN; P8 FIFO_FULL; P8 FIFO_EMPTY

IO_L1P_D31_LC_1 … IO_L8N_D16_CC_LC_1 … IO_L1P_D15_CC_LC_2 … IO_L8N_D0_LC_2

BANK1 - 1.8V IO

BANK2 - 3.3V CMOS

XC4VLX15_363FBGA

U9C

LVDS CLOCK AND OVER RANGE INPUTS FROM ADC

P4 DCLK_P, P4 DCLK_N

DCI RESISTORS FOR LVDS — R79 51, R80 51, 2V5IO

P4 OVR_P, P4 OVR_N

IO_L1P_GC_CC_LC_3 … IO_L8N_GC_CC_LC_3 … IO_L1P_GC_LC_4 … IO_L8N_GC_LC_4

CY_DATA0 W13; CY_DATA2 W12; Y5; CY_DATA8 W5; CY_DATA1 Y12; CY_DATA3 Y11; CY_DATA11 Y6; CY_DATA10 W6; CY_DATA4 W11; CY_DATA6 W10; CY_DATA13 Y7; CY_DATA12 W7; CY_DATA5 Y10; CY_DATA7 Y9; CY_DATA15 W9; CY_DATA14 W8

BANK3 - 2.5V LVDS

BANK4 - 3.3V CMOS

100MHz FPGA CLOCK REF

L18 100MHz, C171 2.2uF, C170 0.01uF, C167 0.1uF, C64 100n, Y3 OSC (SM), R78 47

Cypress CY7C68013A-100AXC

U12B

VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7, VCC8, VCC9, AVCC1, AVCC2

GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8, GND9, AGND1, RSVD_GND

TP8 GND, TP9 GND, TP10 GND, TP11 GND

PWR STB, IDL CLK, SMP OVR, UPL TRG

LD1 LED_2x1, LD2 LED_2x1, LD3 LED_2x1, LD4 LED_2x1

R81 10k, R82 10k, R83 10k, R84 10k, R85 10k 1V8IO

U16 74LVC541 — UPLOAD, TRIGGER, SAMPLE, OVRANGE, IDLE, CLK_ACTIVE; UPLOAD_Q, TRIGGER_Q, SAMPLE_Q, OVRANGE_Q, IDLE_Q, CLK_ACTIVE_Q

R86 330R, R87 330R, R89 330R, R91 330R, R93 330R, R88 330R, R90 330R, R92 330R, C72 100n

U18 74LVC1G04 — C73 100n, nPOWER_EN

U17 74LVC1G00 — UPLOAD_Q, SAMPLE_Q, R94 3.3K, R95 3.3K, C74 100n

IDLE LED WILL ILLUMINMATE ONLY WHEN FPGA IS CONFIGURED

nPOWER_EN = 1 - SWITCH REGS SHUTDOWN (STANDBY)
nPOWER_EN = 0 - SWITCH REGS ARE ON

Each unrouted FPGA pad should have a via connecting it to the bottom layer of the board. This will allow access to IO pins of the FPGA for development purposes.

U14 XCF08P_VO48 N/A — C65 100n, C66 100n, C67 100n, C68 100n, C69 100n, C70 100n, C71 100n

R127 3.3K, PROGRAMB, R75 N/A, R76 N/A, R77 N/A, CONF_CCLK, CONF_INITB, CONF_DONE, V4_TDI, V4_TCK, V4_TMS, CONF_DIN

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DCS PRODUCT LINE
2900 Semiconductor Drive, Santa Clara, CA 95052

PROJECT NAME: ADC08DL500 REFERENCE BOARD

DESIGNED:	IAN KING	DATE:	24 / OCT / 2005
DRAWN:	IAN KING/ C. CHASE	DATE:	21 / APRIL / 2006
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PAGE TITLE: USB CONTROLLER; V4 FLASH CONFIG; LED STATUS

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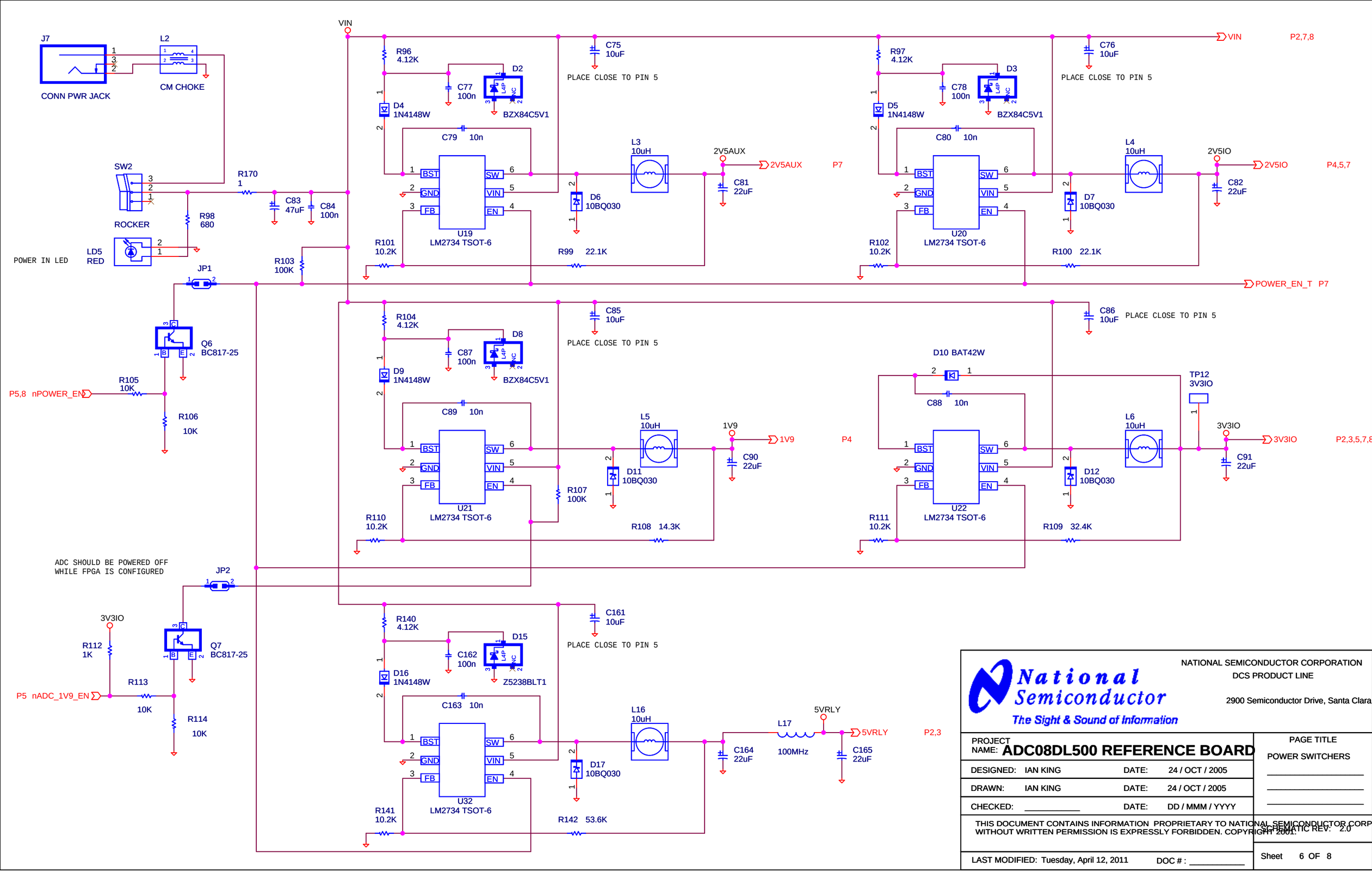

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PROJECT NAME:	**ADC08DL500 REFERENCE BOARD**	PAGE TITLE	POWER SWITCHERS
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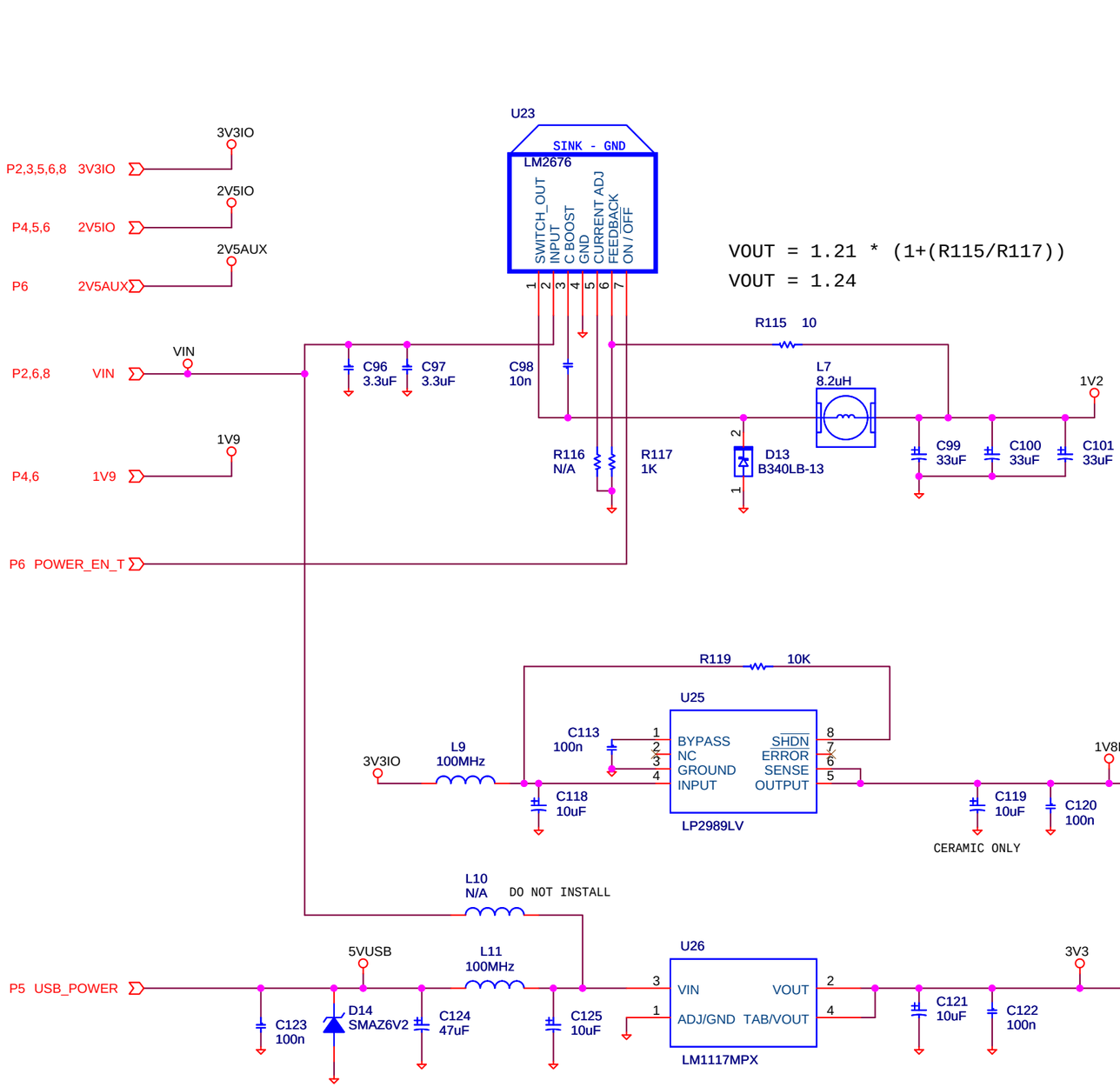
Sheet 6 OF 8



0402 FPGA Decouplers

BANK0 3V3IO: C126 100n, C127 100n

BANK1 1V8IO: C128 100n, C129 100n

BANK2 3V3IO: C130 100n, C131 100n

BANK3 2V5IO: C132 100n, C133 100n

BANK4 3V3IO: C134 100n, C135 100n

BANK5 2V5IO: C136 100n, C137 100n, C138 100n, C139 100n, C140 100n, C141 100n

BANK6 2V5IO: C142 100n, C143 100n, C144 100n, C145 100n, C146 100n, C147 100n

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PROJECT NAME: **ADC08DL500 REFERENCE BOARD**

PAGE TITLE: VIRTEX 4 POWER PERIPHERAL POWER

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P5 SDA
P5 SCL
P5 MSTR_DATA
P5 MSTR_SCLK
P5 FPGA_RESET
P5 FIFO_FULL
P5 FIFO_EMPTY
P4 DCLK_RESET

U9F

IO_L25P_CC_SM7_LC_7	T17	STROBE_IP
IO_L25N_CC_SM7_LC_7	T18	STROBE_IN
IO_L26P_SM6_7	U18	DATA_QA_P1
IO_L26N_SM6_7	U19	DATA_QA_N1
IO_L27P_SM5_7	T15	DATA_QA_P7
IO_L27N_SM5_7	U15	DATA_QA_N7
IO_L28P_7	V19	DATA_QA_P2
IO_L28N_VREF_7	V20	DATA_QA_N2
IO_L29P_SM4_7	U16	DATA_QA_P6
IO_L29N_SM4_7	U17	DATA_QA_N6
IO_L30P_SM3_7	W18	DATA_QA_P3
IO_L30N_SM3_7	W19	DATA_QA_N3
IO_L31P_SM2_7	Y17	DATA_QA_P5
IO_L31N_SM2_7	W17	DATA_QA_N5
IO_L32P_SM1_7	V17	DATA_QA_P4
IO_L32N_SM1_7	V18	DATA_QA_N4
IO_L20P_7	R19	DATA_QA_P0
IO_L20N_VREF_7	R20	DATA_QA_N0
IO_L21P_7	R15	TP4
IO_L21N_7	R16	TP5
IO_L23P_VRN_7	T19	R120 51
IO_L23N_VRP_7	T20	R121 51
IO_L24P_CC_LC_7	R17	
IO_L24N_CC_LC_7	R18	
	U3	
IO_L25P_CC_SM7_LC_8	U2	
IO_L25N_CC_SM7_LC_8	T4	DATA_QB_P5
IO_L26P_8	T3	DATA_QB_N5
IO_L26N_8	T6	DATA_QB_P0
IO_L27P_8	U6	DATA_QB_N0
IO_L27N_8	V2	DATA_QB_P7
IO_L28P_8	V1	DATA_QB_N7
IO_L28N_VREF_8	U5	DATA_QB_P3
IO_L29P_8	U4	DATA_QB_N3
IO_L29N_8	W3	DATA_QB_P6
IO_L30P_8	W2	DATA_QB_N6
IO_L30N_8	Y4	DATA_QB_P2
IO_L31P_8	W4	DATA_QB_N2
IO_L31N_8	V4	DATA_QB_P4
IO_L32P_8	V3	DATA_QB_N4
IO_L32N_8	R2	STROBE_QP
IO_L20P_8	R1	STROBE_QN
IO_L20N_VREF_8	R6	DATA_QB_P1
IO_L21P_8	R5	DATA_QB_N1
IO_L21N_8	T2	R122 51
IO_L23P_VRN_8	T1	R123 51
IO_L23N_VRP_8	R4	
IO_L24P_CC_LC_8	R3	
IO_L24N_CC_LC_8		

XC4VLX15_363FBGA

VEXT
VEXT
R138 10K
JP4 N/A
TP7
VEXT

P7 VEXT
P2,6,7 VIN
P2,3,5,6,7 3V3IO
P2,3,5,7 1V8IO
P5,7 3V3

FUTURE BUS EXPANSION CONNECTOR

P1 FUTUREBUS_24

SDA	A1	C1	DATA_QA_P0
SCL	A2	C2	DATA_QA_P1
MSTR_SDATA	A3	C3	DATA_QA_P2
MSTR_SCLK	A4	C4	DATA_QA_P3
FPGA_RESET	A5	C5	DATA_QA_P4
READ_IN	A6	C6	DATA_QA_P5
	B1	D1	DATA_QA_N0
	B2	D2	DATA_QA_N1
	B3	D3	DATA_QA_N2
	B4	D4	DATA_QA_N3
	B5	D5	DATA_QA_N4
	B6	D6	DATA_QA_N5

P2 FUTUREBUS_24

CAPTURE_IN	A1	C1	DATA_QA_P6
FIFO_FULL	A2	C2	DATA_QA_P7
FIFO_EMPTY	A3	C3	STROBE_IP
DCLK_RESET	A4	C4	DATA_QB_P0
P5 CONF_DONE	A5	C5	DATA_QB_P1
P5 V4_TMS	A6	C6	DATA_QB_P2
	B1	D1	DATA_QA_N6
	B2	D2	DATA_QA_N7
	B3	D3	STROBE_IN
	B4	D4	DATA_QB_N0
	B5	D5	DATA_QB_N1
	B6	D6	DATA_QB_N2

P3 FUTUREBUS_24

P5 V4_TCK	A1	C1	DATA_QB_P3
P5 V4_TDI	A2	C2	DATA_QB_P4
P5 V4_TDO	A3	C3	DATA_QB_P5
notSHUTDOWN	A4	C4	DATA_QB_P6
	A5	C5	DATA_QB_P7
	A6	C6	STROBE_QP
	B1	D1	DATA_QB_N3
	B2	D2	DATA_QB_N4
	B3	D3	DATA_QB_N5
	B4	D4	DATA_QB_N6
	B5	D5	DATA_QB_N7
	B6	D6	STROBE_QN

L12 100MHz
3V3IO
C150 100n
L13 100MHz
VIN
C151 100n

3V3
R124 10K
EXTERNAL STANDBY CONTROL
NOT REQUIRED IF USB MICRO IS INSTALLED

U29
74LVC1G06
3V3
C152 100n
3V3
R125 N/A
R126 N/A
nPOWER_EN P5,6

1V8IO
U27
C148 100n
R129 47
READ P5
74LVC1G17

U28
C149 100n
R130 47
CAPTURE P5
74LVC1G17

LOGIC ANALYSER HEADER

J8

1				2	
3	+5V	NC-1		4	
5	GND	NC-2		6	STROBE_QP
7	CLKe	CLKo		8	DATA_QB_P7
9	D15e	D15o		10	DATA_QB_P6
11	D14e	D14o		12	DATA_QB_P5
13	D13e	D13o		14	DATA_QB_P4
15	D12e	D12o		16	DATA_QB_P3
17	D11e	D11o		18	DATA_QB_P2
19	D10e	D10o		20	DATA_QB_P1
21	D9e	D9o		22	DATA_QB_P0
23	D8e	D8o		24	DATA_QA_P7
25	D7e	D7o		26	DATA_QA_P6
27	D6e	D6o		28	DATA_QA_P5
29	D5e	D5o		30	DATA_QA_P4
31	D4e	D4o		32	DATA_QA_P3
33	D3e	D3o		34	DATA_QA_P2
35	D2e	D2o		36	DATA_QA_P1
37	D1e	D1o		38	DATA_QA_P0
	D0e	D0o			
39	GND1	GND2		40	
41	GND3	GND4		42	
43	GND5				

CONN 38 PIN MICTOR

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2900 Semiconductor Drive, Santa Clara CA 950

PROJECT NAME: ADC08DL500 REFERENCE BOARD

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PAGE TITLE
EXPANSION HEADER
LA CONNECTOR

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