

AFE707xEVM Quick Guide

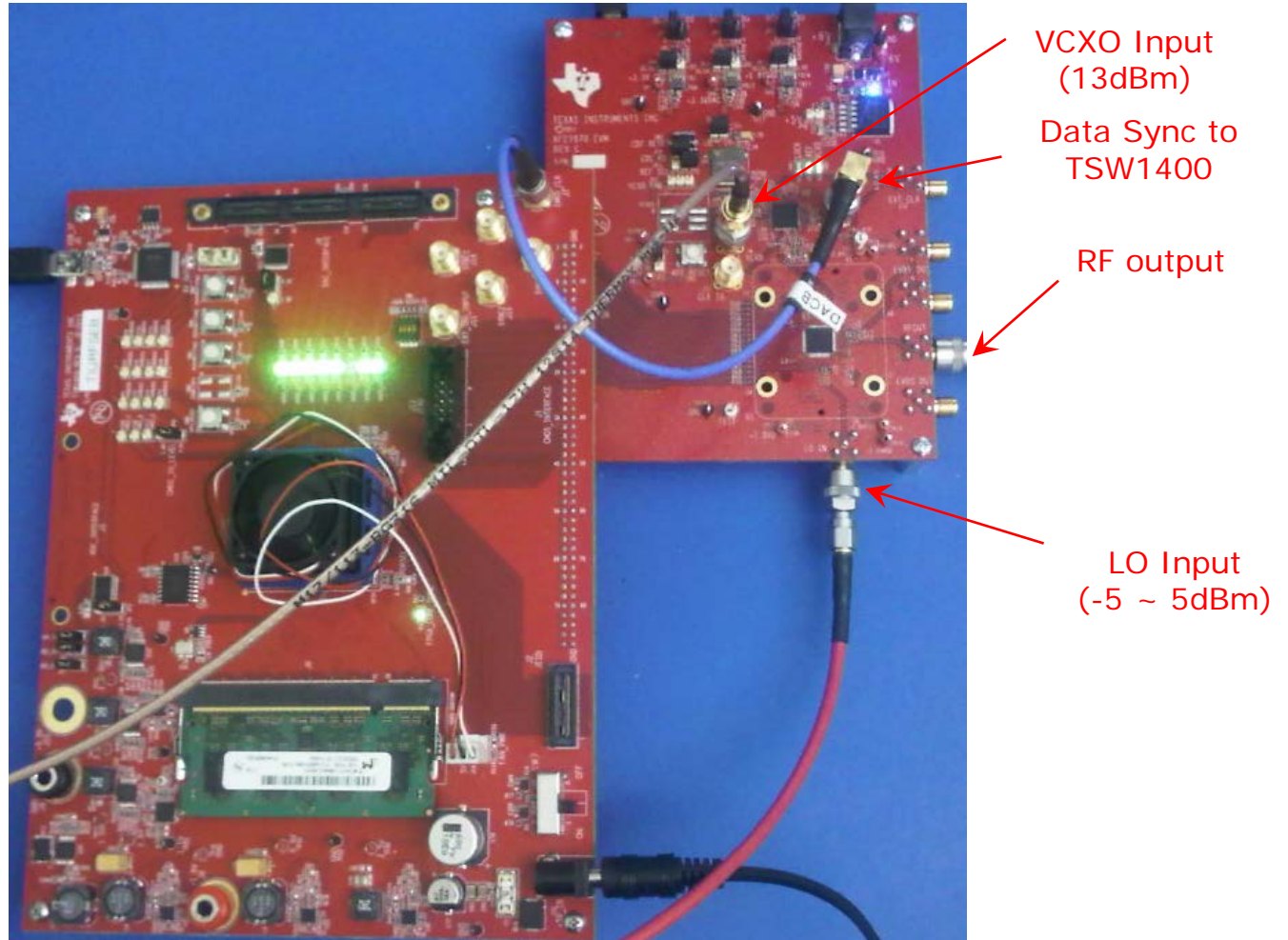
High Speed Data Converters

AFE707xEVM + TSW1400EVM

- Equipment: 2 Signal Generator
(One for external VCXO J4 and the other for external LO J10) and Spectrum Analyzer
- EXT VCXO (J4): AFE7070 DAC clock source (122.88MHz which give AFE707x 61.44MHz of sampling clock)
- LO IN (J10): External LO source (950MHz)
- Power: +6V Plug-in Power Supply
- Test Signal: Single-tone (10MHz) from TSW1400

- *Connect USB cable to AFE707xEVM and configure AFE707x*
- *And then connect USB cable to TSW1400EVM*

AFE707x + TSW1400EVM Configuration



AFE707xEVM GUI capture (AFE707x)

AFE7070 EVM Software Control
Version 2.5

AFE7070 | CDCM7005 | Reset USB Port | Exit

Power Control

- Sleep Awake
- Power Down Fuses Powered
- Power Down Clock Receiver Powered
- LVDS Power Down Powered
- RF Out Power Down Powered
- DAC Power Down Powered
- Analog Out Power Down Powered
- Pwr Dn Clock Receiver on SLEEP No
- LVDS Pwr Dn when SLEEP No
- RF out Pwr Dn when SLEEP No
- DAC Pwr Dn when SLEEP No
- Analog out Pwr Dn when SLEEP No

FIFO Settings

FIFO Disabled

FIFO Offset: -4 -2 0 2 3

- Mask 2-Away Alarm Not masked
- Mask 1-Away Alarm Not masked
- Enable 2-Away Alarm Disabled
- Enable 1-Away Alarm Disabled
- Mask FIFO Sync Not masked

FIFO 2 away

FIFO 1 away

QMC Settings

- QMC Corr Enable Disabled
- QMC Offset Enable Disabled
- QMC Offset A: 0
- QMC Offset B: 0
- QMC Gain A: 0
- QMC Gain B: 0
- QMC Phase: 0

Analog Output Settings

- TX Enable TX enabled
- DAC A Complement Not complement
- DAC B Complement Not complement
- DAC Current Control: 15
- Trim Analog: 0

Digital Input Settings

- Binary Rep 2's comp
- IQ Swap Swapped
- Data Type IQ

SYNC Settings

- SYNC bit 0
- Sync on I or Q I
- Sync / Sleep / TX Enable Selection
- All controlled by SIF bit

Clock Settings

Clock Mode: Dual Input Clock

Trim CLK RC Filter: 0 1 2 3

Mixer/NCO Settings

- Mixer Enable Bypassed
- Mixer Gain x2
- Fdac (MHz): 61.44
- Frequency [MHz]: 5
- NCO: 349525340
- Phase: 0

Misc. Digital Signals

- Enable 4-pin SIF 4-pin mode disabled
- ALARM_SDO Enable Disabled
- Output MSB on ALARM No

QMC Settings (continued)

- Atest: Atest disabled
- Vihilo Disabled
- Sethld Disabled
- Fuse Trim Enable Disabled
- TITest Vol High
- TITest Voh Low
- Version: 2
- LVDS Clock Divider: /4

AFE7070 Register Data

x01 xC2 1100 0010

CDCM7005 Register Data

Reg	Value
00	0x005FF1F0
01	0x000002A1
02	0xD00000A2
03	0x00000007

Register Controls

- Send
- Read All
- Load Regs
- Save All Regs
- Save AFE Regs
- Save CDC Regs

AFE707xEVM GUI capture (CDCM7005)

The screenshot displays the AFE7070 GUI software control interface for the CDCM7005. The interface is organized into several functional areas:

- Advanced Options:** Includes settings for Programmable Delay (M and N), Lock (Digital/Manual), Lock Detect Cycle (64), Lock Window (±8ns), Fast Lock (mode off), Charge Pump (2.0mA), and PFD Pulse (+1.5ns). It also features checkboxes for various operational modes like Reset-(Off)/Hold (On), Power Dwn Mode, Frequency Hold-Over Fcn, Cycle Slip Mode, Preset CP to Vcc/2, Frequency Hold-Over Fcn1, Reset all Dividers, CP 3-State, and Hold Fcn always activated.
- Clock & PLL Options:** Contains Clock Settings (M & N Selection: Auto, Ref. Freq: 10 MHz, VCXO Freq: 983.04 MHz) and PLL Settings (M Divider: 125, N Divider: 1536, B_MUX: 1, Phase Shift: /16). The PLL Output section shows an Output Freq of 983.04 MHz.
- Output Options:** Configures four output channels (Y0-Y4). Y0 and Y2 are unused, while Y1, Y3, and Y4 are active. Each channel has a mode selector (e.g., LVCMO, LVPECL) and a 3-state control.
- AFE7070 Register Data:** A scrollable list of registers (x00-x13) with their values. Below it, a table shows CDCM7005 Register Data:

Reg	Value
00	0x005FF1F0
01	0x000002A1
02	0xD00000A2
03	0x00000077

At the bottom right, there are buttons for Register Controls: Send, Read All, Load Regs, Save All Regs, Save AFE Regs, and Save CDC Regs.

TSW1400 GUI capture (10MHz tone)

The screenshot shows the High Speed Data Converter Pro v1.43 GUI. The DAC section is active, displaying a 10MHz tone in the Time Domain and Frequency Domain. The Time Domain plot shows DAC Codes vs Samples, and the Frequency Domain plot shows dB Fs vs Frequency (Hz). The DAC section is highlighted with a red box, showing the following settings:

Preamble	Data Rate (SPS)	DAC Option	Active Channel	Enabled?
0	61.44M	2's Complement	Channel 1	<input checked="" type="checkbox"/>

The I/Q Multitone Generator section is also highlighted with a red box, showing the following settings:

Tone BW	#	Tone Center
1	1	10M

The 'Send' button is highlighted with a red box. The 'Generate Tone' button is also highlighted with a red box.

Transmit

Generate Tone

Spectrum Analyzer Screen

