INTERFACING OMAP L138 directly to HSDC EVM via uPP [1]

The OMAP L138 uPP interface:

- Supports data widths of 8 to 16 bits
- Has two data channels. Channels may be configured in either receive or transmit mode. The interface also supports two additional modes, duplex and data interleave modes.
- Clocking
    - Channel in Transmit mode
        - When a channel is in transmit mode a Transmit Clock must be provided. This clock is divided by 2 internally by a fixed divider.
        - There is also a user configurable divider which can be set to 1 to 16 to further divide the Transmit clock.
        - The maximum Transmit clock frequency for a channel in Transmit mode is 150MHz for SDR and 75MHz for DDR (this corresponds to a maximum sample rate of 75MHz (or 150MBps) for both SDR and DDR because of the fixed divide by 2).
        - The Transmit clock is output on the channel's CLOCK pin.
    - Channel in Receive mode
        - When a channel is configured in the receive mode an external clock must be provided to its CLOCK pin.
        - This clock is not divided internally and the maximum allowed frequency is 75MHz for SDR and 37.5MHz for DDR.
- Channel Control pins
    - Each data channel has four control pins namely START, ENABLE, WAIT and CLOCK
    - When in Transmit mode the control signals START, ENABLE and CLOCK are output pins and WAIT is an input pin. The WAIT control pin can be disabled through register setting.
    - When in Receive mode, START and ENABLE are input pins and may be disabled through register setting. CLOCK is an input pin and WAIT is an output pin.

Remarks: It should be possible to connect a CMOS output HSDC EVM directly to the OMAP L138 uPP if the registers of the later are configured appropriately.

The table below summarizes the pin out for OMAP L138:

PIN NAME	PIN NUMBER	
	channelB	channelA
ENABLE	64	69
START	76	65
CLOCK	78	67
WAIT	77	71
[0]	21	89
[1]	22	88
[2]	23	91
[3]	24	90
[4]	25	93
[5]	26	92
[6]	27	95
[7]	28	94
[8]	13	81
[9]	14	80
[10]	15	83
[11]	16	82
[12]	17	85
[13]	18	84
[14]	19	87
[15]	20	86

Reference:

"OMAP-L1x Processor Universal Parallel Port (uPP) User's Guide", Lit number: SPRUGJ5B, March 2010. Available: http://www.ti.com.