ADC08D1020 Board Schematic

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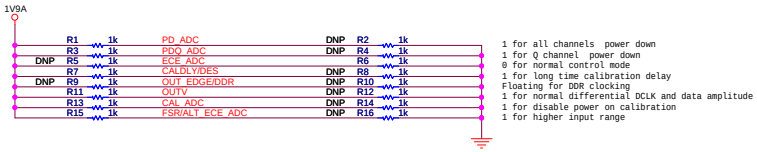
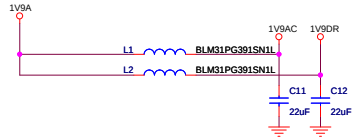
ADC08D1020

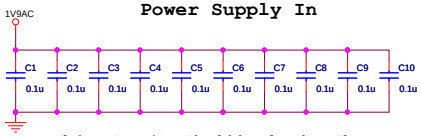
PLACE THESE RESISTORS TOGETHER AND ADD READABLE SILKSCREEN ON LAYOUT



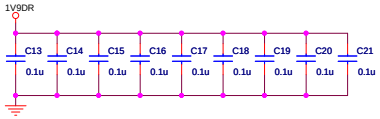
NOTE:ADC Is Initially In Power Down Mode(PD/PQ Pulled HIgh) And Calibration delayed(CAL_ADC Pulled High). When The FPGA Is Ready,It Can Begin The Power And The Calibration Process.



Power Supply In



A 0.1 µF Capacitor Should be Placed As Close As Possible To Each VA And VDR Pins.



NOTE:The Backside Pad Should Be Grounded For Best Performance.

The data output pins DID.

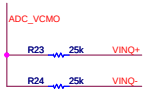
NOTE:All Differential Pairs Are Routed As 100 ohm Pairs (50 ohm individual impedance).

The data output pins DI.

The data output pins DQ.

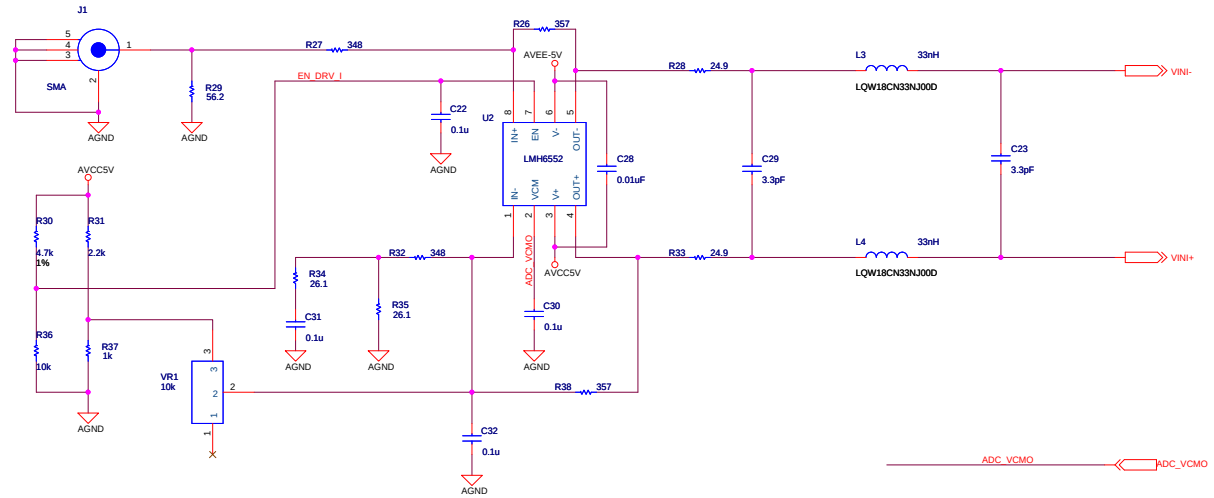
The data output pins DQD.

LAYOUT THE TRACE BETWEEN VINQ+/- IN AND VINQ+/- PIN GOES THROUGH R23 AND R24 PAD NEAR VINQ+/-

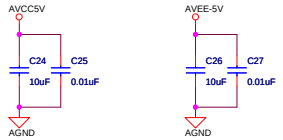


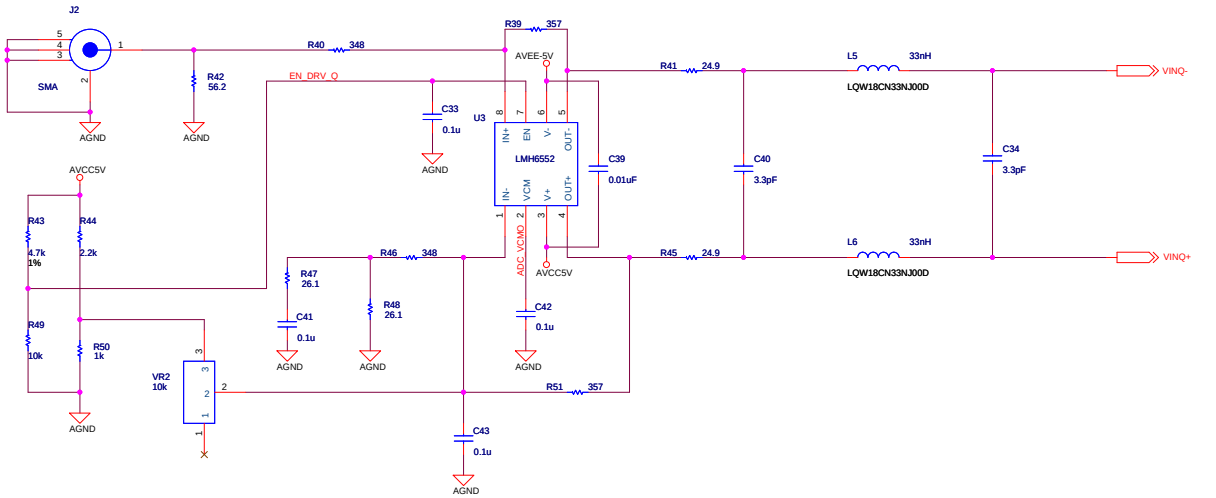
Unused Q anolog input bias to VCMO when the input in DC couple mode

FRONT END

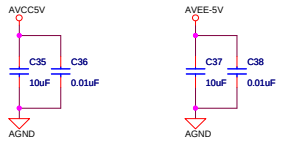


Place Closed To LMH6552 Power PINs

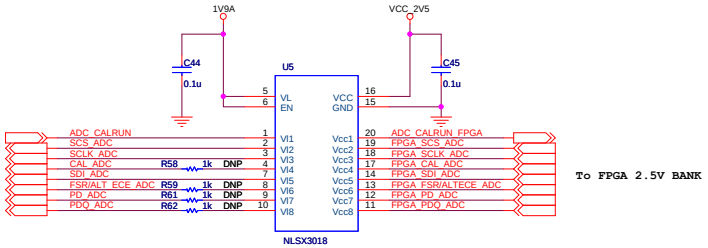




Place Closed To LMH6552 Power PINs

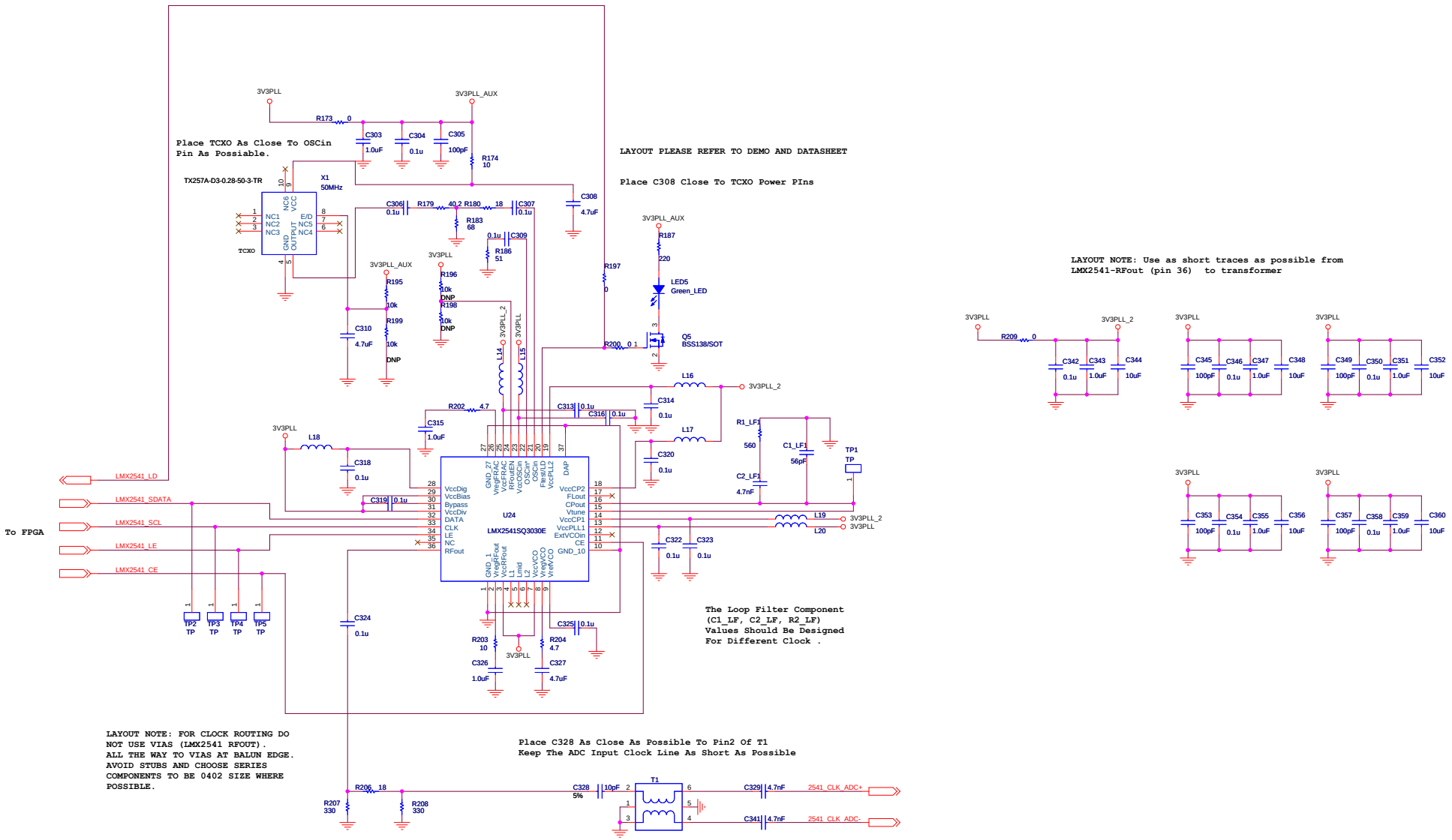


ADC Control Bus Transceiver

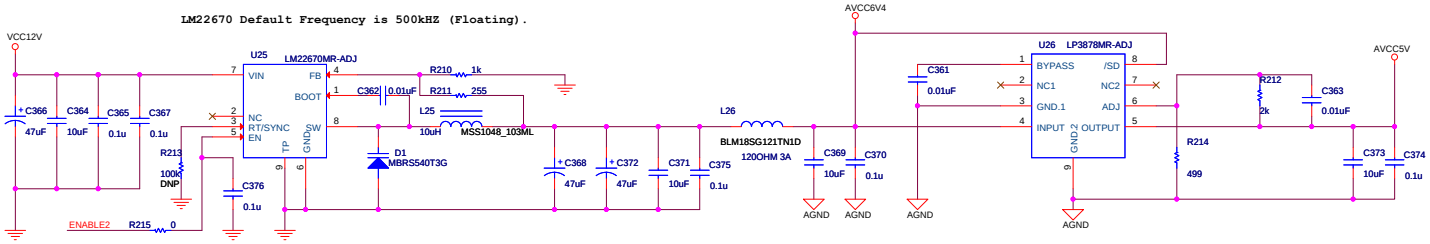


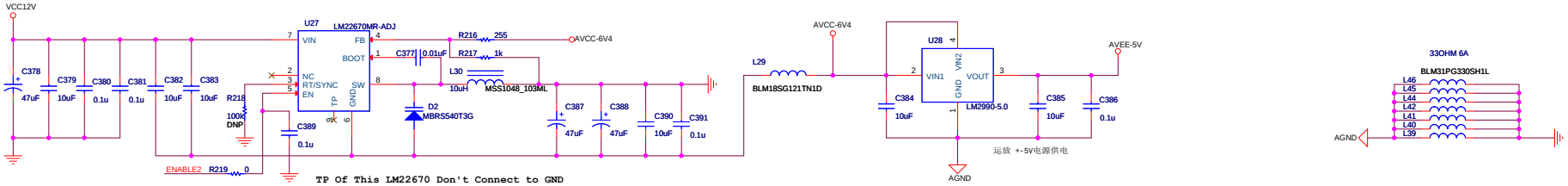
To FPGA 2.5V BANK

ADC PLL

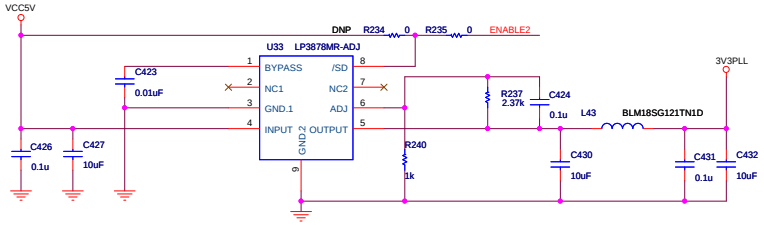

Place TCXO As Close To OSCin Pin As Possiable.
LAYOUT PLEASE REFER TO DEMO AND DATASHEET
Place C308 Close To TCXO Power PIns
LAYOUT NOTE: Use as short traces as possible from LMX2541-RFout (pin 36) to transformer
TX257A-D3-0.28-50-3-TR
X1
50MHz
TCXO
3V3PLL
3V3PLL_AUX
3V3PLL_2
U24
LMX2541SQ3030E
LED5
Green_LED
Q5
BSS138/SOT
TP1
TP
TP2
TP3
TP4
TP5
To FPGA
LMX2541_LD
LMX2541_SDATA
LMX2541_SCL
LMX2541_LE
LMX2541_CE
The Loop Filter Component (C1_LF, C2_LF, R2_LF) Values Should Be Designed For Different Clock .
LAYOUT NOTE: FOR CLOCK ROUTING DO NOT USE VIAS (LMX2541 RFOUT). ALL THE WAY TO VIAS AT BALUN EDGE. AVOID STUBS AND CHOOSE SERIES COMPONENTS TO BE 0402 SIZE WHERE POSSIBLE.
Place C328 As Close As Possible To Pin2 Of T1
Keep The ADC Input Clock Line As Short As Possible
T1
2541_CLK_ADC+
2541_CLK_ADC-

+5V,-5V - Amplifier Board and LMH6552 Analog Power

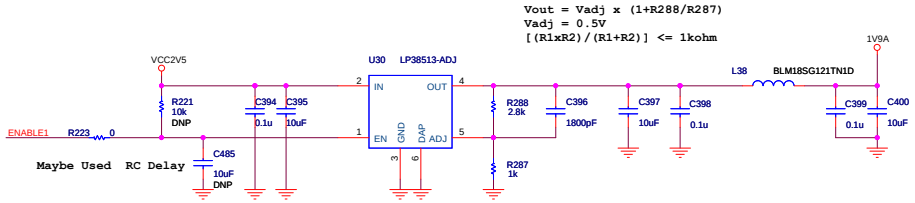




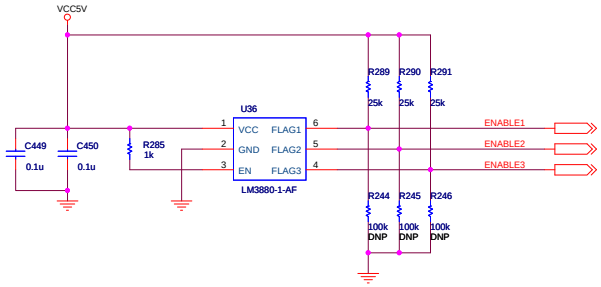
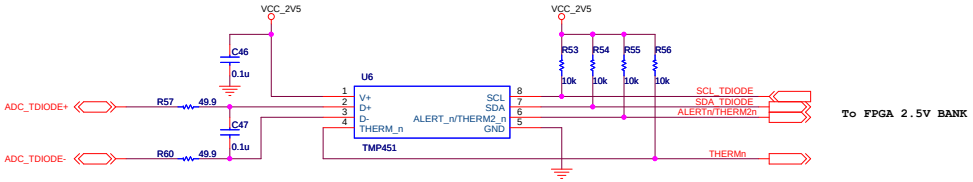
3V3_PLL - PLL Power Supply



1V9A - ADC Supply



Power Sequence Control



ADC Temperature Sensor