Integrated Power Management Unit Top Specification

Check for Samples: TPS659110, TPS659112, TPS659113

FEATURES

The purpose of the TPS65911 device is to provide the following resources:

- **Embedded power controller (EPC) with EEPROM programmability**
- **Two efficient step-down DCDC converters for processor cores (VDD1, VDD2)**
- **One efficient step-down DCDC converter for I/O power (VIO)**
- **One controller for external FETs (VDDCtrl)**
- **Dynamic voltage scaling for processor cores**
- **Eight LDO voltage regulators and one RTC LDO (supply for internal RTC)**
- **One high-speed I^2C interface for general-purpose control commands (CTL-I^2C)**
- **Two independent enable signals for controlling power resources (EN1, EN2). Alternatively, these pins can be used as a high-speed I^2C interface dedicated for voltage scaling for VDD1 and VDD2.**
- **Thermal shutdown protection and hot-die detection**
- **A real-time clock (RTC) resource with:**
  - **Oscillator for 32.768-kHz crystal or 32-kHz built-in RC oscillator**
  - **Date, time and calendar**
  - **Alarm capability**
- **Nine configurable GPIOs with multiplexed feature support:**
  - **Four can be used as enable for external resources, included into power up sequence and controlled by state-machine.**
  - **As GPI, GPIOs support logic-level detection and can generate maskable interrupt for wake-up.**
  - **Two of the GPIOs have 10 mA current sink capability for driving LEDs.**
  - **DCDCs switching synchronization through an external 3-MHz clock.**
- **Two reset inputs, for cold reset (HDRST) and a power initialization reset (PWRDN) for thermal reset input**
- **32-kHz clock and reset (NRESPWRON) for system and an additional output for reset signal**
- **Watchdog**
- **Two ON/OFF LED pulse generators and one PWM generator**
- **Two comparators for system control, connected to VCCS pin**
- **A JTAG® and boundary scan, but not accessible in functional mode (test purpose)**

APPLICATIONS

- **Portable and handheld systems**

DESCRIPTION

The TPS65911 is an integrated Power Management IC available in 98-pin 0.65-mm pitch BGA package and dedicated to applications powered by one Li-Ion or Li-Ion polymer battery cell or 3-series Ni-MH cells or a 5 V input, and which require multiple power rails. The device provides three step-down converters, one controller for external FETs to support high current rail, eight LDOs, and is designed to be flexible PMIC for supporting different processors and applications.

Two of the step-down converters provide power for dual processor cores and support dynamic voltage scaling by a dedicated I^2C interface for optimum power savings. The third converter provides power for the I/Os and memory in the system.

The device includes eight general-purpose LDOs providing a wide range of voltage and current capabilities. Five of the LDOs support 1.0 to 3.3 V with 100-mV step and three (LDO1, LDO2, LDO4) support 1.0 to 3.3 V with 50-mV step. All LDOs are fully controllable by the I^2C interface.

In addition to the power resources, the device contains an EPC to manage the power sequencing requirements of systems and an RTC. Power sequencing is programmable by EEPROM.

Figure 1 shows the top-level diagram of the device.

PRODUCT PREVIEW

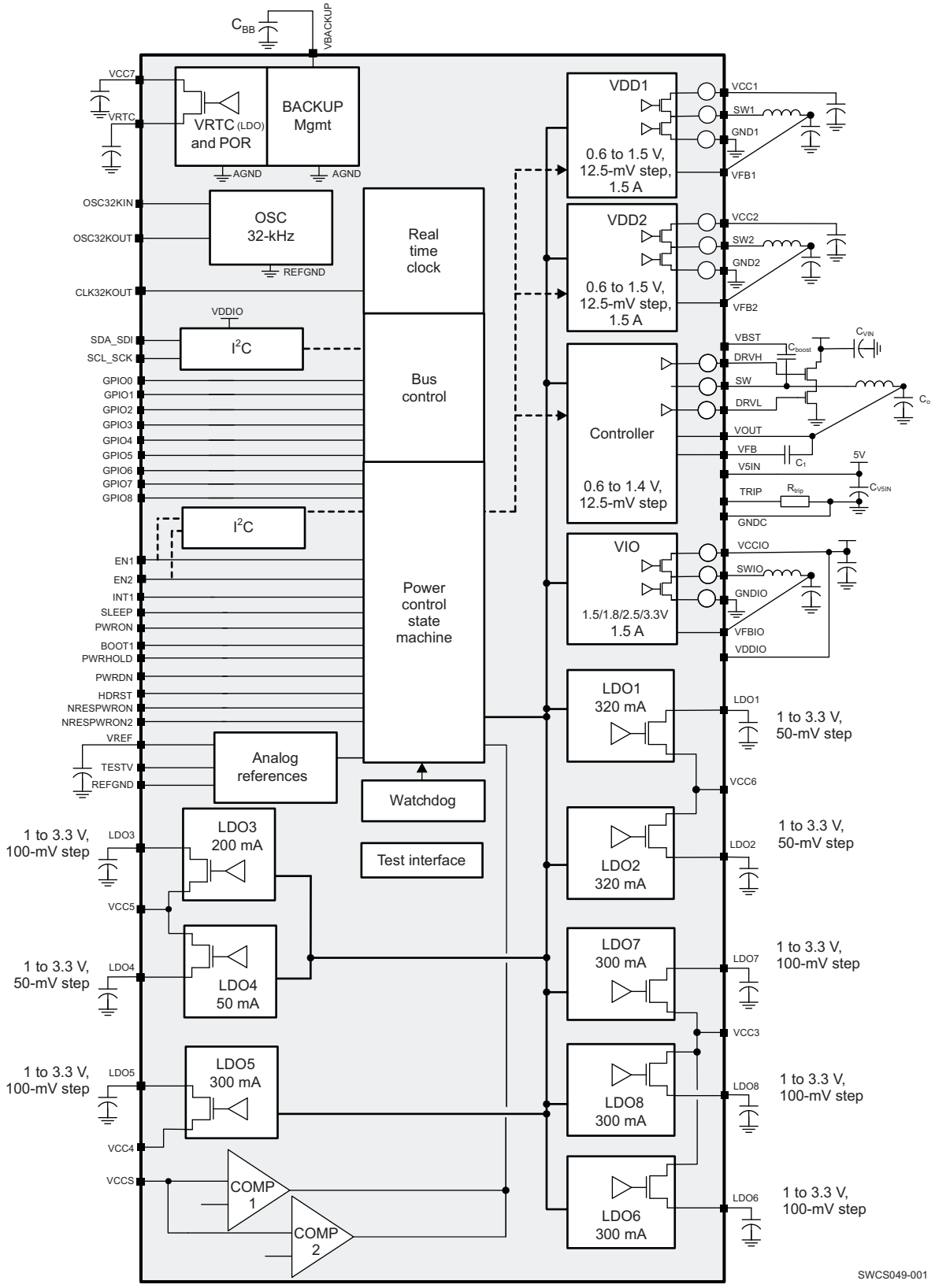

Figure 1. Top-Level Diagram

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated below are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The absolute maximum ratings for the TPS65911 device, over operating free-air temperature range (unless otherwise noted), are listed below.

PARAMETER	MIN	MAX	UNIT
Voltage range on pins/balls VCC1, VCC2, VCCIO, VCC3, VCC4, VCC5, VCC7, V5IN, TRIP	–0.3	7	V
Voltage range on pins/balls VCC6	–0.3	3.6	V
Voltage range on pins/balls VBST	–0.3	37	V
Voltage range on pins/balls SW	–5	30	V
Voltage range on pins/balls SW1, SW2, SWIO	–0.3	7	V
Voltage range on pins/balls VFB1,VFB2,VFBIO	–0.3	3.6	V
Voltage range on pins/balls VOUT, VFB	–0.3	7	V
Voltage range on pins/balls OSC32KIN,OSC32KOUT, BOOT1	–0.3	VRTCMAX + 0.3	V
Voltage range on pins/balls SDA_SDI, SCL_SCK, EN2, EN1, SLEEP, INT1, CLK32KOUT, NRESPWRON	–0.3	VDDIOMAX + 0.3	V
Voltage range on pins/balls PWRON	–0.3	7	V
Voltage range on pins/balls PWRHOLD, GPIO0	–0.3	7	V
Voltage range on balls GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8 (1)	–0.3	7	V
Voltage range on balls HDRST	–0.3	VRTCMAX + 0.3	V
Voltage range on balls NRESPWRON2 (1)	–0.3	7	V
Voltage range on ball PWRDN (2)	–0.3	7	V
Voltage range on ball VCCS	–0.3	7	V
Functional junction temperature range	–45	150	°C
Peak output current on all other terminals than power resources	–5.0	5.0	mA

(1) I/O supplied from VRTC but which can be driven from VCC7 or to VCC7 voltage level.
(2) Input supplied from VRTC but can be driven from VCC7 voltage level.

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RECOMMENDED OPERATING CONDITIONS

Lists of the recommended operating maximum ratings, over operating free-air temperature range (unless otherwise noted), for the TPS65911 device are given below.
Note: VCC7 should be connected to highest supply that is connected to device VCCx pin.
Exception: VCC4, VCC5, and V5IN inputs can be higher than VCC7. VCCS can be higher than VCC7 if VMBBUF_BYPASS = 0 (buffer is enabled).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range on pins/balls VCC1, VCC2, VCCIO, VCC5, VCC7, VCCS		2.7	3.8	5.5	V
Input voltage range on pins/balls VCC3, VCC4		1.7	3.8	5.5	V
Input voltage range on pins/balls VCC6		1.4	3.3	3.6	V
Input voltage range on pin/ball V5IN		4.5		6.5	V
Input voltage range on pin/ball VBST		-0.1		34.5	V
Input voltage range on pin/ball SW (<30% of repetitive period)		-1		28	V
Input voltage range on pin/ball TRIP, VFB		-0.1		6.5	V
Input voltage range on pins/balls PWRON		0	3.8	5.5	V
Input voltage range on pins/balls SDA_SDI, SCL_SCK, EN2, EN1, SLEEP, INT1, CLK32KOUT		1.65	VDDIO	3.45	V
Input voltage range on pins/balls PWRHOLD, HDRTS		1.65	VRTC	5.5	V
Input voltage range on balls GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, PWRDN		1.65	VRTC	5.5	V
Input voltage range on ball VCCS		0		5.5	V
Ambient temperature range		–40	27	85	°C
Junction temperature Tj		–40	27	125	°C
Storage temperature range		–65	27	150	°C
Lead temperature (soldering, 10 sec)			260		°C

EXTERNAL COMPONENT RECOMMENDATION

For crystal oscillator components, see 32-kHz RTC CLOCK.
Note: VCC7 supply should have enough capacitance to quarantee that when supply is switched off, voltage will not fall at a rate faster than 10 mV/ms. This ensures that RTC domain data will be maintained

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Power References					
VREF filtering capacitor $C_{O(VREF)}$	Connected from VREF to REFGND		100		nF
VDD1 SMPS					
Input capacitor $C_{I(VCC1)}$	X5R or X7R dielectric		10		µF
Output filter capacitor $C_{O(VDD1)}$	X5R or X7R dielectric	4	10	12	µF
C_O filter capacitor ESR	f = 3 MHz		10	300	mΩ
Inductor $L_{O(VDD1)}$			2.2		µH
L_O inductor dc resistor DCR_L				125	mΩ
VDD2 SMPS					
Input capacitor $C_{I(VCC2)}$	X5R or X7R dielectric		10		µF
Output filter capacitor $C_{O(VDD2)}$	X5R or X7R dielectric	4	10	12	µF
C_O filter capacitor ESR	f = 3 MHz		10	300	mΩ
Inductor $L_{O(VDD2)}$			2.2		µH
L_O inductor dc resistor DCR_L				125	mΩ
VIO SMPS					

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EXTERNAL COMPONENT RECOMMENDATION (continued)

For crystal oscillator components, see 32-kHz RTC CLOCK.

Note: VCC7 supply should have enough capacitance to guarantee that when supply is switched off, voltage will not fall at a rate faster than 10 mV/ms. This ensures that RTC domain data will be maintained

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Input capacitor $C_{I(VCCIO)}$	X5R or X7R dielectric		10		µF
Output filter capacitor $C_{O(VIO)}$	X5R or X7R dielectric	4	10	12	µF
C_O filter capacitor ESR	f = 3 MHz		10	300	mΩ
Inductor $L_{O(VIO)}$			2.2		µH
L_O inductor dc resistor DCR_L				125	mΩ
VDDCtrl SMPS					
Input capacitor C_{VIN}			4 × 10		µF
High side drive boost capacitor C_{boost}			0.1		µF
Input capacitor for V5IN supply C_{V5IN}			1		µF
Output filter capacitor $C_{O(VDDCtrl)}$			330		µF
C_O Filter capacitor ESR			9	15	mΩ
Inductor $L_{O(VDDCtrl)}$			2.7		µH
L_O Inductor DC resistor DCR_L			20	TBD	mΩ
R_{trip}			40		kΩ
C_1			330		pF
FET FDMC7660					
LDO1					
Input capacitor $C_{I(VCC6)}$	X5R or X7R dielectric		4.7		µF
Output filtering capacitor $C_{O(LDO1)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
LDO2					
Output filtering capacitor $C_{O(LDO2)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
LDO3					
Input capacitor $C_{I(VCC5)}$	X5R or X7R dielectric		4.7		µF
Output filtering capacitor $C_{O(LDO3)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
LDO4					
Output filtering capacitor $C_{O(LDO4)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
LDO5					
Input capacitor $C_{I(VCC4)}$	X5R or X7R dielectric		4.7		µF
Output filtering capacitor $C_{O(LDO5)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
LDO6					
Input capacitor $C_{I(VCC3)}$	X5R or X7R dielectric		4.7		µF
Output filtering capacitor $C_{O(LDO6)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
LDO7					
Output filtering capacitor $C_{O(LDO7)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
LDO8					
Output filtering capacitor $C_{O(LDO8)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
VRTC LDO					

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EXTERNAL COMPONENT RECOMMENDATION (continued)

For crystal oscillator components, see 32-kHz RTC CLOCK.

Note: VCC7 supply should have enough capacitance to quarantee that when supply is switched off, voltage will not fall at a rate faster than 10 mV/ms. This ensures that RTC domain data will be maintained

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Input capacitor $C_{I(VCC7)}$	X5R or X7R dielectric		4.7		µF
Output filtering capacitor $C_{O(VRTC)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
Backup Battery					
Backup battery capacitor C_{BB}		5	10	2000	mF
Series resistors	5 to 15 mF	10		1500	Ω

ESD SPECIFICATIONS

TI standard specification for ESD over operating free-air temperature range (unless otherwise noted) is presented below.

ESD METHOD	STANDARD REFERENCE	PERFORMANCE	TI STANDARD REQUIREMENTS
Human body model (HBM)	EIA/JESD22-A114D	2000 V	2000 V
Charge device model (CDM)	EIA/JESD22-C101C	500 V	500 V

PRODUCT PREVIEW

I/O PULLUP AND PULLDOWN CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA_SDI, SCL_SCK, SDASR_EN2, SCLSR_EN1 external pullup resistor	Connected to VDDIO		1.2		kΩ
SDA_SDI, SCL_SCK, SDASR_EN2, SCLSR_EN1 Programmable pullup (DFT, default inactive)	Grounded, VDDIO = 1.8 V	–45%	8	+45%	kΩ
SLEEP, PWRHOLD, programmable pulldown (default active)	@ 1.8 V, VRTC = 1.8 V	2	4.5	10	µA
NRESPWRON, NRESPWRON2 pulldown	@ 1.8 V, VCC7 = 5.5 V, OFF state	2	4.5	10	µA
32KCLKOUT pulldown (disabled in ACTIVE-SLEEP state)	@ 1.8 V, VRTC = 1.8 V, OFF state	2	4.5	10	µA
PWRON programmable pullup (default active)	Grounded, VCC7 = 5.5 V	–40	–31	–15	µA
GPIO0-8 programmable pulldown (default active except GPIO0)	@ 1.8 V, VRTC = 1.8 V, OFF state	2	4.5	10	µA
GPIO0-8 external pullup resistor	Connected to VDDIO	–20%	120	+20%	kΩ
HDRST programmable pulldown (default active)	@ 1.8 V, VRTC = 1.8 V	2	4.5	10	µA

(1) The internal pullups on the CTL-I^2C and SR-I^2C balls are used for test purposes or when the SR-I^2C interface is not used. Discrete pullups to the VIO supply must be mounted on the board in order to use the I^2C interfaces. The internal I^2C pullups must not be used for functional applications

PRODUCT PREVIEW

DIGITAL I/O VOLTAGE ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Related I/Os: PWRON					
Low-level input voltage V_{IL}				0.3 x VBAT	V
High-level input voltage V_{IH}		0.7 x VBAT			V
Related I/Os: PWRHOLD, GPIO0-8, PWRDN					
Low-level input voltage V_{IL}				0.45	V
High-level input voltage V_{IH}		1.3		VBAT	V
Related I/Os: BOOT1					
Low level input – Impedence between BOOT1 and GND				10	kΩ
High level input – Impedence between BOOT1 and VRTC				10	kΩ
HiZ level input – Impedence between BOOT1 and GND		500			kΩ
Related I/Os: SLEEP					
Low-level input voltage V_{IL}				0.35 x VDDIO	V
High-level input voltage V_{IH}		0.65 x VDDIO			V
Related I/Os: HDRST					
Low-level input voltage V_{IL}				0.35 x VRTC	V
High-level input voltage V_{IH}		0.65 x VRTC			V
Related I/Os: NRESPWRON, INT1, 32KCLKOUT					
Low-level output voltage V_{OL}	I_{OL} = 100 µA			0.2	V
	I_{OL} = 2 mA			0.45	V
High-level output voltage V_{OH}	I_{OH} = 100 µA	VDDIO – 0.2			V
	I_{OH} = 2 mA	VDDIO – 0.45			V
RELATED I/O'S: GPIO0 (PUSH-PULL MODE)					
Low-level output voltage V_{OL}	I_{OL} = 100 µA			0.2	V
	I_{OL} = 2 mA			0.45	V
High-level output voltage V_{OH}	I_{OH} = 100 µA	VCC7 – 0.2			V
	I_{OH} = 2 mA	VCC7 – 0.45			V
Related Open-Drain I/Os: GPIO0, GPIO2, GPIO4-8, NRESPWRON2					
Low-level output voltage V_{OL}	I_{OL} = 100 µA			0.2	V
	I_{OL} = 2 mA			0.45	V
RELATED OPEN-DRAIN I/O'S: GPIO1, GPIO3					
Low-level output voltage V_{OL}	I_{OL} = 100 µA			0.2	V
	I_{OL} = 2 mA			0.4	V
I^2C-Specific Related I/Os: SCL, SDA, EN1, EN2					
Low-level input voltage V_{IL}		–0.5		0.3 x VDDIO	V
High-level input voltage V_{IH}		0.7 x VDDIO			V
Hysteresis		0.1 x VDDIO			V
Low-level output voltage V_{OL} @ 3mA (sink current), VDDIO = 1.8 V				0.2 × VDDIO	V
Low-level output voltage V_{OL} @ 3mA (sink current), VDDIO = 3.3 V				0.4 x VDDIO	V

PRODUCT PREVIEW

I²C INTERFACE AND CONTROL SIGNALS

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER	TEST CONDITIONS(1)(2)	MIN	TYP	MAX
		INT1 rise and fall times, C_L = 5 to 35 pF	5	10	ns
		NRESPWRON rise and fall times, C_L = 5 to 35 pF	5	10	ns
SLAVE HIGH–SPEED MODE					
		SCL/EN1 and SDA/EN2 rise and fall time, C_L = 10 to 100 pF	10	80	ns
		Data rate		3.4	Mbps
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	10		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0	70	ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	160		ns
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	160		ns
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	160		ns
SLAVE FAST MODE					
		SCL/EN1 and SDA/EN2 rise and fall time, C_L = 10 to 400 pF	20 + 0.1 × C_L	250	ns
		Data rate		400	Kbps
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	100		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0	0.9	µs
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	0.6		µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	0.6		µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	0.6		µs
SLAVE STANDARD MODE					
		SCL/EN1 and SDA/EN2 rise and fall time, C_L = 10 to 400 pF		250	ns
		Data rate		100	Kbps
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	250		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0		µs
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	4.7		µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	4		µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	4		µs
SWITCHING CHARACTERISTICS					
SLAVE HIGH–SPEED MODE					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	160		ns
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	60		ns
SLAVE FAST MODE					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	1.3		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	0.6		µs
SLAVE STANDARD MODE					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	4		µs

(1) The input timing requirements are given by considering a rising or falling time of: 80 ns in high–speed mode (3.4 Mbps) 300 ns in fast–speed mode (400 kbps) 1000ns in Standard mode (100 kbps)
(2) SDA is SDA_SDI or EN2 signal, SCL is SCL_SCK or EN1 signal

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POWER CONSUMPTION

over operating free-air temperature range (unless otherwise noted)
All current consumption measurements are relative to the FULL chip, all VCC inputs set to VBAT voltage, COMP2 is off.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device BACKUP state	CK32K clock and RTC digital running (RTC_PWDN = 0)				µA
	VBAT = 2.4 V, VBACKUP = 0 V,		13	18	
	VBAT = 0 V, VBACKUP = 3.2 V, V5IN = 0 V		7	10	
Device OFF state	CK32K clock running, V5IN = 0				µA
	VBAT = 3.8 V		13	18	
	VBAT = 5 V		17	23	
	VBAT = 3.8 V, RTC digital running (RTC_PWDN = 0)		16	22	
	VBAT = 3.8 V, digital running (RTC_PWDN = 0), Backup Battery Charger on, VBACKUP= 3.2 V		26	32	
Device SLEEP state	VBAT = 3.8 V, CK32K clock running:				µA
	3 DCDCs on, 5 LDOs and VRTC on, no load		292		
	3 DCDCs on, 3 LDOs and VRTC on, no load		279		
	VBAT = 3.8 V, CK32K clock and RTC digital running (RTC_PWDN = 0):				
	3 DCDCs on, 5 LDOs and VRTC on, no load		295		
	Additional current from V5IN = 5 V, if VDDCtrl is on, no load		320	500	
Device ACTIVE state	VBAT = 3.8 V, CK32K clock running:				mA
	3 DCDCs on, 5 LDOs and VRTC on, no load		1.2		
	3 DCDCs on, 3 LDOs and VRTC on, no load		1.05		
	3 DCDCs on PWM mode (VDD1_PSKIP = VDD2_PSKIP = VIO_PSKIP = 0), 5 LDOs and VRTC on, no load		23.6		
	Additional current from V5IN = 5 V, if VDDCtrl is on, no load		0.32	0.5	

POWER REFERENCES AND THRESHOLDS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output reference voltage (VREF terminal)	Device in active or low-power mode	–1%	0.85	+1%	V
Main battery charged threshold VMBCH (programmable)	Measured on VCCS terminal Triggering monitored through NRESPRWON				V
	VMBCH_SEL=11000 to 11111		3.5		
	VMBCH_SEL=10111		3.45		
	...		...		
	VMBCH_SEL=01110	–2%	3	+2%	
	...		...		
	VMBCH_SEL=00101		2.55		
	VMBCH_SEL=00001 to 00100		2.5		
	VMBCH_SEL= 00000		bypassed		
Main Battery Charged Hysteresis Threshold VMBDCH	Measured on VCCS terminal		VMBCH – 100 mV		V

PRODUCT PREVIEW

POWER REFERENCES AND THRESHOLDS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Main battery discharged threshold VMBDCH2 (programmable)	Measured on VCC7 terminal (MTL prg) Triggering monitored through INT1				V
	VMBDCH2_SEL=11000 to 11111		3.5		
	VMBDCH2_SEL=10111		3.45		
	...		...		
	VMBDCH2_SEL=01110	–2%	3	+2%	
	...		...		
	VMBDCH2_SEL=00101		2.55		
	VMBDCH2_SEL=00001 to 00100		2.5		
	VMBDCH2_SEL= 00000		bypassed		
Main Battery DisCharged Hysteresis Threshold VMBCH2	Measured on VCCS terminal		VMBDCH2 – 100 mV		V
Main battery low threshold VMBLO	measured on VCC7 terminal (monitored on terminal NRESPWRON)	2.5	2.6	2.7	V
(MB comparator)	MTL programmation	2.4	2.5	2.6	
Main battery high threshold VMBHI	VBACKUP = 0 V, Measured on terminal VCC7 (MB comparator)	2.6	2.75	3	V
	VBACKUP = 3.2 V, Measured on terminal VCC7 (trigger monitored though VCCS Idd, UPR comparator)	2.5	2.55	3	
Main battery not present threshold VBNPR	Measured on terminal VCC7 (Triggering monitored on terminal VRTC)	1.9	2.1	2.2	V
Ground current (analog references + comparators + backup battery switch)	V_{CCx} = VBAT = 3.8 V except VCC6 = 3.6 V				µA
	Device in OFF state		8		
	Device in ACTIVE or SLEEP state		15		
	COMP2 consumption when enabled		5		
	Buffer consumption if COMP1 or COMP2 is active and buffer enabled		8		

PRODUCT PREVIEW

THERMAL MONITORING AND SHUTDOWN

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hot-die temperature rising threshold	THERM_HDSEL[1:0] = 00	113	117	136	°C
	THERM_HDSEL[1:0] = 01		121		
	THERM_HDSEL[1:0] = 10		125		
	THERM_HDSEL[1:0] = 11		130		
Hot-die temperature hysteresis			10		°C
Thermal shutdown temperature rising threshold		136	148	160	°C
Thermal shutdown temperature hysteresis			10		°C
Ground current	Device in ACTIVE state, Temp = 27°C, VCC7 = 3.8 V		6		µA

32-kHz RTC CLOCK

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLK32KOUT rise and fall time	C_L = 35 pF			10	ns
Bypass Clock (OSC32KIN: input, OSC32KOUT floating)					
Input bypass clock frequency	OSCKIN input		32		kHz
Input bypass clock duty cycle	OSCKIN input	40%		60%	
Input bypass clock rise and fall time	10% – 90%, OSC32KIN input		10	20	ns
CLK32KOUT duty cycle	Logic output signal	40%		60%	
Bypass clock setup time	32KCLKOUT output			1	ms
Ground current	Bypass mode			1.5	µA
Crystal oscillator (connected from OSC32KIN to OSC32KOUT)					
Crystal frequency	@ specified load cap value		32.768		kHz
Crystal tolerance	@ 27°C	–20	0	20	ppm
Frequency temperature coefficient.	Oscillator contribution (not including crystal variation)	–0.5		0.5	ppm/ºC
Secondary temperature coefficient		–0.04	–0.035	–0.03	ppm/ºC^2
Voltage coefficient		–2		2	ppm/V
Max crystal series resistor	@ Fundamental frequency			90	kΩ
Crystal load capacitor	According to crystal data sheet	6		12.5	pF
Load crystal oscillator Coscin ,Coscout	parallel mode Including parasitic PCB capacitor	12		25	pF
Quality factor		8000		80000	
Oscillator startup time	On power on			2	s
Ground current			1.5		µA
RC oscillator (OSC32KIN: grounded, OSC32KOUT floating)					
Output frequency	CK32KOUT output		32		kHz
Output frequency accuracy	@ 25°C	–15%	0%	+15%	
Cycle jitter (RMS)	Oscillator contribution			+10%	
Output duty cycle		+40%	+50%	+60%	
Settling time				150	µs
Ground current	Active @ fundamental frequency		4		µA

PRODUCT PREVIEW

BACKUP BATTERY CHARGER

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Backup battery charging current	VBACKUP = 0 to 2.8 V, BBCHEN = 1	350	650	900	µA
End-of-charge backup battery voltage	VCC5 = 3.6 V, $I_{VBACKUP}$ = –10 µA, BBSEL = 10	–3%	3.15	+3%	V
	VCC5 = 3.6 V, $I_{VBACKUP}$ = –10 µA, BBSEL = 00	–3%	3	+3%	
	VCC5 = 3.6 V, $I_{VBACKUP}$ = –10 µA, BBSEL = 01	–3%	2.52	+3%	
	VCC5 = 3.6 V, $I_{VBACKUP}$ = –10 µA, BBSEL = 11	VBAT – 0.3 V		VBAT	
	VCC5 = 3.0 V, $I_{VBACKUP}$ = –10 µA, BBSEL = 10	VBAT – 0.2 V		VBAT	
Ground current	On mode		10		µA

VRTC LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage V_{IN}	On mode	2.5		5.5	V
	Backup mode	1.9		3	
DC output voltage V_{OUT}	On mode, 3.0 V < V_{IN} < 5.5 V	1.78	1.83	1.88	V
	Backup mode, 2.3 V ≤ V_{IN} ≤ 2.6 V	1.72	1.78	1.84	
Rated output current I_{OUTmax}	On mode	20			mA
	Backup mode	0.1			
DC load regulation	On mode, I_{OUT} = I_{OUTmax} to 0			100	mV
	Backup mode, I_{OUT} = I_{OUTmax} to 0			100	
DC line regulation	On mode, V_{IN} = 3.0 V to V_{INmax} @ I_{OUT} = I_{OUTmax}			2.5	mV
	Backup mode, V_{IN} = 2.3 V to 5.5 V @ I_{OUT} = I_{OUTmax}			100	
Transient load regulation	On mode, V_{IN} = V_{INmin} + 0.2 V to V_{INmax} I_{OUT} = I_{OUTmax}/2 to I_{OUTmax} in 5 µs and I_{OUT} = I_{OUTmax} to I_{OUTmax}/2 in 5 µs			50 (1)	mV
Transient line regulation	On mode, V_{IN} = V_{INmin} + 0.5 V to V_{INmin} in 30 µs And V_{IN} = V_{INmin} to V_{INmin} + 0.5 V in 30 µs, I_{OUT} = I_{OUTmax}/2			25 (1)	mV
Turn-on time	I_{OUT} = 0, V_{IN} rising from 0 up to 3.6 V, @ V_{OUT} = 0.1 V up to V_{OUTmin}		2.2		ms
Ripple rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+} = V_{INmin} + 0.1 V to V_{INmax} @ I_{OUT} = I_{OUTmax}/2				dB
	f = 217 Hz		55		
	f = 50 kHz		35		
Ground current	Device in ACTIVE state		23		µA
	Device in BACKUP or OFF state		3		

(1) These parameters are not tested. They are used for design specification only.

PRODUCT PREVIEW

VIO SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCCIO and VCC7) V_{IN}	V_{OUT} = 1.5 V, 1.8 V, or 2.5 V	2.7		5.5	V
	V_{OUT} = 3.3 V	V_{OUT}		5.5	
DC output voltage (V_{OUT})	PWM mode (VIO_PSKIP = 0) or pulse skip mode I_{OUT} = 0 to I_{MAX}				V
	VSEL=00	–3%	1.5	+3%	
	VSEL = 01	–3%	1.8	+3%	
	VSEL = 10	–3%	2.5	+3%	
	VSEL = 11	–3%	3.3	+3%	
	Power down		0		
Rated output current I_{OUTmax}		1500			mA
P-channel MOSFET	V_{IN} = V_{INmin}		300		mΩ
On-resistance $R_{DS(ON)\_PMOS}$	V_{IN} = 3.8 V		250	400	
P-channel leakage current I_{LK_PMOS}	V_{IN} = V_{INMAX}, SWIO = 0 V			2	µA
N-channel MOSFET	V_{IN} = V_{MIN}		300		mΩ
On-resistance $R_{DS(ON)\_NMOS}$	V_{IN} = 3.8 V		250	400	
N-channel leakage current I_{LK_NMOS}	V_{IN} = V_{INmax}, SWIO = V_{INmax}			2	µA
PMOS current limit (high-side)	V_{IN} = V_{INmin} to V_{INmax} source current load				mA
	ILMAX = 00	1800			
	ILMAX = 01	900			
NMOS current limit (low-side)	V_{IN} = V_{INmin} to V_{INmax} source current load				mA
	ILMAX = 00	1800			
	ILMAX = 01	900			
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}			20	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			20	mV
Transient load regulation	V_{IN} = 3.8 V, V_{OUT} = 1.8 V			50	mV
	I_{OUT} = 0 to 500 mA , Max slew = 100 mA/µs				
	I_{OUT} = 700 to 1200 mA , Max slew = 100 mA/µs				
t on, off to on	I_{OUT} = 200 mA		350		µs
Overshoot	SMPS turned on		3%		
Power-save mode Ripple voltage	PFM (Pulse skip mode) mode, I_{OUT} = 1 mA		0.025 × V_{OUT}		V_{PP}
Switching frequency		2.7	3	3.3	MHz
Duty cycle				100%	
Minimum On Time $T_{ON(MIN)}$ P-channel MOSFET			35		ns
VFBIO internal resistance		0.5	1		MΩ
Ground current (I_Q)	Off			1	µA
	PWM mode, I_{OUT} = 0 mA, V_{IN} = 3.8 V, VIO_PSKIP = 0		7500		
	PFM (Pulse Skipping) mode, no switching, 3-MHz clock on		250		
	Low-power (pulse skipping) mode, no switching				
	ST[1:0]=11		63		
Conversion efficiency	PWM mode, DCR_L < 50 mΩ, V_{OUT} = 1.8 V, V_{IN} = 3.6 V:				
	I_{OUT} = 10 mA		40%		
	I_{OUT} = 100 mA		83%		

PRODUCT PREVIEW

VIO SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	I_{OUT} = 400 mA		85%		
	I_{OUT} = 800 mA		80%		
	I_{OUT} = 1200 mA		75%		
	I_{OUT} = 1500 mA		71%		
	PFM mode, DCR_L < 50 mΩ, V_{OUT} = 1.8 V, V_{IN} = 3.6 V:				
	I_{OUT} = 1 mA		68%		
	I_{OUT} = 10 mA		80%		
	I_{OUT} = 400 mA		85%		

PRODUCT PREVIEW

VDD1 SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC1 and VCC7) V_{IN}	V_{OUT} ≤ 2.7 V	2.7		5.5	V
	V_{OUT} > 2.7 V	V_{OUT}		5.5	
DC output voltage (V_{OUT})	VGAIN_SEL = 00, I_{OUT} = 0 to I_{OUTmax}:				
	max programmable voltage, SEL[6:0] = 1001011		1.5		
		–3%	1.2	+3%	V
	min programmable voltage, SEL[6:0] = 0000011		0.6		
	SEL[6:0] = 000000: power down		0		
	VGAIN_SEL = 10, SEL = 0101011 = 43, I_{OUT} = 0 to I_{OUTmax}	–3%	2.2	+3%	V
	VGAIN_SEL = 11, SEL = 0101000 = 40, I_{OUT} = 0 to I_{OUTmax}	–3%	3.2	+3%	V
DC output voltage programmable step ($V_{OUTSTEP}$)	VGAIN_SEL = 00, 72 steps		12.5		mV
Rated output current I_{OUTmax}		1500			mA
P-channel MOSFET	V_{IN} = V_{INmin}		300		mΩ
On-resistance $R_{DS(ON)\_PMOS}$	V_{IN} = 3.8 V		250	400	
P-channel leakage current I_{LK_PMOS}	V_{IN} = V_{INmax}, SW1 = 0 V			2	µA
N-channel MOSFET	V_{IN} = V_{MIN}		300		mΩ
On-resistance $R_{DS(ON)\_NMOS}$	V_{IN} = 3.8 V		250	400	
N-channel leakage current I_{LK_NMOS}	V_{IN} = V_{INmax}, SW1 = V_{INmax}			2	µA
PMOS current limit (high-side)	V_{IN} = V_{INmin} to V_{INmax}	1800			mA
NMOS current limit (low-side)	V_{IN} = V_{INmin} to V_{INmax}, source current load	1800			mA
	V_{IN} = V_{INmin} to V_{INmax}, sink current load	1800			
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}			20	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			20	mV
Transient load regulation	V_{IN} = 3.8 V, V_{OUT} = 1.2 V				
	I_{OUT} = 0 to 500 mA , Max slew = 100 mA/µs			50	mV
	I_{OUT} = 700 mA to 1.2A , Max slew = 100 mA/µs				
t on, off to on	I_{OUT} = 200 mA		350		µs
Output voltage transition rate	From V_{OUT} = 0.6 V to 1.5 V and V_{OUT} = 1.5 V to 0.6 V I_{OUT} = 500 mA				
	TSTEP[2:0] = 001		12.5		
	TSTEP[2:0] = 011 (default)		7.5		mV/µs
	TSTEP[2:0] = 111		2.5		
Overshoot	SMPS turned on		3%		
Power-save mode ripple voltage	PFM (pulse skip mode), I_{OUT} = 1 mA		0.025 × V_{OUT}		V_{PP}
Switching frequency		2.7	3	3.3	MHz
Duty cycle				100%	
Minimum on time $t_{ON(MIN)}$ P-channel MOSFET			35		ns
VFB1 internal resistance		0.5	1		MΩ

PRODUCT PREVIEW

VDD1 SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ground current (I_Q)	Off			1	µA
	PWM mode, I_{OUT} = 0 mA, V_{IN} = 3.8 V, VDD1_PSKIP = 0		7500		
	Pulse skipping mode, no switching		78		
	Low-power (pulse skipping) mode, no switching ST[1:0] = 11		63		
Conversion efficiency	PWM mode, DCR_L < 0.1 Ω, V_{OUT} = 1.2 V, V_{IN} = 3.6 V:				
	I_{OUT} = 10 mA		35%		
	I_{OUT} = 100 mA		78%		
	I_{OUT} = 400 mA		80%		
	I_{OUT} = 800 mA		74%		
	I_{OUT} = 1500 mA		62%		
	PFM mode, DCR_L < 0.1Ω, V_{OUT} = 1.2 V, V_{IN} = 3.6 V:				
	I_{OUT} = 1 mA		59%		
	I_{OUT} = 10 mA		70%		
	I_{OUT} = 400 mA		80%		

PRODUCT PREVIEW

VDD2 SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC2 and VCC7) V_{IN}	V_{OUT} ≤ 2.7 V	2.7		5.5	V
	V_{OUT} > 2.7 V	V_{OUT}		5.5	
DC output voltage (V_{OUT})	VGAIN_SEL = 00, I_{OUT} = 0 to I_{OUTmax}:				V
	max programmable voltage, SEL[6:0] = 1001011		1.5		
		–3%	1.2	+3%	
	min programmable voltage, SEL[6:0] = 0000011		0.6		
	SEL[6:0] = 000000: power down		0		
	VGAIN_SEL = 10, SEL = 0101011 = 43	–3%	2.2	+3%	
	VGAIN_SEL = 11, default, BOOT[1:0] = 00	–3%	3.3	+3%	
DC output voltage programmable step ($V_{OUTSTEP}$)	VGAIN_SEL = 00, 72 steps		12.5		mV
Rated output current I_{OUTmax}		1500			mA
P-channel MOSFET	V_{IN} = V_{INmin}		300		mΩ
On-resistance $R_{DS(ON)\_PMOS}$	V_{IN} = 3.8 V		250	400	
P-channel leakage current I_{LK_PMOS}	V_{IN} = V_{INmax}, SW2 = 0 V			2	µA
N-channel MOSFET	V_{IN} = V_{MIN}		300		mΩ
On-resistance $R_{DS(ON)\_NMOS}$	V_{IN} = 3.8 V		250	400	
N-channel leakage current I_{LK_NMOS}	V_{IN} = V_{INmax}, SW2 = V_{INmax}			2	µA
PMOS current limit (high-side)	V_{IN} = V_{INmin} to V_{INmax}, source current load	1800			mA
NMOS current limit (low-side)	V_{IN} = V_{INmin} to V_{INmax}, source current load	1800			mA
	V_{IN} = V_{INmin} to V_{INmax}, sink current load	1800			
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}			20	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			20	mV
Transient load regulation	V_{IN} = 3.8 V, V_{OUT} = 1.2 V				mV
	I_{OUT} = 0 to 500 mA , Max slew = 100 mA/µs			50	
	I_{OUT} = 700 mA to 1.2 A , Max slew = 100 mA/µs				
t on, Off to on	I_{OUT} = 200 mA		350		µs
Output voltage transition rate	From V_{OUT} = 0.6 V to 1.5 V and V_{OUT} = 1.5 V to 0.6 V I_{OUT} = 500 mA				mV/µs
	TSTEP[2:0] = 001		12.5		
	TSTEP[2:0] = 011 (default)		7.5		
	TSTEP[2:0] = 111		2.5		
Overshoot	SMPS turned on		3%		
Power-save mode ripple voltage	PFM (pulse skip mode), I_{OUT} = 1 mA		0.025 × V_{OUT}		V_{PP}
Switching frequency		2.7	3	3.3	MHz
Duty cycle				100%	
Minimum On time P-Channel MOSFET			35		ns
VFB2 internal resistance		0.5	1		MΩ
Ground current (I_Q)	Off			1	µA
	PWM mode, I_{OUT} = 0 mA, V_{IN} = 3.8 V, VDD2_PSKIP = 0		7500		
	PFM (pulse skipping) mode, no switching		78		
	Low-power (pulse skipping) mode, no switching ST[1:0] = 11		63		
	PWM mode, DCR_L < 50 mΩ, V_{OUT} = 1.2 V, V_{IN} = 3.6 V:				

PRODUCT PREVIEW

VDD2 SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion efficiency	I_{OUT} = 10 mA		35%		
	I_{OUT} = 100 mA		78%		
	I_{OUT} = 400 mA		80%		
	I_{OUT} = 800 mA		74%		
	I_{OUT} = 1200 mA		66%		
	I_{OUT} = 1500 mA		62%		
	PFM mode, DCR_L < 50 mΩ, V_{OUT} = 1.2 V, V_{IN} = 3.6 V:				
	I_{OUT} = 1 mA		59%		
	I_{OUT} = 10 mA		70%		
	I_{OUT} = 400 mA		80%		
	PWM mode, DCR_L < 50 mΩ, V_{OUT} = 3.3 V, V_{IN} = 5 V:				
	I_{OUT} = 10 mA		39%		
	I_{OUT} = 100 mA		85%		
	I_{OUT} = 400 mA		91%		
	I_{OUT} = 800 mA		90%		
	I_{OUT} = 1200 mA		86%		
	I_{OUT} = 1500 mA		84%		
	PFM mode, DCR_L < 50 mΩ, V_{OUT} = 3.3 V, V_{IN} = 5 V:				
	I_{OUT} = 1 mA		80%		
	I_{OUT} = 10 mA		82%		
	I_{OUT} = 400 mA		92%		

PRODUCT PREVIEW

VDDCtrl SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage for external FETs V_{IN}		3		25	V
Input voltage V5IN		4.5		5.5	V
DC output voltage (V_{OUT})	IOUT=0 to IOUTmax : max programmable voltage: SEL[6:0]=1000011 to 1111111 ... SEL[6:0]=0110001 ... min programmable voltage: SEL[6:0]=0000001 to 0000011 SEL[6:0]=000000: power down		 1.4 1.2 0.6 0		V
DC Output Voltage programmable step ($V_{OUTSTEP}$)			12.5		mV
Rated output current I_{OUTmax}				6000	mA
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}			20	mV
DC line regulation	On mode, VI_N = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			20	mV
Transient load regulation	VIN =12v, VOUT=1.2v I_{OUT} = 250 to 3250 mA, Max slew = 3 A/µs I_{OUT} = 3250 to 250 mA , Max slew = 3 A/µs		 –25 25		mV
t on, off to on	From EN high to V_{out} = 95%		900		µs
Output voltage transition rate	From V_{OUT} = 0.6 V to 1.4 V and V_{OUT} = 1.4 V to 0.6 V I_{OUT} = 500 mA		100(1)		mV/20 µs
Overshoot/Undershoot	Percentage of target value		5%		
Switching frequency	I_{OUT} = 100 mA I_{OUT} = 1 A I_{OUT} = 5 A		10 100 340		kHz
Ground current (I_Q)	Off No load		 400	1 500	µA
Conversion efficiency	V_{IN} = 12 V, V_{OUT} = 1.2 V I_{OUT} = 250 mA I_{OUT} = 1 A I_{OUT} = 6 A		 47% 89% 80%		

(1) 100 mV/20 µs reached with 50 mV/10 µs steps

PRODUCT PREVIEW

LDO1 AND LDO2

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC6) V_{IN}	V_{OUT}(LDO1) = 1.05 V @ 320 mA and V_{OUT}(LDO2) = 1.05 V @ 160 mA	1.4		3.6	V
	V_{OUT}(LDO1) = 1.2 V/1.5 V @ 100 mA and V_{OUT}(LDO2) = 1.2 V/1.1 V/1.0 V	1.7		3.6	
	V_{OUT}(LDO1) = 1.5 V and V_{OUT} (LDO1, LDO2) = 1.8 V @ 200 mA	2.1		3.6	
	V_{OUT}(LDO1) = 1.8 V and V_{OUT}(LDO2) = 1.8 V	2.7		3.6	
	V_{OUT}(LDO1) = 2.7 V	3.2		3.6	
	V_{OUT} (LDO1) = V_{OUT}(LDO2) = 3.3 V	3.5		3.6	
LDO1					
DC output voltage V_{OUT}	ON and Low-power mode, V_{IN} = V_{INmin} to V_{INmax} (V_{INmax} 3.6 V)	–3%	1 1.05 ... 3.25 3.3	+3%	
Rated output current I_{OUTmax}	On mode	320			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, V_{OUT} = V_{OUTmin} – 100 mV	450	600	1000	mA
Dropout voltage V_{DO}	ON mode, V_{DO} = V_{IN} – V_{OUT}, V_{IN} = 1.4 V, I_{OUT} = I_{OUTmax}			350	mV
DC load regulation	On mode, I_{OUT} = I_{OUTmax} to 0			12	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			1	mV
Transient load regulation	ON mode, V_{IN} = 1.5 V, V_{OUT} = 1.05 V I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs and I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs		20	40	mV
Transient line regulation	On mode, V_{IN} = 2.7 + 0.5 V to 2.7 in 30 µs, and V_{IN} = 2.7 to 2.7 + 0.5 V in 30 µs, I_{OUT} = I_{OUTmax}		5	10	mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}	50	75	100	µs
	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmax}	200	300	420	
Turn-on inrush current			300	600	mA
Ripple rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+}= 1.8 V, I_{OUT} = I_{OUTmax}/2				dB
	f = 217 Hz		70		
	f = 20 kHz		40		
LDO1 internal resistance	LDO off		600		Ω
Ground current	On mode, I_{OUT} = 0		63	75	µA
	On mode, I_{OUT} = I_{OUTmax}			2000	
	Low-power mode		22	20	
	Off mode (max 85°C)			2.7	
LDO2					
DC output voltage V_{OUT}	On and low-power mode, V_{IN} = V_{INmin} to V_{INmax} (V_{INmax} = 3.6 V)	–3%	1 1.05 ... 3.25 3.3	+3%	

PRODUCT PREVIEW

LDO1 AND LDO2 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rated output current I_{OUTmax}	On mode	320			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} – 100$ mV	450	600	1000	mA
Dropout voltage V_{DO}	ON mode, $V_{DO} = V_{IN} – V_{OUT}$, $V_{IN} = 1.4$ V, $I_{OUT} = I_{OUTmax}$			350	mV
DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$ to 0			12	mV
DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} @ $I_{OUT} = I_{OUTmax}$			1	mV
Transient load regulation	ON mode, $V_{IN} = 1.5$ V, $V_{OUT} = 1.05$ V $I_{OUT} = 0.1 \times I_{OUTmax}$ to $0.9 \times I_{OUTmax}$ in 5 µs and $I_{OUT} = 0.9 \times I_{OUTmax}$ to $0.1 \times I_{OUTmax}$ in 5 µs		20	40	mV
Transient line regulation	On mode, $V_{IN} = 2.7 + 0.5$ V to 2.7 in 30 µs, And $V_{IN} = 2.7$ to $2.7 + 0.5$ V in 30 µs, $I_{OUT} = I_{OUTmax}$		5	10	mV
Turn-on time	$I_{OUT} = 0$, @ $V_{OUT} = 0.1$ V up to V_{OUTmin}	40	75	100	µs
	$I_{OUT} = 0$, @ $V_{OUT} = 0.1$ V up to V_{OUTmax}	200	300	420	
Turn-on inrush current			300	600	mA
Ripple rejection	$V_{IN} = V_{INDC} + 100$ mV_{pp} tone, $V_{INDC+} = 1.8$ V, $I_{OUT} = I_{OUTmax}/2$				dB
	f = 217 Hz		70		
	f = 20 kHz		40		
LDO2 internal resistance	LDO off		600		Ω
Ground current	On mode, $I_{OUT} = 0$		63	75	µA
	On mode, $I_{OUT} = I_{OUTmax}$			2000	
	Low-power mode		22	20	
	Off mode (max 85°C)			2.7	

PRODUCT PREVIEW

LDO3 AND LDO4

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC5) V_{IN}	V_{OUT} (LDO3) = 1.8 V and V_{OUT} (LDO4) = 1.8 V/ 1.1 V/ 1.0 V	2.7		5.5	V
	V_{OUT} (LDO3) = 2.6 V and V_{OUT} (LDO4) = 2.5 V	3.0		5.5	
	V_{OUT} (LDO3) = 2.8 V	3.2		5.5	
LDO3					
DC output voltage V_{OUT}	On and low-power mode, V_{OUT} = 1.0 – 3.3 V, V_{IN} = V_{INmin} to V_{INmax}	–3%	1 1.1 ... 3.2 3.3	+3%	V
Rated output current I_{OUTmax}	On mode	200			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, V_{OUT} = V_{OUTmin} – 100 mV	400	550	650	On mode, V_{OUTtyp} = 2.8 V, V_{DO} = V_{IN} - V_{OUT}, mA
Dropout Voltage V_{DO}	On mode, V_{OUTtyp} = 3.3 V, V_{DO} = V_{IN} – V_{OUT}, V_{IN} = 3.6 V, I_{OUT} = I_{OUTmax}		150	250	mV
DC load regulation	On mode, I_{OUT} = I_{OUTmax} to 0			10	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			1	mV
Transient load regulation	On mode, V_{IN} = 2.7 V, V_{OUTtyp} = 1.8 V I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs and I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs		15	22	mV
Transient line regulation	On mode, V_{OUTtyp} = 1.8V, I_{OUT} = I_{OUTmax}, V_{IN} = V_{INmin} + 0.5 V to V_{INmin} in 30 µs and V_{IN} = V_{INmin} to V_{INmin} + 0.5 V in 30 µs, I_{OUT} = I_{OUTmax}		0.5	1	mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}	25	50	70	µs
	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmax}	120	180	230	
Turn-on inrush current			200	450	mA
Ripple Rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, I_{OUT} = I_{OUTmax}/2				dB
	f = 217 Hz		70		
	f = 50 kHz		40		
LDO3 internal resistance	LDO off		500		kΩ
Ground current	On mode, I_{OUT} = 0		65	76	µA
	On mode, I_{OUT} = I_{OUTmax}			2000	
	Low-power mode		14	22	
	Off mode			1	
LDO4					
DC output voltage V_{OUT}	On and low-power mode, V_{IN} = V_{INmin} to V_{INmax}	–3%	1 1.05 ... 3.25 3.3	+3%	V
Rated output current I_{OUTmax}	On mode	50			mA
	Low-power mode	1			

PRODUCT PREVIEW

LDO3 AND LDO4 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} - 100$ mV	200	400	500	mA
Dropout voltage V_{DO}	On mode, $V_{OUTtyp} = 2.5$ V, $V_{DO} = V_{IN} - V_{OUT}$ $V_{IN} = 3.6$ V, $I_{OUT} = I_{OUTmax}$		100	160	mV
DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$ to 0			5	mV
DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} @ $I_{OUT} = I_{OUTmax}$			1	mV
Transient load regulation	On mode, $V_{IN} = 2.7$ V, $V_{OUTtyp} = 1.8$ V $I_{OUT} = 0.1 \times I_{OUTmax}$ to $0.9 \times I_{OUTmax}$ in 5 µs and $I_{OUT} = 0.9 \times I_{OUTmax}$ to $0.1 \times I_{OUTmax}$ in 5 µs		6	10	mV
Transient line regulation	On mode, $V_{IN} = V_{INmin} + 0.5$ V to V_{INmin} in 30 µs and $V_{IN} = V_{INmin}$ to $V_{INmin} + 0.5$ V in 30 µs, $I_{OUT} = I_{OUTmax}/2$		0.2	1	mV
Turn-on time	$I_{OUT} = 0$, @ $V_{OUT} = 0.1$ V up to V_{OUTmin} $I_{OUT} = 0$, @ $V_{OUT} = 0.1$ V up to V_{OUTmax}	25 120	50 180	70 230	µs
Ripple rejection	$V_{IN} = V_{INDC} + 100$ mV_{pp} tone, $V_{INDC+} = 3.8$ V, $I_{OUT} = I_{OUTmax}/2$ f = 217 Hz f = 50 kHz		 70 40		dB
LDO4 internal resistance	LDO Off		500		kΩ
Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode Off mode		55 14	65 900 17 1	µA

PRODUCT PREVIEW

LDO5

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC4) V_{IN}	V_{OUT} (LDO5) = 1.8 V	2.7		5.5	V
	V_{OUT} (LDO5) = 2.5 V	3.2		5.5	
	V_{OUT} (LDO5) = 2.8 V @ I_{load} = 200 mA	3.2		5.5	
	V_{OUT} (VAUX2) = 2.8 V @ 300 mA	3.2		5.5	
LDO5					
DC output voltage V_{OUT}	On and low-power mode, V_{OUT} = 1.0 – 3.3 V, V_{IN} = V_{INmin} to V_{INmax}	–3%	1 1.1 ... 3.2 3.3	+3%	V
Rated output current I_{OUTmax}	On mode	300			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, V_{OUT} = V_{OUTmin} – 100 mV	450	550	650	mA
Dropout voltage V_{DO}	On mode, V_{DO} = V_{IN} – V_{OUT},				mV
	V_{IN} = 2.7 V, I_{OUT} = I_{OUTmax}			500	
	V_{IN} = 2.7 V, I_{OUT} = 250 mA			400	
	V_{IN} = 2.7 V, I_{OUT} = 200 mA			300	
DC load regulation	On mode, I_{OUT} = I_{OUTmax} to 0			15	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUTmax}			1	mV
Transient load regulation	On mode, V_{IN} = 3.2 V, V_{OUTtyp} = 2.8 V I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs and I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs		16	30	mV
Transient line regulation	On mode, V_{IN} = V_{INmin} + 0.5 V to V_{INmin} in 30 µs and V_{IN} = V_{INmin} to V_{INmin} + 0.5 V in 30 µs, I_{OUT} = I_{OUTmax}		4	12	mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}	20	50	70	µs
	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmax}	120	180	250	
Turn-on inrush current			200	450	mA
Ripple Rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, I_{OUT} = I_{OUTmax}/2				dB
	f = 217 Hz		70		
	f = 20 kHz		40		
LDO5 internal resistance	LDO Off		60		Ω
Ground current	On mode, I_{OUT} = 0		65	76	µA
	On mode, I_{OUT} = I_{OUTmax}			2000	
	Low-power mode		14	22	
	Off mode			1	

PRODUCT PREVIEW

LDO6, LDO7, AND LDO8

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC3) V_{IN}	V_{OUT}(LDO6) = 1.2 V @ 150 mA, V_{OUT}(LDO7) = 1.1 V @ 150 mA and (VLDO8) = 1 V @ 180 mA	1.7		5.5	V
	V_{OUT}(LDO7) = 1.8 V/2 V and V_{OUT}(LDO6) = 1.8 V	2.7		5.5	
	V_{OUT}(LDO7) = 2.8 V	3.2		5.5	
	V_{OUT}(LDO7) = 3.3 V	3.6		5.5	
	V_{OUT}(LDO7) = 2.8 V @ 250 mA	3.2		5.5	
	V_{OUT}(LDO7) = 3.0 V	3.6		5.5	
	V_{OUT}(LDO7) = 3.3 V @ 250 mA	3.6		5.5	
LDO6					
DC Output voltage V_{OUT}	On and low-power mode, V_{IN} = V_{INmin} to V_{INmax}	–3%	1 1.1 ... 3.2 3.3	+3%	V
Rated output current I_{OUTmax}	On mode	300			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, V_{OUT} = V_{OUTmin} – 100 mV	450	550	650	mA
Dropout Voltage V_{DO}	On mode, V_{DO} = V_{IN} – V_{OUT},				mV
	V_{IN} = 2.7 V, I_{OUT} = I_{OUTmax}			500	
	V_{IN} = 2.7 V, I_{OUT} = 250 mA			400	
	V_{IN} = 2.7 V, I_{OUT} = 200 mA			300	
	V_{IN} = 1.7 V, I_{OUT} = 180 mA			700	
	V_{IN} = 1.7 V, I_{OUT} = 150 mA			500	
	V_{IN} = 1.7 V, I_{OUT} = 100 mA			300	
DC load regulation	On mode, I_{OUT} = I_{OUTmin} to 0			15	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			1	mV
Transient load regulation	On mode, V_{IN} = 3.2 V, V_{OUTtyp} = 2.8 V I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs and I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs		20	32	mV
Transient line regulation	On mode, V_{IN} = 2.7 V + 0.5 V to 2.7 V in 30 µs and V_{IN} = 2.7 V to 2.7 V + 0.5 V in 30 µs, I_{OUT} = I_{OUTmax}		5	15	mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}	20	50	70	µs
	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmax}	120	180	250	
Turn-on Inrush current			200	450	mA
Ripple Rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, I_{OUT} = I_{OUTmax}/2				dB
	f = 217 Hz		70		
	f = 20 kHz		40		
LDO6 internal resistance	LDO off		60		Ω
Ground current	On mode, I_{OUT} = 0		65	76	µA
	On mode, I_{OUT} = I_{OUTmax}			2000	
	Low-power mode		14	22	
	Off mode			1	
LDO7					
DC output voltage V_{OUT}	On and low-power mode, V_{IN} = V_{INmin} to V_{INmax}		1		

PRODUCT PREVIEW

LDO6, LDO7, AND LDO8 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		–3%	1.1 ... 3.2 3.3	+3%	V
Rated output current I_{OUTmax}	On mode Low-power mode	300 1			mA
Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} – 100$ mV	450	550	650	mA
Dropout voltage V_{DO}	On mode, $V_{DO} = V_{IN} – V_{OUT}$, V_{IN} = 2.7 V, $I_{OUT} = I_{OUTmax}$ V_{IN} = 2.7 V, I_{OUT} = 250 mA V_{IN} = 2.7 V, I_{OUT} = 200 mA V_{IN} = 1.7 V, I_{OUT} = 180 mA V_{IN} = 1.7 V, I_{OUT} = 150 mA V_{IN} = 1.7 V, I_{OUT} = 100 mA			 500 400 300 700 500 300	mV
DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$ to 0			15	mV
DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} @ $I_{OUT} = I_{OUTmax}$			1	mV
Transient load regulation	On mode, V_{IN} = 3.6 V, V_{OUTtyp} = 3.3 V $I_{OUT} = 0.1 \times I_{OUTmax}$ to $0.9 \times I_{OUTmax}$ in 5 µs and $I_{OUT} = 0.9 \times I_{OUTmax}$ to $0.1 \times I_{OUTmax}$ in 5 µs		16	25	mV
Transient line regulation	On mode, $I_{OUT} = I_{OUTmax}/2$, V_{IN} = 2.7 + 0.5 V to 2.7 in 30 µs and V_{IN} = 2.7 V + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}/2$		5	15	mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}	20	50	70	µs
	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmax}	120	180	250	
Turn-on inrush current			200	450	mA
Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax}/2$ f = 217 Hz f = 20 kHz		 70 40		dB
LDO7 internal resistance	LDO off		60		Ω
Ground current	On mode, I_{OUT} = 0 On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode Off mode		65 14	76 2000 22 1	µA
LDO8					
DC output voltage V_{OUT}	On and low-power mode, $V_{IN} = V_{INmin}$ to V_{INmax}	–3%	1 1.1 ... 3.2 3.3	+3%	V
Rated output current I_{OUTmax}	On mode Low-power mode	300 1			mA
Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} – 100$ mV	450	550	650	mA

PRODUCT PREVIEW

LDO6, LDO7, AND LDO8 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout voltage V_{DO}	On mode, $V_{DO} = V_{IN} - V_{OUT}$,				
	V_{IN} = 2.7 V, $I_{OUT} = I_{OUTmax}$			500	
	V_{IN} = 2.7 V, I_{OUT} = 250 mA			400	
	V_{IN} = 2.7 V, I_{OUT} = 200 mA			300	mV
	V_{IN} = 1.7 V, I_{OUT} = 180 mA			700	
	V_{IN} = 1.7 V, I_{OUT} = 150 mA			500	
	V_{IN} = 1.7 V, I_{OUT} = 100 mA			300	
DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$ to 0			15	mV
DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} @ $I_{OUT} = I_{OUTmax}$			1	mV
Transient load regulation	On mode, V_{IN} = 1.7 V, V_{OUTtyp} = 1.2 V I_{OUT} = 10 mA to 90 mA in 5 µs and I_{OUT} = 90 mA to 10 mA in 5 µs		7	30	mV
Transient line regulation	On mode, I_{OUT} = 100 mA, V_{IN} = 2.7 V + 0.2 V to 2.7 V in 30 µs and V_{IN} = 2.7 V to 2.7 v + 0.2 V in 30 µs, I_{OUT} = 100 mA		5	15	mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}	20	50	70	µs
	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmax}	120	180	250	
Turn-on inrush current			200	450	mA
Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax}/2$				
	f = 217 Hz		70		dB
	f = 20 kHz		40		
LDO8 internal resistance	LDO off		60		Ω
Ground current	On mode, I_{OUT} = 0		65	76	µA
	On mode, $I_{OUT} = I_{OUTmax}$			2000	
	Low-power mode		14	22	
	Off mode			1	

SWITCH-ON/-OFF SEQUENCES AND TIMING

An example boot sequence is described in this chapter. TPS65911 supports one fixed boot sequence and one EEPROM programmable boot sequence. Boot mode selection is described in BOOT CONFIGURATION AND SWITCH-ON/-OFF SEQUENCES.

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SWITCH-ON/-OFF SEQUENCES AND TIMING (continued)

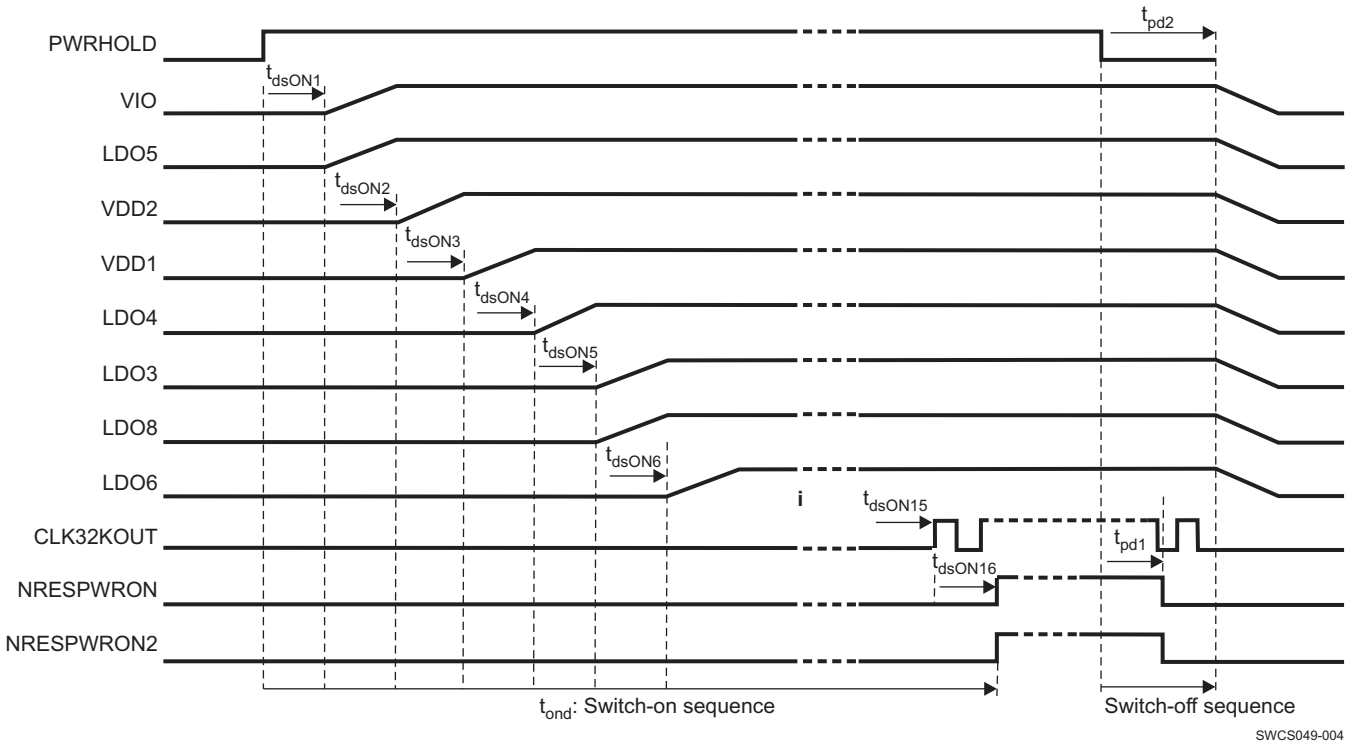


Figure 2. Boot Sequence Example with 2-ms Time Slot and Simultaneous Switch-Off of Resources

Table 1. Timing Characteristics for Boot Sequence Example

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dsON1}	PWRHOLD rising edge to VIO, LDO5 enable delay		66 × t_{CK32k} = 2060		µs
t_{dsON2}	VIO to VDD2 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON3}	VDD2 to VDD1 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON4}	VDD1 to LDO4 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON5}	LDO4 to LDO3, LDO8 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON6}	LDO3 to LDO6 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON7}	LDO6 to CLK32KOUT rising-edge delay		9 × 64 × t_{CK32k} = 18000		µs
t_{dsON8}	CLK32KOUT to NRESPWON, NRESPWON2 rising-edge delay		64 × t_{CK32k} = 2000		µs
t_{dsONT}	Total switch-on delay		32		ms
t_{dsOFF1}	PWRHOLD falling-edge to NRESPWON, NRESPWON2 falling-edge delay		2 × t_{CK32k} = 62.5		µs
$t_{dsOFF1B}$	NRESPWON falling-edge to CLK32KOUT low delay		3 × t_{CK32k} = 92		µs
t_{dsOFF2}	PWRHOLD falling-edge to supplies and reference disable delay		5 × t_{CK32k} = 154		µs

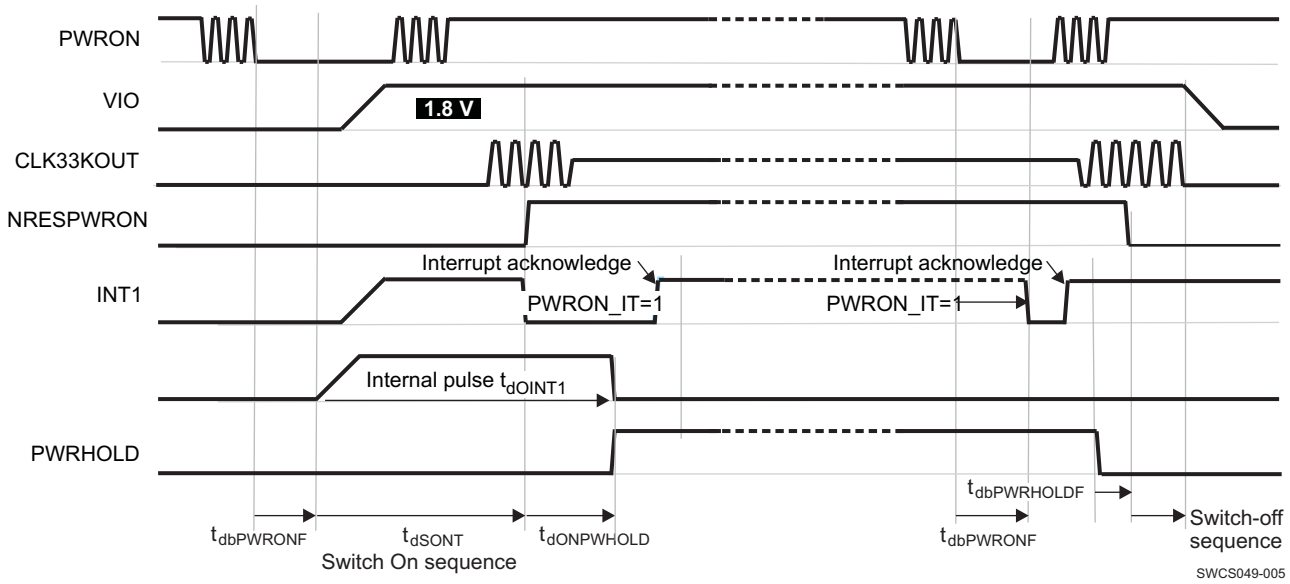
POWER CONTROL TIMING

Device State Control Through PWRON Signal

Figure 3 shows the device state control through PWRON signal.

PRODUCT PREVIEW

POWER CONTROL TIMING (continued)



NOTE: DEV_ON or AUTODEV_ON control bits can be used instead of PWRHOLD signal to maintain supplies on after switch-on sequence.

NOTE: Internal POWER ON enable condition pulse TdOINT1 keeps device active until PWRHOLD acknowledge.

Figure 3. Device State Control Through PWRON Signal

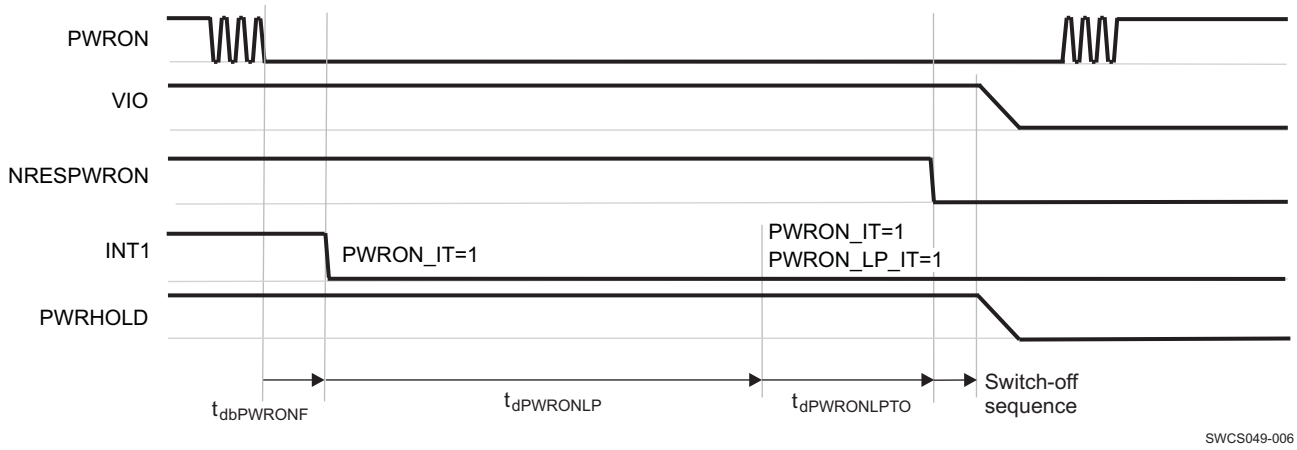


Figure 4. PWRON Long-Press Turn-Off

Table 2 lists the power control timing characteristics.

Table 2. Power Control Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dbPWRONF}$: PWRON falling-edge debouncing delay			100		µs
$t_{dbPWRONR}$: PWRON rising-edge debouncing delay			3 × t_{CK32k} = 94		µs
$t_{dbPWRHOLD}$: PWRON rising-edge debouncing delay			2 × t_{CK32k} = 63		µs
t_{dOINT1}: INT1 (internal) Power-on pulse duration after PWRON low-level (debounced) event			1		s

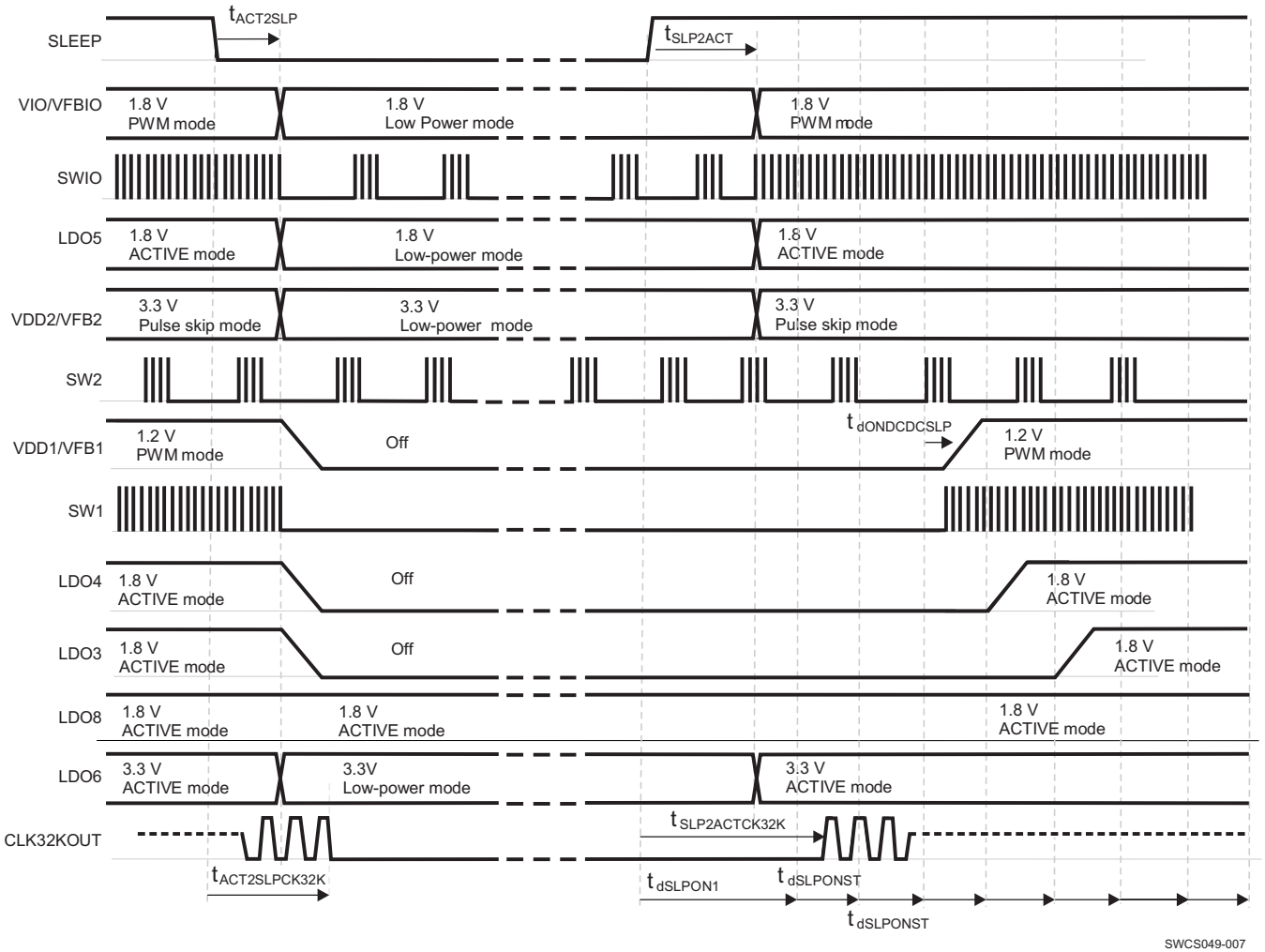
POWER CONTROL TIMING (continued)

Table 2. Power Control Timing Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dONPWHOLD}$: delay to set high PWRHOLD signal or DEV_ON control bit after NRESPWON released to keep on the supplies			$t_{dOINT1} - t_{DSONT} = 970$ (1)		ms
$t_{dPWRONLP}$: PWRON long-press delay	PWRON falling-edge to PWRON_LP_IT		4		s
$t_{dPWRONLPTO}$: PWROW long-press interrupt (PWRON_LP_IT) to supplies switch-off	PWRON_LP_IT to NRESPWRON falling-edge		1		s

(1) T_{dSONT} = 30 ms, as in example boot sequence.

Device SLEEP State Control



NOTE: Registers programming: VIO_PSKIP = 0, VDD1_PSKIP = 0, VDD1_SETOFF = 1, LDO3_SETOFF = 1, LDO4_SETOFF = 1, LDO8_KEEPON = 1.

Figure 5. Device SLEEP State Control

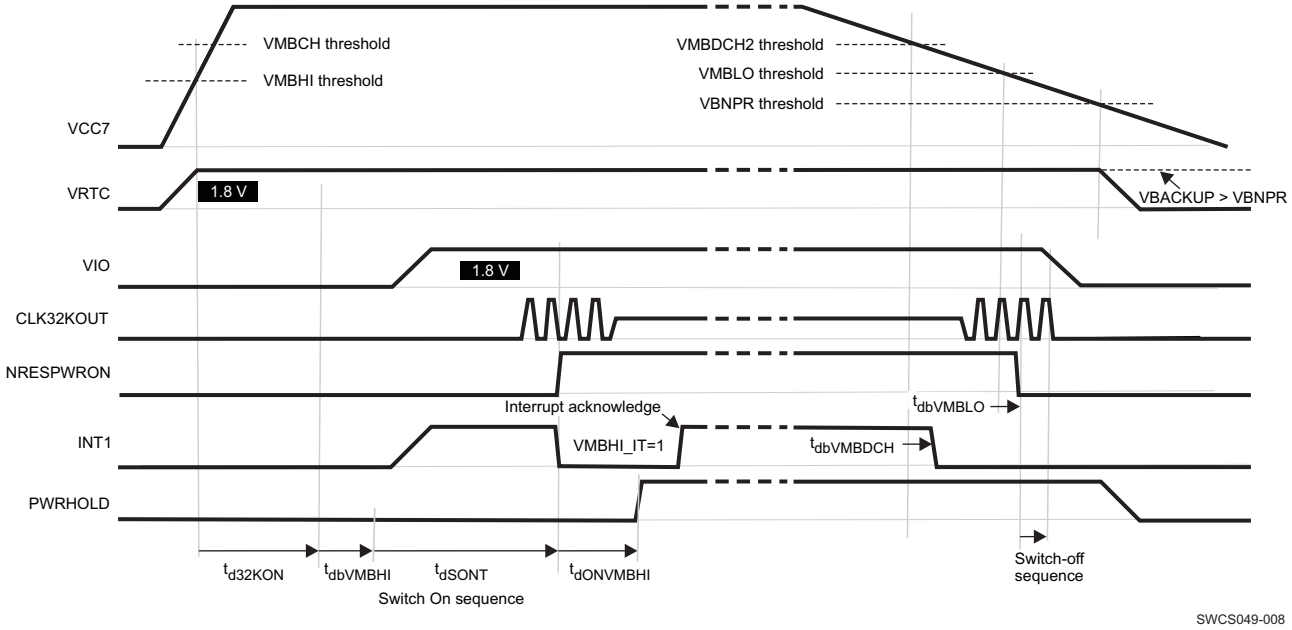
PRODUCT PREVIEW

Table 3. Device SLEEP State Control Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ACT2SLP}$	SLEEP falling-edge to supply n low-power mode (SLEEP resynchronization delay)	$2 \times t_{CK32k} = 62$		$3 \times t_{CK32k} = 94$	µs
$t_{ACT2SLP}$	SLEEP falling-edge to CLK32KOUT low	156	$t_{ACT2SLP} + 3 \times t_{CK32k}$	188	µs
$t_{SLP2ACT}$	SLEEP rising edge to supply in high-power mode	$8 \times t_{CK32k} = 250$		$9 \times t_{CK32k} = 281$	µs
$t_{SLP2ACTCK32K}$	SLEEP rising edge to CLK32KOUT running	344	$t_{SLP2ACT} + 3 \times t_{CK32k}$	375	µs
$t_{dSLPON1}$	SLEEP rising edge to time step 1 of the turn-on sequence from SLEEP state	281	$t_{SLP2ACT} + 1 \times t_{CK32k}$	312	µs
$t_{dSLPONST}$	turn-on sequence step duration, from SLEEP state				µs
	TSLOT_LENGTH[1:0] = 00		0		
	TSLOT_LENGTH[1:0] = 01		200		
	TSLOT_LENGTH[1:0] = 10		500		
	TSLOT_LENGTH[1:0] = 11		2000		
$t_{dSLPONDCDC}$	VDD1, VDD2, or VIO turn-on delay from turn-on sequence time step		$2 \times t_{CK32k} = 62$		µs

PRODUCT PREVIEW

Device Turn-On/Turn-Off with Rising/Falling Input Voltage



NOTE: To allow power-up from first supply insertion as shown here, VMBHI_IT_MSK is set to 0.

NOTE: Power-up to active state is enabled when VMBHI interrupt is not masked (VMBHI_IT_MSK in boot configuration).

NOTE: DEV_ON or AUTODEV_ON control bits can be used instead of PWRHOLD signal to maintain supplies on after switch-on sequence

Figure 6. Device Turn-On/Off with Rising/Falling Input Voltage

Table 4. Device Turn-On Voltage with Rising Input Voltage, Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d32KON}: 32-kHz oscillator turn-on time	RC oscillator Quartz oscillator bypass clock		0.1 200 0.1		ms
$t_{dbVMBHI}$: VMBHI rising-edge debouncing delay		$3 \times t_{CK32k} = 94$		$4 \times t_{CK32k} = 125$	µs
t_{dOINT1}: INT1 Power On pulse duration after VMBHI high level (debounced) event			1		s
$t_{dONVMBHI}$: delay to set high PWRHOLD signal or DEV_ON control bit after NRESPWRON released in order to keep on the supplies			$t_{dOINT1} - t_{DSONT} = 970$		ms
$t_{dbVMBDCH}$: Main Battery voltage = VMBDCH threshold to INT1 falling-edge delay		$3 \times t_{CK32k} = 94$		$4 \times t_{CK32k} = 125$	s
$t_{dbVMBLO}$: Main Battery voltage = VMBLO threshold to NRESPWRON falling-edge delay		$3 \times t_{CK32k} = 94$		$4 \times t_{CK32k} = 125$	s

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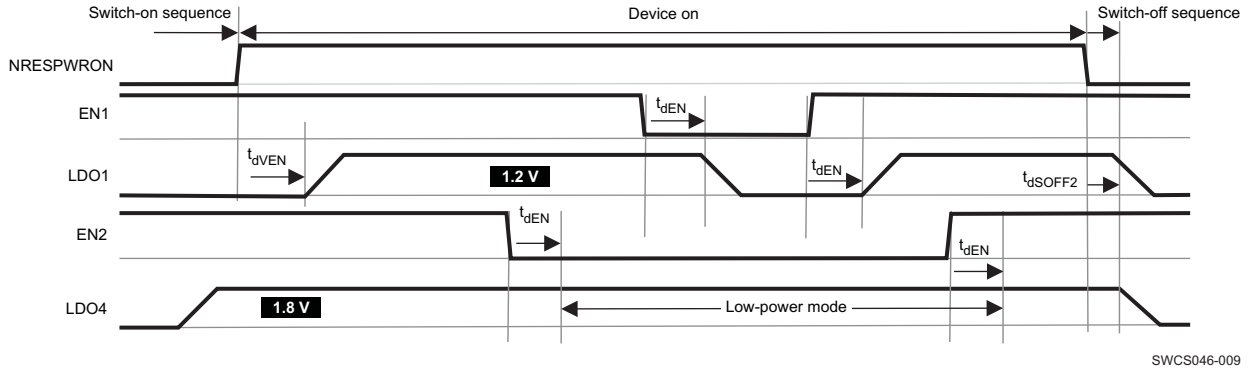
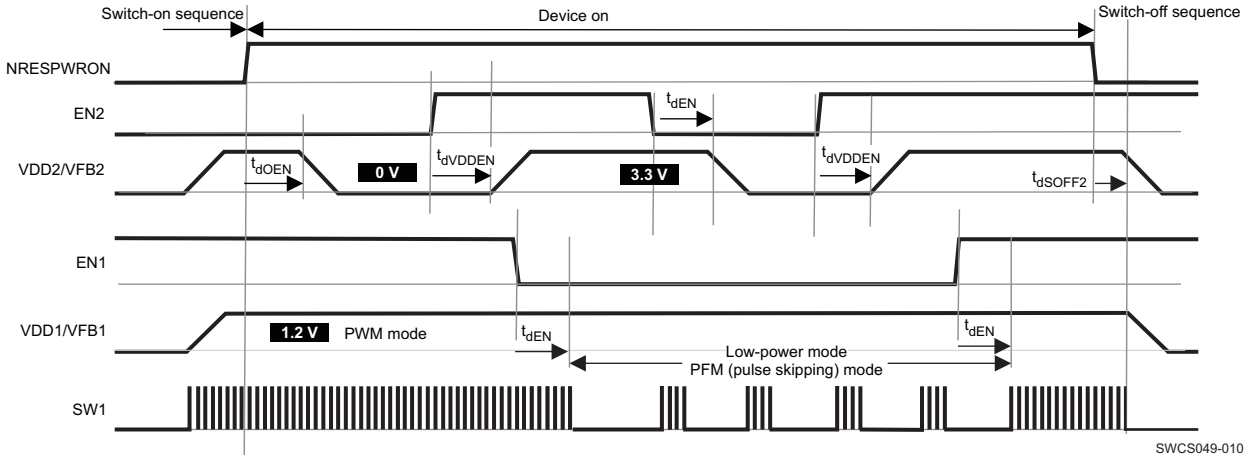
Power Supplies State Control Through EN1 and EN2 Signals



NOTE: Register setting: LDO1_EN1 = 1, LDO4_EN2 = 1, and LDO4_KEEPON = 1.

Figure 7. LDO Type Supplies State Control Through EN1 and EN2



NOTE: Register setting: VDD2_EN2 = 1, VDD1_EN1 = 1, VDD1_KEEPON = 1, VDD1_PSKIP = 0, and SEL[6:0] = hex00 in VDD2_SR_REG.

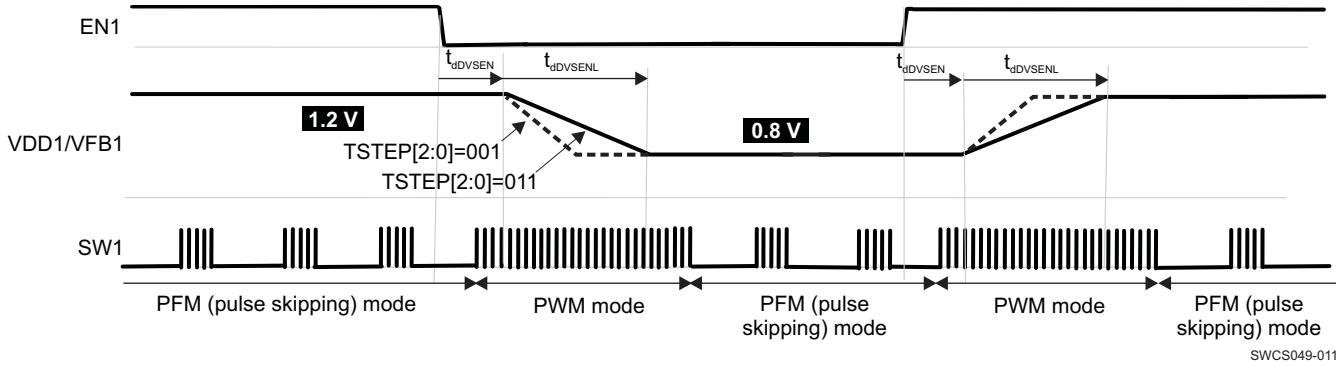
Figure 8. VDD1 and VDD2 Supplies State Control Through EN1 and EN2

Table 5. Supplies State Control Through EN1 and EN2 Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dEN}: NRESPWRON to to supply state change delay, EN1 or EN2 driven			0		ms
t_{dOEN}: EN1 or EN2 edge to supply state change delay			$1 \times t_{CK32k} = 31$		µs
t_{dVDDEN}: EN1 or EN2 edge to VDD1 or VDD2 DCDC turn on delay			$3 \times t_{CK32k} = 63$		µs

PRODUCT PREVIEW

VDD1, VDD2 Voltage Control Through EN1 and EN2 Signals



NOTE: Register setting: VDD1_EN1=1, SEL[6:0]=hex13 in VDD1_SR_REG

Figure 9. VDD1 Supply Voltage Control Through EN1

Table 6. VDD1 Supply Voltage Control Through EN1 Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dDVSEN}: EN1 (or EN2) edge to VDD1 (or VDD2) voltage change delay			2 × t_{CK32k} = 62		µs
$t_{dDVSENL}$: VDD1 (or VDD2) voltage settling delay	TSTEP[2:0] = 001		32		µs
	TSTEP[2:0] = 011 (default)		0.4/7.5 = 53		
	TSTEP[2:0] = 111		160		

PRODUCT PREVIEW

DEVICE INFORMATION

Table 7. TERMINAL FUNCTIONS

NAME	BGA PIN	SUPPLIES	TYPE	I/O	DESCRIPTION	PU / PD
VDDIO	N7	VDDIO/DGND	Power	I	Digital Ios supply	No
SDA_SDI	M5	VDDIO/DGND	Digital	I/O	I^2C bi-directional data signal / Serial Peripheral Interface Data Input (multiplexed)	External PU
SCL_SCK	M4	VDDIO/DGND	Digital	I/O	I^2C bi-directional clock signal / Serial Peripheral Interface Clock Input (multiplexed)	External PU
SLEEP	F1	VDDIO/DGND	Digital	I	ACTIVE-SLEEP state transition control signal	Programmable PD (default active)
PWRHOLD	N1	VRTC/DGND	Digital	I	Switch-on, switch off control signal / GPI	Programmable PD (default active)
PWRON	E4	VCC7/DGND	Digital	I	External switch-on control(ON button)	Programmable PU (default active)
NRESPWRON	C7	VDDIO/DGND	Digital	O	Power off reset	PD active during device OFF state
INT1	L3	VDDIO/DGND	Digital	O	Interrupt flag	No
NRESPWRON2	C7	VRTC/DGND	Digital	O, OD	2nd NRESPWRON output	PD active during device OFF state.External pullup in ACTIVE
BOOT1	J5	VRTC/DGND	Digital	I	Power-up sequence selection	No
CLK32KOUT	F4	VDDIO/DGND	Digital	O	32-kHz clock output	PD diseable in ACTIVE or SLEEP state
OSC32KIN	F8	VRTC/REFGND	Analog	I	32-kHz crystal oscillator	No
OSC32KOUT	F7	VRTC/REFGND	Analog	I	32-kHz crystal oscillator	No
VREF	G8	VCC7/REFGND	Analog	O	Bandgap voltage	No
REFGND	G7	REFGND	Analog	I/O	Reference ground	No
TESTV	B8	VCC7/AGND	Analog	O	Analog test output (DFT)	No
VBACKUP	D7	VBACKUP/AGND	Power	I	Backup Battery input	No
VCC1	E1	VCC1/GND1	Power	I	VDD1 DCDC power Input	No
GND1	C1	VCC1/GND1	Power	I/O	VDD1 DCDC Power ground	No
SW1	D2/D1/E2	VCC1/GND1	Power	O	VDD1 DCDC switched output	No
VFB1	D4	VCC7/DGND	Analog	I	VDD1 feedback voltage	PD 5uA
VCC2	G2/G1	VCC2/GND2	Power	I	VDD2 DCDC power Input	No
GND2	J2/J1	VCC2/GND2	Power	I/O	VDD2 DCDC Power ground	No
SW2	H2/H1	VCC2/GND2	Power	O	VDD2 DCDC switched output	No

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Table 7. TERMINAL FUNCTIONS (continued)

VFB2	K2	VCC7/DGND	Analog	I	VDD2 DCDC feedback voltage	PD 5uA
VCCIO	L7	VCCIO/GNDIO	Power	I	VIO DCDC power Input	No
GNDIO	J8	VCCIO/GNDIO	Power	I/O	VIO DCDC Power ground	No
SWIO	K8/K7	VCCIO/GNDIO	Power	O	VIO DCDC switched output	No
VFBIO	H8	VCC7/DGND	Analog	I	VIO feedback voltage	PD 5uA
VCC3	N3	VCC3/AGND2	Power	I	LDO6, LDO7, LDO8 power Input	No
LDO8	M1	VCC3/REFGND	Power	O	LDO Regulator output	PD 5uA
LDO7	M3	VCC3/REFGND	Power	O	LDO Regulator output	PD 5uA
LDO6	M2	VCC3/REFGND	Power	O	LDO Regulator output	PD 5uA
VCC4	L1	VCC4/AGND2	Power	I	LDO5 power Input	No
LDO5	K1	VCC4/REFGND	Power	O	LDO Regulator output	PD 5uA
VCC5	D8	VCC5/AGND	Power	I	LDO3, LDO4 power Input	No
LDO3	E7	VCC5/REFGND	Power	O	LDO Regulator output	PD 5uA
LDO4	C8	VCC5/REFGND	Power	O	LDO Regulator output	PD 5uA
VRTC	B5	VCC7/REFGND	Power	O	LDO Regulator output	PD 5uA
VCC6	N5	VCC6/AGND2	Power	I	LDO1, LDO2 power Input	No
LDO1	N6	VCC6/REFGND	Power	O	LDO Regulator output	No
LDO2	N4	VCC6/REFGND	Power	O	LDO Regulator output	No
VCC7	B6	VCC7/REFGND	Power	I	VRTC power Input and analog references supply	No
AGND	H6/H5	AGND	Power	I/O	Analog ground	No
AGND2	N8/J3	AGND	Power	I/O	Analog ground	No
DGND	B2/B1/A1	DGND	Power	I/O	Digital ground	No
EN2	M6	VDDIO/DGND	Digital	I/O	Enable for supplies/ voltage scaling dedicated I^2C data	External PU
EN1	M7	VDDIO/DGND	Digital	I/O	Enable for supplies/ voltage scaling dedicated I^2C clock	External PU
GPIO0	L5	VCC7/DGND	Digital	I/O	GPIO, push-pull/ OD as output	OD: external PU
GPIO1	F6	VRTC/DGND	Digital	I/O, OD	GPIO/ LED1 output	OD: External PU
GPIO2	L2	VRTC/DGND	Digital	I/O, OD	GPIO/ DCDC clock synchronization	OD: External PU
GPIO3	B7	VRTC/DGND	Digital	I/O, OD	GPIO/ LED2 output	OD: External PU

PRODUCT PREVIEW

Table 7. TERMINAL FUNCTIONS (continued)

GPIO4	H7	VRTC/DGND	Digital	I/O, OD	GPIO	OD: External PU
GPIO5	G6	VRTC/DGND	Digital	I/O, OD	GPIO	OD: external PU
GPIO6	G3	VRTC/DGND	Digital	I/O; OD	GPIO	OD: External PU
GPIO7	L4	VRTC/DGND	Digital	I/O, OD	GPIO	OD: External PU
GPIO8	K5	VRTC/DGND	Digital	I/O, OD	GPIO	OD: External PU
PWRDN	N2	VRTC/DGND	Analog	I	Reset input e.g for thermal reset	PD
HDRST	L6	VRTC/DGND	Digital	I	Cold reset	PD
VCCS	E8	VCC7/DGND	Analog	I/O	Input for two comparators	
VBST	A2	VBST/GNDC	Analog	I	VDDCtrl, Supply for high-side FET driver	
DRVH	A3	VBST/GNDC	Analog	O	VDDCtrl, High-side FET driver output	
SW	A4	VBST/GNDC	Analog	I	VDDCtrl, Switch node	
V5IN	A5	V5IN/GNDC	Power	I	VDDCtrl, 5V input	
DRVL	A6	V5IN/GNDC	Analog	O	VDDCtrl, FET driver output	
VOUT	B4	VOUT/GNDC	Analog	I	VDDCtrl, Feedback input	
TRIP	B3	V5IN/GNDC	Analog	I	VDDCtrl, OCL detection threshold pin	
VFB	C5	VOUT/GNDC	Analog	I	VDDCtrl, slew rate control capacitance	
PGOOD	C4	VCC7/GNDC	Analog	O, OD	VDDCtrl, internal signal, leave floating (controller trimming only)	
GNDC	A8/A7	GNDC	Power	I/O	VDDCtrl, Controller gnd	
TRAN	C6	VCC7/GNDC	Analog	I	Internal functional pin, leave floating (controller trimming only)	
EN	D5	VCC7/GNDC	Analog	I	Internal functional pin, leave floating	

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PIN/BALL ASSIGNMENT

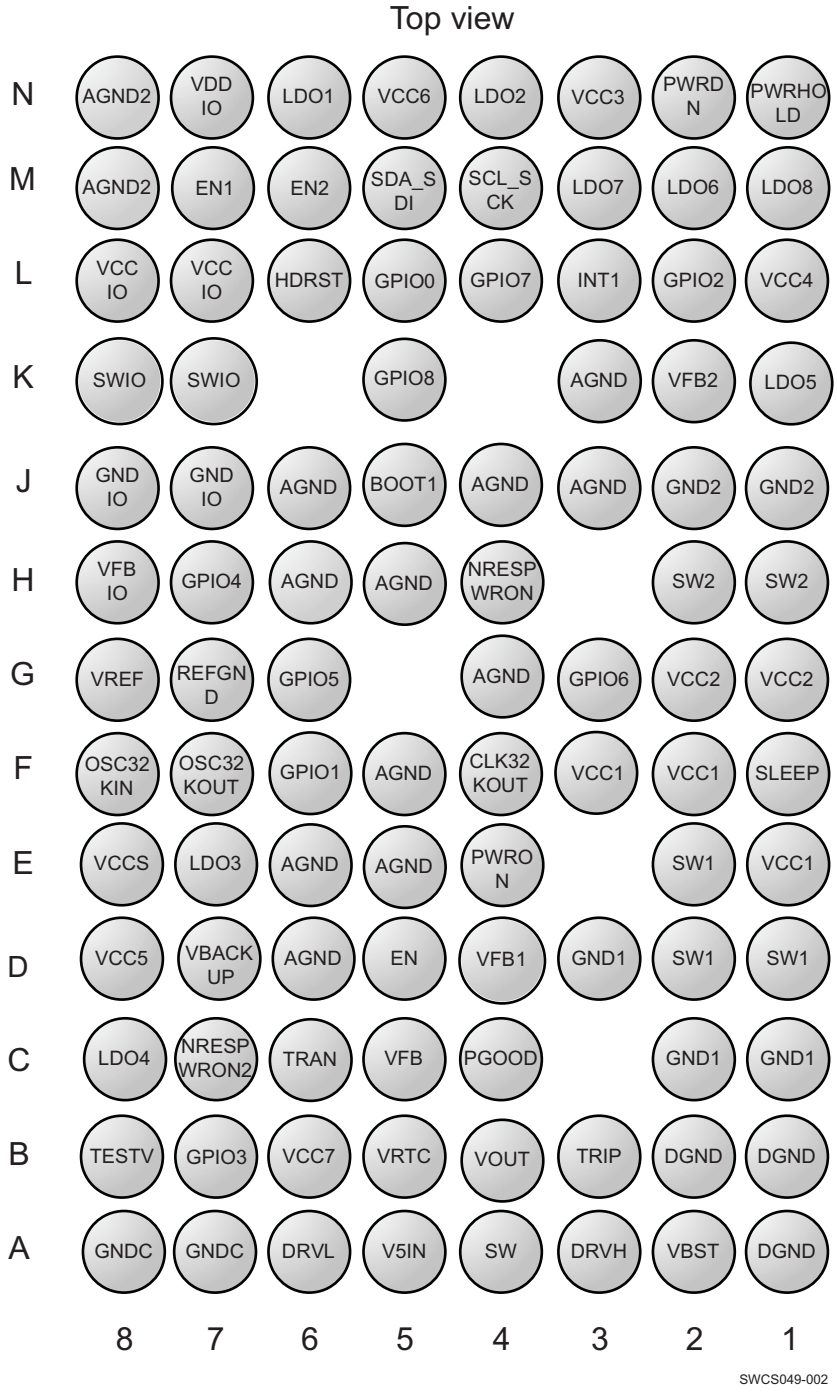

Figure 10. Ball Assignment - Top View

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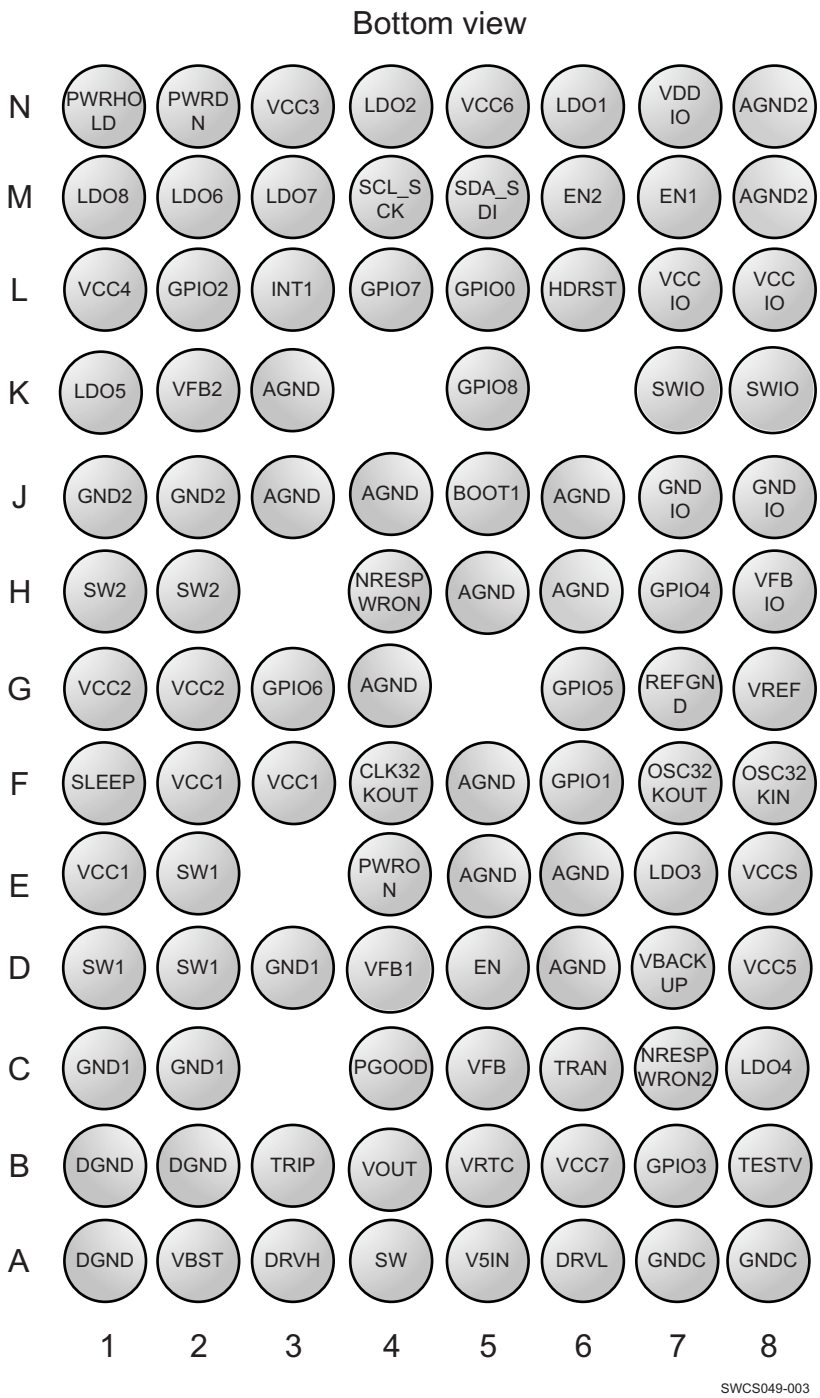

Figure 11. Ball Assignment - Bottom View

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DETAILED DESCRIPTION

POWER REFERENCE

The bandgap voltage reference is filtered by using an external capacitor connected across the VREF output and the analog ground REFGND (see RECOMMENDED OPERATING CONDITIONS). The VREF voltage is distributed and buffered inside the device.

POWER RESOURCES

The power resources provided by the TPS65911 device include inductor based switched mode power supplies (SMPSs) and linear low-dropout voltage regulators (LDOs). These supply resources provide the required power to the external processor cores and external components, and to modules embedded in the TPS65911 device.

Two of the integrated SMPSs and the external FET SMPS have voltage scaling capability. These SMPSs will provide independent core voltage domains to the host processor. When changing the output voltage, VDD1 and VDD2 reach the new value through successive steps of 2.5 to 12.5 mV. The size of the voltage step is selected by the TSTEP bit. VDDCtrl has a target slew rate of 100 mV/20 µs. New output values are reached in successive smaller steps of N × LSB, LSB = 12.5 mV, N = 1 to 4. A suitable combination of steps is calculated internally based on current and new target value for output voltage.

The VIO SMPS provides supply voltage for the host processor I/Os.

Table 8 lists the power sources provided by the TPS65911 device.

Table 8. Power Sources

RESOURCE	TYPE	VOLTAGES	POWER
VIO	SMPS	1.5/ 1.8/ 2.5/3.3 V	1500 mA
VDD1	SMPS	0.6 ... 1.5 V in 12.5-mV steps Programmable multiplication factor: x2, x3	1500 mA
VDD2	SMPS	0.6 ... 1.5 V in 12.5-mV steps Programmable multiplication factor: x2, x3	1500 mA
VDDCtrl	SMPS	0.6 … 1.4 V in 12.5-mV steps	6000 mA
LDO1	LDO	1.0–3.3 V, 0.05-V step	320 mA
LDO2	LDO	1.0–3.3 V, 0.05-V step	320 mA
LDO3	LDO	1.0–3.3 V, 0.1-V step	200 mA
LDO4	LDO	1.0–3.3 V, 0.05-V step	50 mA
LDO5	LDO	1.0–3.3 V, 0.1-V step	300 mA
LDO6	LDO	1.0–3.3 V, 0.1-V step	300 mA
LDO7	LDO	1.0–3.3 V, 0.1-V step	300 mA
LDO8	LDO	1.0–3.3 V, 0.1-V step	300 mA

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EMBEDDED POWER CONTROLLER

The embedded power controller (EPC) manages the state of the device and controls the power-up sequence.

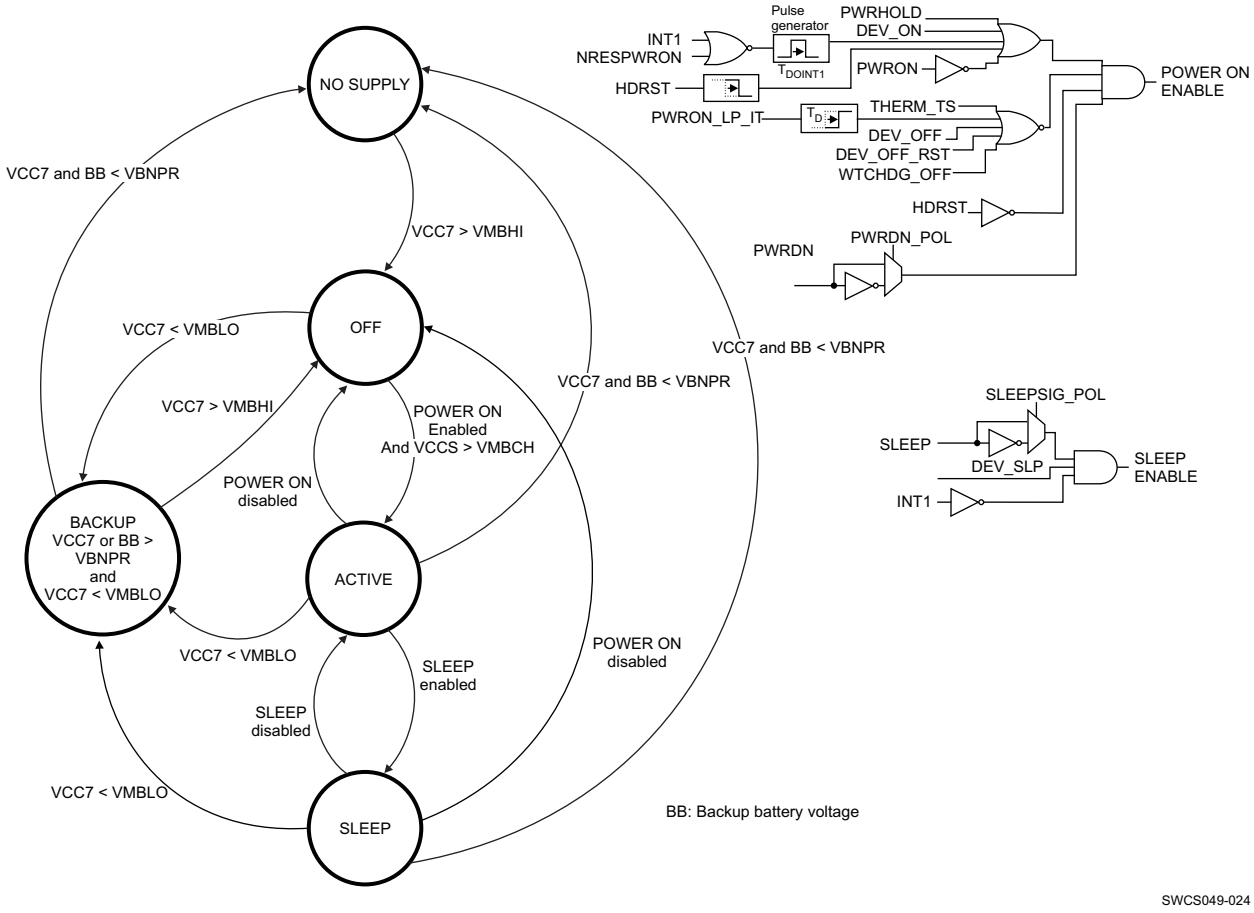
STATE-MACHINE

The EPC supports the following states:

- **NO SUPPLY:** The main battery supply voltage is not high enough to power the VRTC regulator. A global reset is asserted in this case. Everything on the device is off.
- **BACKUP:** The main battery supply voltage is high enough to enable the VRTC domain but not enough to switch on all the resources. In this state, the VRTC regulator is in backup mode and only the 32K oscillator and RTC module are operating (if enabled). All other resources are off or under reset.
- **OFF:** The main battery supply voltage is high enough to start the power-up sequence but device power on is not enabled. All power supplies are in the OFF state except VRTC.
- **ACTIVE:** Device POWER ON enable conditions are met and regulated power supplies are on or can be enabled with full current capability.

- **SLEEP:** Device SLEEP enable conditions are met and some selected regulated power supplies are in low-power mode.

Figure 12 shows the transitions for the state-machine.



NOTE: PWRHOLD enables power-on unless the pin is programmed as GPI.

Figure 12. Embedded Power Control State-Machine

Device POWER ON enable conditions:

- None of the device POWER ON disable conditions are met.
- PWRON signal low level
- Or PWRHOLD signal high level
- Or DEV_ON control bit set to 1 (default inactive)
- Or interrupt flag active (default INT1 low) generates a POWER ON enable condition during a fixed delay (t_{DOINT1} pulse duration defined in POWER CONTROL TIMING). Interrupt sources expected (if enabled), when the device is off:
  - RTC alarm interrupt
  - First-time input voltage rising above the VMBHI threshold (depending on the boot mode used) and input voltage > VMBCH threshold. The interrupt corresponding to this last condtion is VMBCH_IT in the INT_STS_REG register.

Interrupt flag active generates a POWER ON enable condition pulse of length t_{DOINT1} only when the device is in the OFF state (when the NRESPWRON signal is low). The POWER ON enable condition pulse occurs only if the interrupt status bit is initially low (no previous interrupt pending in the status register). The interrupt status register must first be cleared to allow device power off during the t_{DOINT1} pulse duration.

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GPIO2 cannot be used to turn on the device, even if its associated interrupt is not masked. The GPIO0, GPIO1, GPIO3, GPIO4, or GPIO5 signals can be used to turn on the device, if its associated interrupt is not masked.

Note: The watchdog interrupt is not a power on event, but will wake up the device from sleep mode.

Device POWER ON disable conditions:

- PWRON signal low level during more than the long-press delay: PWON_LP_DELAY (can be disabled though register programming). The interrupt corresponding to this condtion is PWRON_LP_IT in the INT_STS_REG register.
- Or die temperature has reached the thermal shutdown threshold (THERM_TS = 1).
- Or DEV_OFF or DEV_OFF_RST control bit is set to 1 (DEV_OFF value is cleared when the device is in OFF state).

Note: If the DEV_ON bit is set to 1, after switch-off, the device will switch back on. To keep the device off, DEV_ON must be cleared first.

Device SLEEP enable conditions:

- SLEEP signal low level (default, or high level depending on the programmed polarity)
- And DEV_SLP control bit is set to 1.
- And interrupt flag inactive (default INT1 high): no nonmasked interrupt is pending.

The SLEEP state can be controlled by programming DEV_SLP and keeping the SLEEP signal floating, or it can be controlled through the SLEEP signal setting the DEV_SLP bit to 1 once, after device turn-on.

Device reset scenarios:

The device has three reset scenarios:

- Full reset: All digital logic of device is reset.
  - Caused by POR (power on reset) when VCC7 < VBNPR
- General reset: No impact on the RTC, backup registers, or interrupt status.
  - Caused by PWON_LP_RST bit set high
  - Or DEV_OFF_RST bit set high
  - Or HDRST input set high
- Turnoff: Power reinitialization in off/backup mode.

A mapping of digital registers to these reset scenarios is described in Table 13.

BOOT CONFIGURATION AND SWITCH-ON/-OFF SEQUENCES

The power sequence is the automated switch-on of the devices resources when an OFF-to-ACTIVE transition occurs. The power-on sequence has 15 sequencial time slots to which resources (DCDCs, LDOs, 32-kHz clock, GPIO0, GPIO2, GPIO6, GPIO7) can be assigned. The time slot length can be selected to be 0.5 ms or 2 ms. If a resource is not assigned to any time slot, it will be in off mode after the power-on sequence and the voltage level can be changed through the register SEL bits before enabling the resource.

Power off disables all power resources at the same time by default. By setting the PWR_OFF_SEQ control bit to 1, power off will follow the power-up sequence in reverse order (the first resource to be powered on will be last to power off).

The values of VDD1, VDD2, and VDDCtrl set in the boot sequence can be selected from 16 steps. For the whole range, 100-mV steps are available: 0.6/0.7...1.4/1.5 V. From 0.8 to 1.4 V, additional values with 50-mV step resolution can be set: 0.85/1.05...1.35 V.

For LDO1, LDO2, and LDO4 all levels from 1.0 to 3.3 V are selectable in the boot sequence with 50-mV steps. For other LDOs, the level is selectable with 100-mV steps, from 1.0 to 3.3 V.

The device supports three boot configurations, which define the power sequence and several device control bits. The boot configuration is selectable by the device BOOT1 pin.

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BOOT1	Boot Configuration
Floating	Test boot mode
0	Fixed boot mode
1	EEPROM boot mode

The BOOT1 input pad is disabled after the boot mode is read at power up, to save power.

Table 9 and Table 10 describe the power sequence and general control bits defined in the boot sequence, respectively.

Fixed boot mode is the same in all part numbers while EEPROM boot mode is different in each part number. Table 9 and Table 10 describe the EEPROM for the TPS659110. For the TPS659112 and TPS659113, see their respective user guides.

Table 9. Boot Configuration: Power Sequence Control Bits

Register	Bit	Description	TPS65911	
			Fixed Boot	EEPROM Boot TPS659110
VDD1_OP_REG/VDD1_SR_REG		VDD1 voltage level selection for boot. Levels available: 0.6/0.7/0.8/0.85/0.9/0.95/.../1.35/1.4/1.5 V	1.2 V	1.2 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection, x1 or x2	x1	x1
EEPROM		VDD1 time slot selection	3	3
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Enable skip	Enable skip
VDD2_OP_REG/VDD2_SR_REG		VDD2 voltage level selection for boot. Levels available: 0.6/0.7/0.8/0.85/0.9/0.95/.../1.35/1.4/1.5 V	1.5 V	1.5 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection, x1 or x3	x1	x1
EEPROM		VDD2 time slot selection	6	6
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Enable skip	Enable skip
VIO_REG	SEL[3:2]	VIO voltage selection	1.8 V	1.8 V
EEPROM		VIO time slot selection	4	4
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Enable skip	Enable skip
VDDCtrl_OP_REG/VDDCtrl_SR_REG		VDDCtrl voltage level selection for boot. Levels available: 0.6/0.7/0.8/0.85/0.9/0.95/../1.35/1.4 V	Off	Off
EEPROM		VDDCtrl time slot selection	Off	Off
LDO1_REG	SEL[7:2]	LDO1 voltage selection	1.05 V	1.05 V
EEPROM		LDO1 time slot	Off	Off
LDO2_REG	SEL[7:2]	LDO2 voltage selection	1.2 V	1.2 V
EEPROM		LDO2 time slot	7	7
LDO3_REG	SEL[6:2]	LDO3 voltage selection	LDO3 voltage: 1 V	LDO3 voltage: 1 V
EEPROM		LDO3 time slot	Off	Off
LDO4_REG	SEL[7:2]	LDO4 voltage selection	1.2 V	1.2 V
EEPROM		LDO4 time slot	2	2
LDO5_REG	SEL[6:2]	LDO5 voltage selection	LDO5 voltage: 1 V	LDO5 voltage: 1 V
EEPROM		LDO5 time slot	Off	Off
LDO6_REG	SEL[6:2]	LDO6 voltage selection	LDO6 voltage: 1 V	LDO5 voltage: 1 V
EEPROM		LDO6 time slot	Off	Off
LDO7_REG	SEL[6:2]	LDO7 voltage selection	1.2 V	1.2 V
EEPROM		LDO7 time slot	5	5
LDO8_REG	SEL[6:2]	LDO8 voltage selection	1.0 V	1.0 V
EEPROM		LDO8 time slot	7	7

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Table 9. Boot Configuration: Power Sequence Control Bits (continued)

Register	Bit	Description	TPS65911	
			Fixed Boot	EEPROM Boot TPS659110
CLK32KOUT pin		CLK32KOUT time slot	5	5
NRESPWRON, NRESPWRON2 pin		NRESPWRON time slot	10	10
GPIO0 pin		GPIO0 time slot	1	1
GPIO2 pin		GPIO2 time slot	Off	Off
GPIO6 pin		GPIO6 time slot	6	6
GPIO7 pin		GPIO7 time slot	5	5

Table 10. Boot Configuration: General Control Bits

Register	Bit	Description	TPS65911	
			Fixed Boot	EEPROM Boot
VRTC_REG	VRTC_OFFMASK	0: VRTC LDO will be in low-power mode during OFF state. 1: VRTC LDO will be in full-power mode during OFF state.	0	0
DEVCTRL_REG	CK32K_CTRL	0: Clock source is crystal/external clock. 1: Clock source is internal RC oscillator.	Crystal	Crystal
DEVCTRL_REG	DEV_ON	0: No impact 1: Will maintain device on, in ACTIVE or SLEEP state	0	0
DEVCTRL2_REG	TSLOTD	Boot sequence time slot duration: 0: 0.5 ms 1: 2 ms	2 ms	2 ms
DEVCTRL2_REG	PWON_LP_OFF	0: Turn off device after PWRON long-press not allowed. 1: Turn off device after PWRON long-press.	1	1
DEVCTRL2_REG	PWON_LP_RST	0: No impact 1: Reset digital core when device is off	1	1
DEVCTRL2_REG	IT_POL	0: INT1 signal will be active-low. 1: INT1 signal will be active-high.	0	0
INT_MSK_REG	VMBHI_IT_MSK	0: Device will automatically switch-on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition 1: Start-up reason required before switch-on	1	1
INT_MSK3_REG	GPIO5_F_IT_MSK	0: GPIO5 falling-edge detection interrupt not masked 1: GPIO5 falling-edge detection interrupt masked	1	1
INT_MSK3_REG	GPIO5_R_IT_MSK	0: GPIO5 rising-edge detection interrupt not masked 1: GPIO5 rising-edge detection interrupt masked	0	0
INT_MSK3_REG	GPIO4_F_IT_MSK	0: GPIO4 falling-edge detection interrupt not masked 1: GPIO4 falling-edge detection interrupt masked	1	1

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Table 10. Boot Configuration: General Control Bits (continued)

Register	Bit	Description	TPS65911	
			Fixed Boot	EEPROM Boot
INT_MSK3_REG	GPIO4_R_IT_MSK	0: GPIO4 rising-edge detection interrupt not masked 1: GPIO4 rising-edge detection interrupt masked	0	0
GPIO0_REG	GPIO_ODEN	0: GPIO0 confiured as push-pull output 1: GPIO0 configured as open-drain output	Push-pull	Push-pull
WATCHDOG_REG	WATCHDOG_EN	0: Watchdog disabled 1: Watchdog enabled, periodic operation with 100 s	1	0
VMBCH_REG	VMBBUF_BYPASS	0: Enable input buffer for external resistive divider 1: In single-cell system, disable buffer for low lower	Disable buffer	Disable buffer
VMBCH_REG	VMBCH_SEL[5:1]	Select threshold for boot gating comparator COMP1, 2.5–3.5 V.	3.1 V	3.1 V
EEPROM	AUTODEV_ON	0: PWRHOLD pin is used as PWRHOLD feature. 1: PWRHOLD pin is GPI. After power on, DEV_ON set high internally, no processor action needed to maintain supplies.	1, PWRHOLD pin is GPI	1, PWRHOLD pin is GPI
EEPROM	PWRDN_POL	0: PWRDN signal will be active-low. 1: PWRDN signal will be active-high.	Active-low	Active-low

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CONTROL SIGNALS

SLEEP

When none of the device SLEEP-disable conditions are met, a falling edge (default, or rising edge, depending on the programmed polarity) of this signal causes an ACTIVE-to-SLEEP state transition of the device. A rising edge (default, or falling edge, depending on the programmed polarity) causes a transition back to the ACTIVE state. This input signal is level-sensitive and no debouncing is applied.

While the device is in the SLEEP state, predefined resources are automatically set in their low-power mode or off. Resources can be kept in their active mode (full-load capability) by programming the SLEEP_KEEP_LDO_ON and the SLEEP_KEEP_RES_ON registers. These registers contain 1 bit per power resource. If the bit is set to 1, then that resource stays in active mode when the device is in the SLEEP state.

32KCLKOUT is also included in the SLEEP_KEEP_RES_ON register and the 32-kHz clock output is maintained in the SLEEP state if the corresponding mask bit is set.

The status (low or high) of GPO0, GPO6, GPO7, and GPO8 are also controlled by the SLEEP signal, to allow enabling and disabling of external resources during sleep.

PWRHOLD

The PWRHOLD pin can be used as a PWRHOLD signal input or as a general purpose input (GPI). The mode is selected by the AUTODEV_ON bit, which is part of the boot configuration. When AUTODEV_MODE = 0, the PWRHOLD feature is selected.

Configured as PWRHOLD, when none of the device POWER ON disable conditions are met, a high level of this signal causes an OFF-to-ACTIVE state transition of the device and a low level causes a transition back to the OFF state.

This input signal is level-sensitive and no debouncing is applied. The rising and/or falling edge of PWRHOLD is highlighted through an associated interrupt if interrupt is unmasked.

When AUTODEV_ON = 1, the pin is used as a GPI. As a GPI, this input can generate a maskable interrupt from a rising or falling edge of the input. When AUTODEV_ON = 1, a rising edge of NRESPWRON also automatically sets the DEV_ON bit to 1 to maintain supplies after the switch-on sequence, thus removing the need for the processor to set the PWRHOLD signal or the DEV_ON bit.

BOOT1

This signal determines with which processor the device is working and, hence, which power-up sequence is needed. For more details, see SWITCH-ON/-OFF SEQUENCES AND TIMING. There is no debouncing on this input signal.

NRESPWRON, NRESPWRON2

The NRESPWRON signal is used as the reset to the processor and is in the VDDIO domain. It is held low until the ACTIVE state is reached. See SWITCH-ON/-OFF SEQUENCES AND TIMING to get detailed timing.

The NRESPWRON2 signal is a second reset output. It follows the state of NRESPWRON but has an open-drain output with external pullup. The supply for the external pullup must not be activated before the TPS65911 device is in control of the output state (that is, not earlier than during first power-up sequence slot). In off mode, the NRESPWRON2 output has weak internal pulldown.

CLK32KOUT

This signal is the output of the 32K oscillator, which can be enabled or not during the power-on sequence, depending on the boot mode. It can be enabled and disabled by register bit, during the ACTIVE state of the device. The CLK32KOUT output can also be enabled or not during the SLEEP state of the device depending on the programming of the SLEEPMASK register.

PWRON

The PWRON input is connected to an external button. If the device is in the OFF or SLEEP state, a debounced falling edge (PWRON input low for minimum of 100 µs) causes an OFF-to-ACTIVE state or a SLEEP-to-ACTIVE state transition of the device. If the device is in active mode, then a low level on this signal generates an interrupt. If the PWRON signal is low for more than the PWON_TO_OFF_DELAY delay and the corresponding interrupt is not acknowledged by the processor within 1 second, the device goes into the OFF state. See Figure 3 and Figure 4 for PWRON behaviour.

INT1

The INT1 signal (default active low) warns the host processor of any event that has occurred on the TPS65911 device. The host processor can then poll the interrupt from the interrupt status register through I^2C to identify the interrupt source. A low level (default setting) indicates an active interrupt, highlighted in the INT_STS_REG register. The polarity of INT1 can be set programming the IT_POL control bit. INT1 flag active is a POWER ON enable condition during a fixed delay, t_{DOINT1} (only), when the device is in the OFF state (when NRESPWRON is low).

Any of the interrupt sources can be masked programming the INT_MSK_REG register. When an interrupt is masked its corresponding interrupt status bit is still updated, but the INT1 flag is not activated. Interrupt source masking can be used to mask a device switch-on event. Because interrupt flag active is a POWER ON enable condition, during t_{DOINT1} delay, any interrupt not masked must be cleared to allow immediate turn off of the device.

For a description of interrupt sources, see Table 12.

EN2 and EN1

EN2 and EN1 are the data and clock signals of the serial control interface dedicated to voltage scaling applications.

These signals can also be programmed to be used as enable signals of one or several supplies, when the device is on (NRESPWRON high). A resource assigned to EN2 or EN1 control automatically disables the serial control interface.

Programming EN1_LDO_ASS_REG, EN2_LDO_REG, and SLEEP_KEEP_LDO_ON_REG registers: EN1 and EN2 signals can be used to control the turn on/off or SLEEP state of any LDO-type supplies.

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Programming EN1_SMPS_ASS_REG, EN2_SMPS_ASS_REG, and SLEEP_KEEP_RES_ON registers: EN1 and EN2 signals can be used to control the turn on/off or LOW-POWER state (PFM mode) of SMPS-type supplies.

The EN2 and EN1 signals can be used to set the output voltage of VDD1 and VDD2 SMPS from a roof to a floor value, preprogrammed in the VDD1_OP_REG, VDD2_OP_REG and VDD1_SR_REG, VDD2_SR_REG registers.

When a supply is controlled through the EN1 or EN2 signals, its state is no longer driven by the device SLEEP state.

GPIO0–8

GPIO0, GPIO2, and GPIO6–7 can be programmed to be part of the power-up sequence and used as enable signals for external resources.

GPIO0 is a configurable I/O in the VCC7 domain. By default, its output is push-pull, driving low. GPIO0 can also be configured as an open-drain output with external pullup.

GPIO1 through GPIO8 are configurable open-drain digital I/Os in the VRTC domain. GPIO directivity, debouncing delay, and internal pullup can be programmed. By default, all are inputs with weak internal pulldown; as open-drain output an external pullup is required.

GPIO0–1 and GPIO3–5 can be used to turn on the device if the corresponding interrupt is not masked. When configured as an input, GPIO2 cannot be used to turn on the device, even if its associated interrupt is not masked. The GPIO interrupt is level sensitive. When an interrupt is detected, before clearing the interrupt, it should first be disabled by masking it.

GPIO1 and GPIO3, which have current sink capability of 10 mA, can also be used to drive LEDs connected to a 5-V supply.

GPIO2 can be used for synchronizing DCDCs to an external clock. Programming DCDCCKEXT = 1, VDD1, VDD2, and VIO DCDC switching can be synchronized using a 3-MHz clock set though the GPIO2 pin. VDD1 and VDD2 will be in-phase and VIO will be phase shifted by 180 degrees.

It is recommended not to connect noisy switching signals to GPIO4 and GPIO5.

HDRST Input

HDRST is a cold reset input for the PMIC. High level at input forces the TPS65911 into off mode, causing a general reset of device to the default settings. The default state is defined by the register reset state and boot configuration. HDRST high level keeps the device in off mode. When reset is released and HDRST input goes low, the device automatically transitions to active mode. The device is kept in active mode for the period t_{DONIT1}, after which another power-on enable reason is needed to maintain the device on.

The HDRST input is in the VRTC domain and has a weak internal pulldown, which is active by default.

PWRDN

The PWRDN input is a reset input with selectable polarity (PWRDN_POL). High(low) level at input forces the TPS65911 device into off mode, causing a power-off reset. Off mode is maintained until PWRDN is released and a start-up reason like PWRON button press or DEV_ON = 1 is detected. An interrupt is generated to indicate the cause for shutdown. The PWRDN input is in the VRTC domain, but can tolerate a 5-V input.

Comparators: COMP1 and COMP2

The TPS65911 device has three comparators for system status detection/control. One comparator detects the voltage at pin VCC7. When VCC7 > VMBHI, the comparator initiates a NO SUPPLY-to-OFF transition and the VMBHI_IT interrupt is generated. When VCC7 < VMBLO, the comparator initiates an ACTIVE/SLEEP/OFF-to-BACKUP transition. When both VCC7 and backup battery are below VBPNR, the NO SUPPLY state is entered.

Comparators COMP1 and COMP2 detect the voltage of VCCS. Programmbale comparator COMP1 is intended for detecting if battery voltage is high enough for an OFF-to-ACTIVE transition of the TPS65911 device. For an

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OFF-to-ACTIVE transition VCCS must be > VMBCH (main battery charged) and a level below the comparator threshold prevents the power-up sequence. The threshold can be set from 2.5 to 3.5 V with 50-mV steps through VMBCH_SEL. The comparator has debouncing so that VCCS must stay above VMBDCH (VMBCH – 0.1 V) for a debouncing period of 61 µs. The comparator can be bypassed if the threshold selection is set to 0. The default threshold is set in the boot configuration.

In a system with a multiple-cell battery, the battery level is sensed through an external resistor divider. The TPS65911 device has an internal buffer at the VCCS input, which must be used with the external resistive divider.

In a single-cell system, VCCS and VCC7 are connected directly to the battery. The VCCS input buffer can be bypassed to minimize power consumption. The buffer bypass is controlled with the VMBBUF_BYPASS bit in the boot configuration.

COMP2 is disabled by default and can be enabled by software. The comparator trigger generates an interrupt which is programmable on the rising (VMBCH2_H_IT) or falling edge (VMBCH2_L_IT), hence the comparator can be used for detecting high or low battery scenarios. COMP2 generates an interrupt for the host. In sleep mode, this creates a wake-up interrupt for the host. In off mode, the comparator trigger generates a turn-on event. In backup or no supply modes, the comparator is not active.

The COMP2 threshold can be set from 2.5 to 3.5 V with 50-mV steps. Enabling the comparator is done through the voltage threshold selection bit VMBDCH2_SEL, which is set to 0 by default.

Watchdog

The watchdog has two modes of operation.

In periodic operation an interrupt is generated with a regular period defined by the WTCHDG_TIME setting. The IC initiates WTCHDOG shutdown if the interrupt is not cleared within the period. The watchdog interrupt WTCHDOG counter is reinitialized when NRESPWRON is low.

In interrupt mode the IC initiates WTCHDOG counter when interrupt is set pending and is cleared when interrupt is cleared. If no interrupt is cleared before watchdog expiration within WTCHDG_TIME, the device goes to off mode.

By default, periodic watchdog functionality is enabled with the maximum WTCHDG_TIME period.

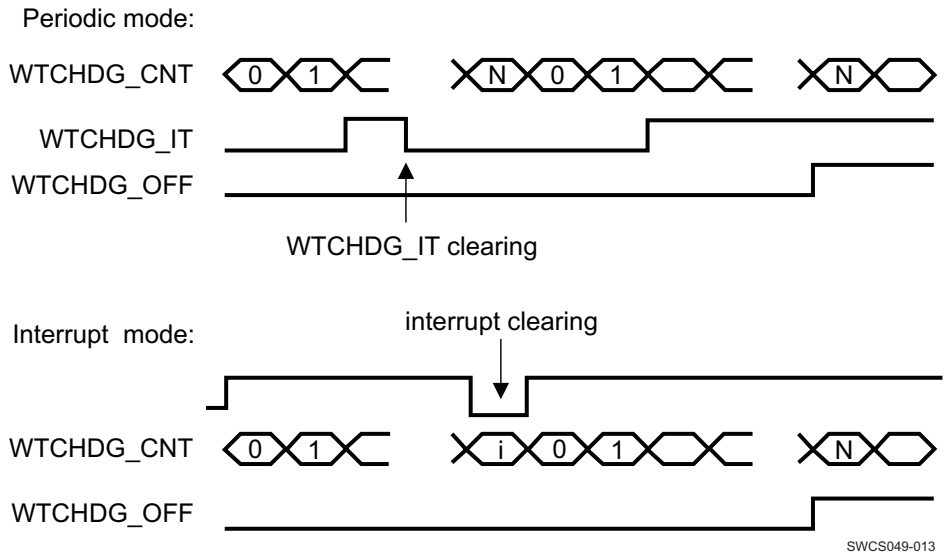

Figure 13. Watchdog Signals

Tracking LDO

LDO4 has an optional mode where its output level follows that of VDD1, from 0.6 to 1.5 V, when VDD1 is active. When VDD1 is set to off, the LDO4 output is defined by the SEL[7:2] bits in LDO4_REG, and can be set from 0.8 to 1.5 V.

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Tracking mode is enabled by setting TRACK = 1 in DCDCCTRL_REG. In initial activation, VDD1 must be enabled and allowed to settle before enabling tracking mode. After initial activation, tracking mode can be kept enabled while VDD1 is turned off. The value of TRACK is set to default (0) after any turnoff event.

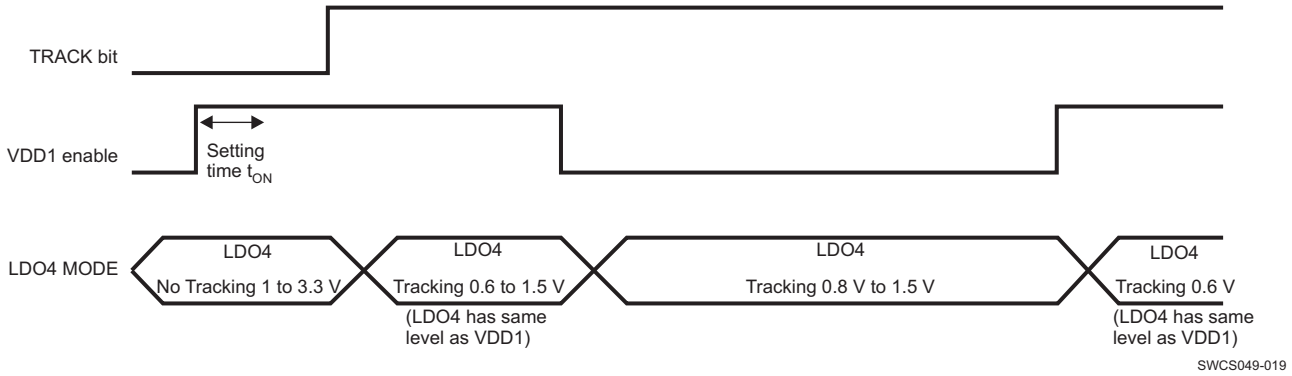

Figure 14. Tracking LDO

PWM AND LED GENERATORS

The TPS65911 device has two LED ON/OFF signal generators, LED1 and LED2. LED1 and LED2 have independently controllable periods from 125 ms to 8 s and ON time from 62.5 to 500 ms. Within the period, one or two ON pulses can be generated (control bit LED1(2)_SEQ). The user must take care to program period and ON time correctly, because no limitation on selected values is imposed. LED1 and LED2 signals can be routed to GPIO1 and GPO3 open-drain outputs, respectively. These GPIOs have a current sink capability of 10 mA.

The PWM generator frequency and duty cycle are set by the PWM_FREQ and PWM_DUTY_CYCLE bits, respectively. The PWM generator signal can be connected to the GPIO3 or GPIO8 output. The PWM generator uses the 3-MHz clock, which is not available in off mode. To enable the PWM in sleep mode, the I2CHS_KEEPON bit must be set to 1.

DYNAMIC VOLTAGE FREQUENCY SCALING AND ADAPTIVE VOLTAGE SCALING OPERATION

Dynamic voltage frequency scaling (DVFS) operation: A supply voltage value corresponding to a targeted frequency of the digital core supplied is programmed in VDD1_OP_REG or VDD2_OP_REG registers.

The slew rate of the voltage supply reaching a new VDD1_OP_REG or VDD2_OP_REG programmed value is limited to 12.5 mV/µs, fixed value.

Adaptative voltage scaling (AVS) operation: A supply voltage value corresponding to a supply voltage adjustment is programmed in VDD1_SR_REG or VDD2_SR_REG registers. The supply voltage is then intended to be tuned by the digital core supplied, based its performance self-evaluation. The slew rate of VDD1 or VDD2 voltage supply reaching a new programmed value is programmable though the VDD1_REG or VDD2_REG register, respectively.

A serial control interface (optional mode for EN1 and EN2 pins) can be dedicated to voltage scaling applications, to give dedicated access to the VDD1_OP_REG, VDD1_SR_REG and VDD2_OP_REG, VDD2_SR_REG registers.

A general-purpose serial control interface (CTL-I^2C) also gives access to these registers, if the SR_CTL_I2C_SEL control bit is set to 1 in the DEVCTRL_REG register (default inactive).

Both control interfaces are compliant with HS-I^2C specification (100 Kbps, 400 Kbps, or 3.4 Mbps).

32-kHz RTC CLOCK

The TPS65911 device can provide a 32-kHz clock to the platform through the CLK32KOUT output, when a crystal is connected.

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Alternatively, the device can accept a square-wave 32-kHz clock signal applied to OSC32IN input (OSC32KOUT kept floating) and gate the clock to CLK32OUT. This clock must be present for any state of the EPC except the NO SUPPLY state. The TPS65911 device also has an internal 32-kHz RC oscillator, to reduce the BOM, if an accurate clock is not needed by the system.

Default selection of a 32-kHz RC oscillator versus 32-kHz crystal oscillator or external square-wave 32-kHz clock depends on the boot configuration setting for the CK32K_CTRL bit.

Switching from the 32-kHz RC oscillator to the 32-kHz crystal oscillator or external square-wave 32-kHz clock can also be programmed though the DEVCTRL_REG register.

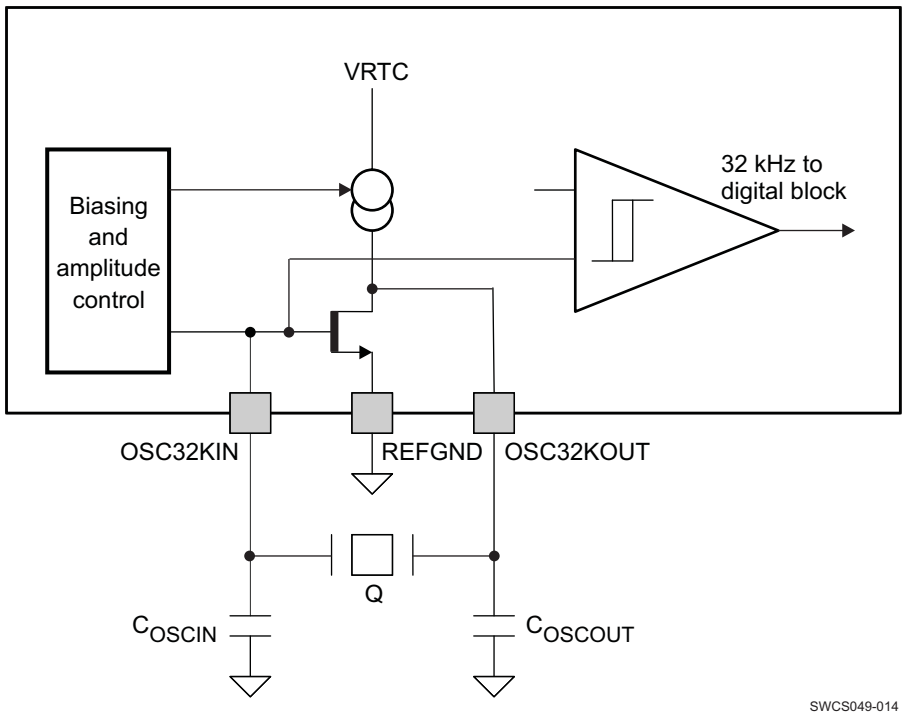

Figure 15. Crystal Oscillator 32-kHz Clock

Real-Time Clock (RTC)

The RTC, which is driven by the 32-kHz clock, provides the alarm and timekeeping functions. The RTC is kept supplied when the device is in the OFF or the BACKUP state.

The main functions of the RTC block are:

- Time information (seconds/minutes/hours) directly in binary-coded decimal (BCD) format
- Calendar information (Day/Month/Year/Day of the week) directly in BCD code up to year 2099
- Programmable interrupts generation: The RTC can generate two interrupts: a timer interrupt RTC_PERIOD_IT periodically (1s/1m/1h/1d period) and an alarm interrupt RTC_ALARM_IT at a precise time of the day (alarm function). These interrupts are enabled using IT_ALARM and IT_TIMER control bits. Periodically interrupts can be masked during the SLEEP period to avoid host interruption and are automatically unmasked after SLEEP wakeup (using the IT_SLEEP_MASK_EN control bit).
- Oscillator frequency calibration and time correction

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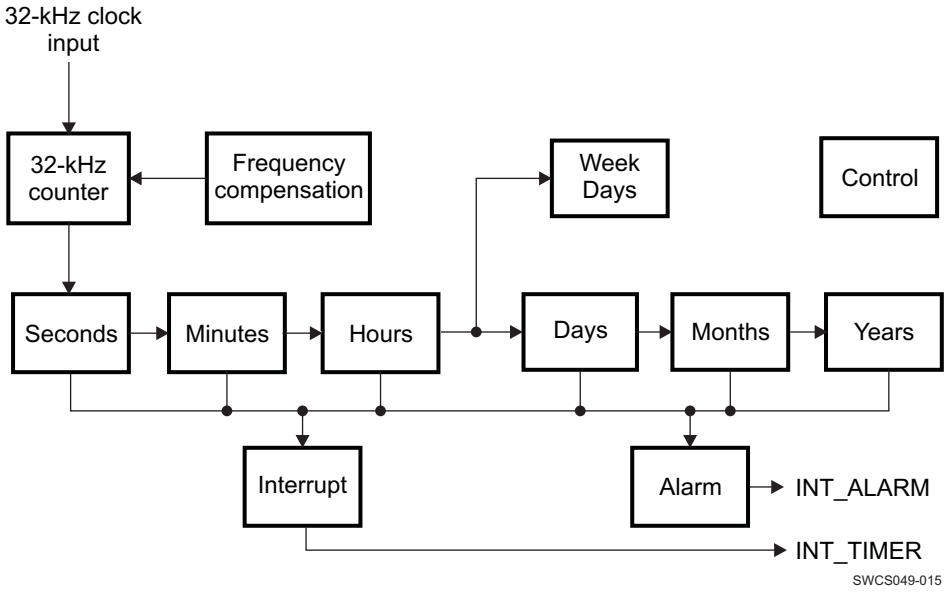

Figure 16. RTC Digital Section Block Diagram

TIME CALENDAR REGISTERS

All the time and calendar information is available in these dedicated registers, called TC registers. Values of the TC registers are written in BCD format.

1. Years data ranges from 00 to 99
   - Leap year = Year divisible by four (2000, 2004, 2008, 2012...)
   - Common year = other years
2. Months data ranges from 01 to 12
3. Days value ranges from:
   - 1 to 31 when months are 1, 3, 5, 7, 8, 10, 12
   - 1 to 30 when months are 4, 6, 9, 11
   - 1 to 29 when month is 2 and year is a leap year
   - 1 to 28 when month is 2 and year is a common year
4. Weeks value ranges from 0 to 6
5. Hours value ranges from 00 to 23 in 24-hour mode and ranges from 1 to 12 in AM/PM mode
6. Minutes value ranges from 0 to 59
7. Seconds value ranges from 0 to 59

To modify the current time, software writes the new time into TC registers to fix the time/calendar information. The processor can write into the TC registers without stopping the RTC. In addition, software can stop the RTC by clearing the STOP_RTC bit of the control register and check the RUN bit of the status to be sure that the RTC is frozen, then update the TC values, and then restart the RTC by setting STOP_RTC bit.

Example: Time is 10H54M36S PM (PM_AM mode set), 2008 September 5, previous register values are:

Table 11. Real-Time Clock Registers Example

Register	Value
SECONDS_REG	0x36
MINUTES_REG	0x54
HOURS_REG	0x90
DAYS_REG	0x05
MONTHS_REG	0x09

Table 11. Real-Time Clock Registers Example (continued)

Register	Value
YEARS_REG	0x08

The user can round to the closest minute, by setting the ROUND_30S register bit. TC values are set to the closest minute value at the next second. The ROUND_30S bit is automatically cleared when the rounding time is performed.

Example:

- If current time is 10H59M45S, a round operation changes time to 11H00M00S.
- if current time is 10H59M29S, a round operation changes time to 10H59M00S.

GENERAL REGISTERS

Software can access the RTC_STATUS_REG and RTC_CTRL_REG registers at any time (except for the RTC_CTRL_REG[5] bit, which must be changed only when the RTC is stopped).

COMPENSATION REGISTERS

The RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers must respect the available access period. These registers must be updated before each compensation process. For example, software can load the compensation value into these registers after each hour event, during an available access period.

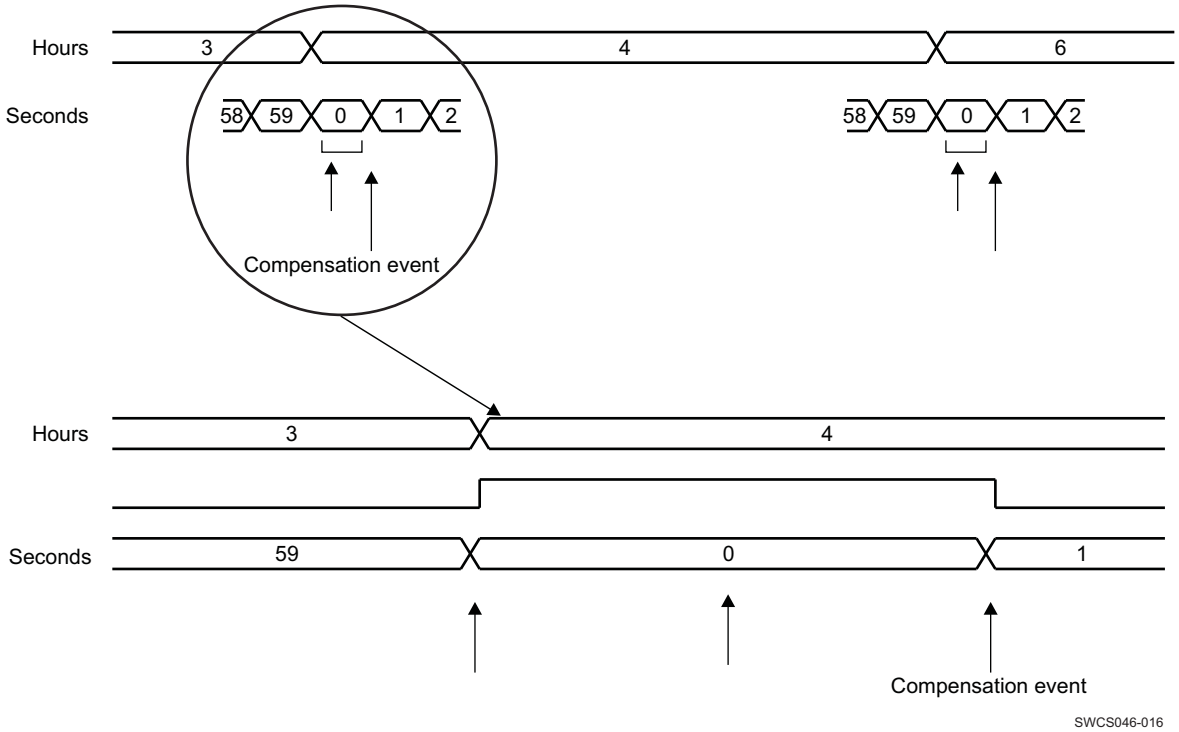

Figure 17. RTC Compensation Scheduling

This drift can be balanced to compensate for any inaccuracy of the 32-kHz oscillator. Software must calibrate the oscillator frequency, calculate the drift compensation versus 1-hour time period; and then load the compensation registers with the drift compensation value. Indeed, if the AUTO_COMP_EN bit in the RTC_CTRL_REG is enabled, the value of COMP_REG (in twos-complement) is added to the RTC 32-kHz counter at each hour and 1 second. When COMP_REG is added to the RTC 32-kHz counter, the duration of the current second becomes (32768 – COMP_REG)/32768s; so, the RTC can be compensated with a 1/32768 s/hour time unit accuracy.

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NOTE

The compensation is considered once written into the registers.

BACKUP BATTERY MANAGEMENT

The device includes a back-up battery switch connecting the VRTC regulator input to a main battery (VCC7) or to a back-up battery (VBACKUP), depending on the voltage value of the battery.

The VRTC supply can then be maintained during a BACKUP state as long as the input voltage is high enough (> VBNPR threshold). Below the VBNPR voltage threshold, the digital core of the device is set under reset by internal signal POR (PowerOnReset).

The back-up domain functions which are always supplied from VRTC are:

- The internal 32-kHz oscillator
- Back-up registers

The back-up battery can be charged from the main battery through an embedded charger. The back-up battery charge voltage and enable is controlled through BBCH_REG register programming. This register content is maintained during the device BACKUP state.

Hence, when enabled, the back-up battery charge is maintained as long as the main battery voltage is higher than the VMBLO threshold and the back-up battery voltage.

BACKUP REGISTERS

As part of the RTC, the device contains five 8-bit registers that can be used for storage by the application firmware when the external host is powered down. These registers retain their content as long as the VRTC is active.

I^2C INTERFACE

A general-purpose serial control interface (CTL-I^2C) allows read and write access to the configuration registers of all resources of the system.

A second serial control interface (optional mode for EN1 and EN2 pins) can be dedicated to DVFS.

Both control interfaces are compliant with the HS-I^2C specification.

These interfaces support the standard slave mode (100 Kbps), fast mode (400 Kbps), and high-speed mode (3.4 Mbps). The general-purpose I^2C module using one slave hard-coded address (ID1 = 2Dh). The voltage scaling dedicated I^2C module uses one slave hard-coded address (ID0 = 12h). The master mode is not supported.

Addressing:

The device supports seven-bit mode addressing.

It does not support the following features:

- 10-bit addressing
- General call

ACCESS PROTOCOLS

or compatibility , the I2C interfaces in the TPS65911x device use the same read/write protocol as other TI power ICs, based on an internal register size of 8 bits. Supported transactions are described below.

SINGLE BYTE ACCESS

A write access is initiated by a first byte including the address of the device (7 MSBs) and a write command (LSB), a second byte provides the address (8 bits) of the internal register, and the third byte represents the data to be written in the internal register, see Figure 18.

A read access is initiated by:

- A first byte, including the address of the device (7 MSBs) and a write command (LSB)
- A second byte, providing the address (8 bits) of the internal register

- A third byte, including again the device address (7 MSBs) and the read command (LSB)

The device replies by sending

- A fourth byte, representing the content of the internal register (see Figure 19)

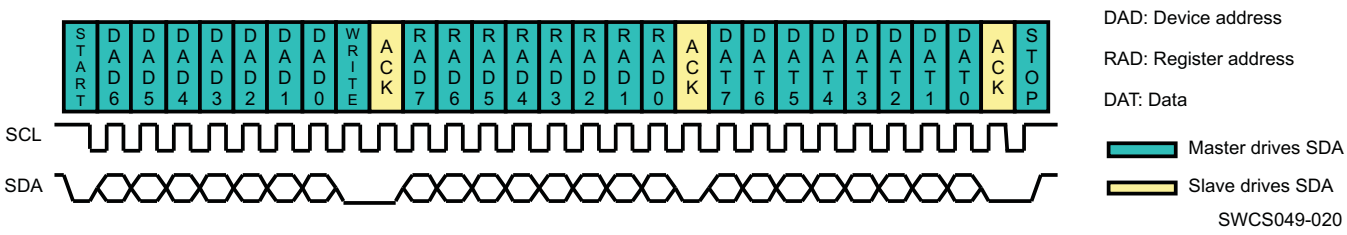

Figure 18. I²C Write Access Single Byte

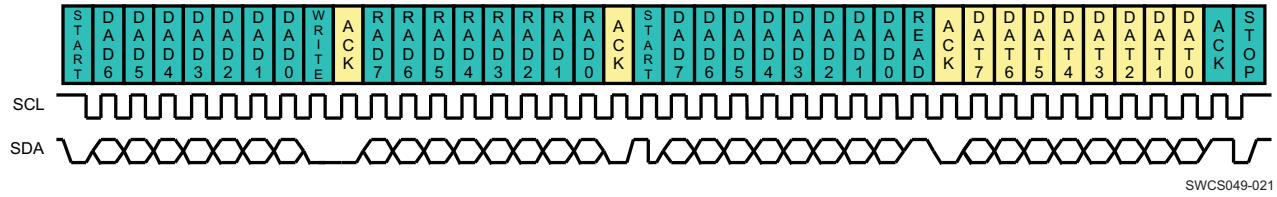

Figure 19. I²C Read Access Single Byte

Multiple Byte Access To Several Adjacent Registers

A write access is initiated by:

- A first byte, including the address of the device (7 MSBs) and a write command (LSB)
- A second byte, providing the base address (8 bits) of the internal registers

The following N bytes represent the data to be written in the internal register starting at the base address and incremented by one at each data byte (see Figure 20).

A read access is initiated by:

- A first byte, including the address of the device (7 MSBs) and a write command (LSB)
- A second byte, providing the base address (8 bits) of the internal register
- A thirrd byte, including again the device address (7 MSBs) and the read command (LSB)

The device replies by sending:

- A fourth byte, representing the content of the internal registers, starting at the base address and next consecutive ones (see Figure 21).

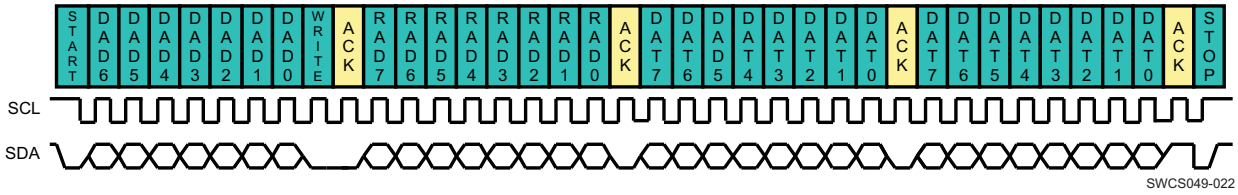

Figure 20. I²C Write Access Multiple Bytes

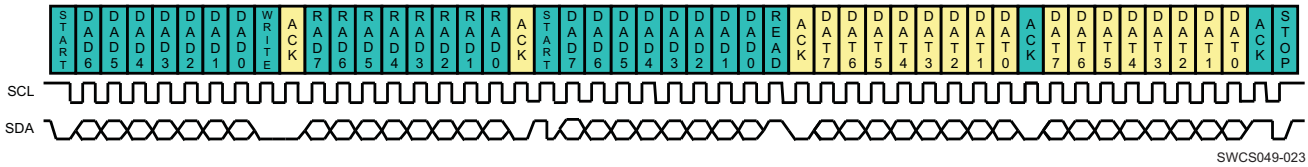

Figure 21. I²C Read Access Multiple Bytes

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THERMAL MONITORING AND SHUTDOWN

A thermal protection module monitors the junction temperature of the device versus two thesholds:

- Hot-die temperature threshold
- Thermal shutdown temperature threshold

When the hot-die temperature threshold is reached, an interrupt is sent to software to close the noncritical running tasks.

When the thermal shutdown temperature threshold is reached, the TPS65911 device is set under reset and a transition to OFF state is initiated. Then the POWER ON enable conditions of the device are not considered until the die temperature has decreased below the hot-die threshold. Hysteresis is applied to the hot-die and shutdown thresholds, when detecting a falling edge of temperature, and both detections are debounced to avoid any parasitic detection.

The TPS65911 device allows programming of four hot-die temperature thresholds to increase the flexibility of the system.

By default, the thermal protection is enabled in ACTIVE state, but can be disabled through programming the THERM_REG register. The thermal protection can be enabled in SLEEP state programming the SLEEP_KEEP_RES_ON register. The thermal protection is automatically enabled during an OFF-to-ACTIVE state transition and is kept enabled in OFF state after a switch-off sequence caused by a thermal shutdown event. Transition to OFF state sequence caused by a thermal shutdown event is highlighted in the INT_STS_REG status register. Recovery from this OFF state is initiated (switch-on sequence) when the die temperature falls below the hot-die temperature threshold.

Hot-die and thermal shutdown temperature threshold detection states can be monitored or masked by reading or programming the THERM_REG register. The hot-die interrupt can be masked by programming the INT_MSK_REG register.

INTERRUPTS

Table 12. Interrupt Sources

Interrupt	Description
RTC_ALARM_IT	RTC alarm event: Occurs at programmed determinate date and time (running in ACTIVE, OFF, and SLEEP state, default inactive)
RTC_PERIOD_IT	RTC periodic event: Occurs at programmed regular period of time (every second or minute) (running in ACTIVE, OFF, and SLEEP state, default inactive)
HOT_DIE_IT	The embedded thermal monitoring module has detected a die temperature above the hot-die detection threshold (running in ACTIVE and SLEEP state). Level sensitive interrupt.
PWRHOLD_R_IT	PWRHOLD signal rising edge
PWRHOLD_F_IT	PWRHOLD signal falling-edge
PWRON_LP_IT	PWRON is low during more than the long-press delay: PWON_TO_OFF_DELAY (can be disable though register programming).
PWRON_IT	PWRON is low while the device is on (running in ACTIVE and SLEEP state). Level-sensitive interrupt.
VMBHI_IT	The battery voltage rise above the VMBHI threshold: NO SUPPLY-to-OFF or BACKUP-to-OFF device states transition (first battery plug or battery voltage bounce detection)
VMBDCH_IT	The battery voltage fall down below the VMBDCH threshold: the minimum operating voltage of power supplies.
GPIO0_R_IT	GPIO_CKSYNC rising-edge detection
GPIO0_F_IT	GPIO_CKSYNC falling-edge detection
VMBCH2_H_IT	Comparator 2 input above threshold detection
VMBCH2_L_IT	Comparator 2 input below threshold detection
GPIO1_R_IT	GPIO1 rising-edge detection
GPIO1_F_IT	GPIO1 falling-edge detection
GPIO2_R_IT	GPIO2 rising-edge detection

Table 12. Interrupt Sources (continued)

Interrupt	Description
GPIO2_F_IT	GPIO2 falling-edge detection
GPIO3_R_IT	GPIO3 rising-edge detection
GPIO3_F_IT	GPIO3 falling-edge detection
GPIO4_R_IT	GPIO4 rising-edge detection
GPIO4_F_IT	GPIO4 falling-edge detection
GPIO5_R_IT	GPIO5 rising-edge detection
GPIO5_F_IT	GPIO5 falling-edge detection
WTCHDG_IT	Watchdog interrupt
PWRDN_IT	PWRDN reset interrupt

PAKCAGE DESCRIPTION

The following are the package descriptions of the TPS65911 PMU devices:

- Package type:

Package	TPS65911
Type	ZRC98 BGA Microstar Junior
Size (mm)	6x9
Substrate layers	1 layer
Pitch ball array (mm)	0.65 mm
Number of balls	98
Thickness (mm) (max. height including balls)	1

PACKAGE THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPS65911 ZRC 96 pins	UNITS
θJA	Junction-to-ambient thermal resistance(2)	32	°C/W
θJC(TOP)	Junction-to-case(top) thermal resistance (3)	18	
θJB	Junction-to-board thermal resistance(4)	16	
ψJT	Junction-to-top characterization parameter(5)	0.2	
ψJB	Junction-to-board characterization parameter(6)	12	
θJC(BOTTOM)	Junction-to-case(bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953. http://focus.ti.com/lit/an/spra953a/spra953a.pdf

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case(top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, yJT, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining qJA, using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, yJB estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining qJA , using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case(bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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APPENDIX A: FUNCTIONAL REGISTERS

The possible device reset domains are:

- Full reset: All digital of device is reset.
  - Caused by POR (Power On Reset) when VCCS < VBNPR
- General reset: No impact on RTC, backup registers or interrupt status.
  - Caused by PWON_LP_RST bit set high or
  - DEV_OFF_RST bit set high or
  - HDRST input set high
- Turnoff OFF: Power reinitialization in off/backup mode.

In following register description, reset domain for each register is defined at the register table heading.

Note: DCDCCTRL_REG and DEVCTRL2_REG have bits in two reset domains.

Note 2:Comment “Default value: See boot configuration” indicates that bit default value is set in boot configuration and not by register Reset value .”

TPS65911_FUNC_REG REGISTERS MAPPING SUMMARY

Table 13. TPS65911_FUNC_REG Register Summary(1)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset
SECONDS_REG	RW	8	0x00	0x00
MINUTES_REG	RW	8	0x00	0x01
HOURS_REG	RW	8	0x00	0x02
DAYS_REG	RW	8	0x01	0x03
MONTHS_REG	RW	8	0x01	0x04
YEARS_REG	RW	8	0x00	0x05
WEEKS_REG	RW	8	0x00	0x06
ALARM_SECONDS_REG	RW	8	0x00	0x08
ALARM_MINUTES_REG	RW	8	0x00	0x09
ALARM_HOURS_REG	RW	8	0x00	0x0A
ALARM_DAYS_REG	RW	8	0x01	0x0B
ALARM_MONTHS_REG	RW	8	0x01	0x0C
ALARM_YEARS_REG	RW	8	0x00	0x0D
RTC_CTRL_REG	RW	8	0x00	0x10
RTC_STATUS_REG	RW	8	0x80	0x11
RTC_INTERRUPTS_REG	RW	8	0x00	0x12
RTC_COMP_LSB_REG	RW	8	0x00	0x13
RTC_COMP_MSB_REG	RW	8	0x00	0x14
RTC_RES_PROG_REG	RW	8	0x27	0x15
RTC_RESET_STATUS_REG	RW	8	0x00	0x16
BCK1_REG	RW	8	0x00	0x17
BCK2_REG	RW	8	0x00	0x18
BCK3_REG	RW	8	0x00	0x19
BCK4_REG	RW	8	0x00	0x1A
BCK5_REG	RW	8	0x00	0x1B
PUADEN_REG	RW	8	0x1F	0x1C
REF_REG	RO	8	0x01	0x1D
VRTC_REG	RW	8	0x01	0x1E
VIO_REG	RW	8	0x05	0x20
VDD1_REG	RW	8	0x0D	0x21
VDD1_OP_REG	RW	8	0x33	0x22
VDD1_SR_REG	RW	8	0x33	0x23
VDD2_REG	RW	8	0x0D	0x24
VDD2_OP_REG	RW	8	0x4B	0x25
VDD2_SR_REG	RW	8	0x4B	0x26
VDDCRTL_REG	RW	8	0x00	0x27
VDDCRTL_OP_REG	RW	8	0x03	0x28
VDDCRTL_SR_REG	RW	8	0x03	0x29
LDO1_REG	RW	8	0x15	0x30
LDO2_REG	RW	8	0x15	0x31
LDO5_REG	RW	8	0x00	0x32
LDO8_REG	RW	8	0x09	0x33
LDO7_REG	RW	8	0x0D	0x34
LDO6_REG	RW	8	0x21	0x35

(1) Register reset values are for fixed boot mode.

Table 13. TPS65911_FUNC_REG Register Summary(1) (continued)

LDO4_REG	RW	8	0x00	0x36
LD03_REG	RW	8	0x00	0x37
THERM_REG	RW	8	0x0D	0x38
BBCH_REG	RW	8	0x00	0x39
DCDCCTRL_REG	RW	8	0x39	0x3E
DEVCTRL_REG	RW	8	0x0000 0014	0x3F
DEVCTRL2_REG	RW	8	0x0000 0036	0x40
SLEEP_KEEP_LDO_ON_REG	RW	8	0x00	0x41
SLEEP_KEEP_RES_ON_REG	RW	8	0x00	0x42
SLEEP_SET_LDO_OFF_REG	RW	8	0x00	0x43
SLEEP_SET_RES_OFF_REG	RW	8	0x00	0x44
EN1_LDO_ASS_REG	RW	8	0x00	0x45
EN1_SMPS_ASS_REG	RW	8	0x00	0x46
EN2_LDO_ASS_REG	RW	8	0x00	0x47
EN2_SMPS_ASS_REG	RW	8	0x00	0x48
INT_STS_REG	RW	8	0x06	0x50
INT_MSK_REG	RW	8	0xFF	0x51
INT_STS2_REG	RW	8	0xA8	0x52
INT_MSK2_REG	RW	8	0xFF	0x53
INT_STS3_REG	RW	8	0x5A	0x54
INT_MSK3_REG	RW	8	0xFF	0x55
GPIO0_REG	RW	8	0x07	0x60
GPIO1_REG	RW	8	0x08	0x61
GPIO2_REG	RW	8	0x08	0x62
GPIO3_REG	RW	8	0x08	0x63
GPIO4_REG	RW	8	0x08	0x64
GPIO5_REG	RW	8	0x08	0x65
GPIO6_REG	RW	8	0x05	0x66
GPIO7_REG	RW	8	0x05	0x67
GPIO8_REG	RW	8	0x08	0x68
WATCHDOG_REG	RW	8	0x07	0x69
VMBCH_REG	RW	8	0x1E	0x6A
VMBCH2_REG	RW	8	0x00	0x6B
LED_CTRL1_REG	RW	8	0x00	0x6C
LED_CTRL2_REG1	RW	8	0x00	0x6D
PWM_CTRL1_REG	RW	8	0x00	0x6E
PWM_CTRL2_REG	RW	8	0x00	0x6F
SPARE_REG	RW	8	0x00	0x70
VERNUM_REG	RO	8	0x00	0x80

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TPS65911_FUNC_REG REGISTER DESCRIPTIONS

Table 14. SECONDS_REG

Address Offset	0x00		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for seconds		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEC1			SEC0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	SEC1	Second digit of seconds (range is 0 up to 5)	RW	0x0
3:0	SEC0	First digit of seconds (range is 0 up to 9)	RW	0x0

Table 15. MINUTES_REG

Address Offset	0x01		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for minutes		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	MIN1			MIN0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	MIN1	Second digit of minutes (range is 0 up to 5)	RW	0x0
3:0	MIN0	First digit of minutes (range is 0 up to 9)	RW	0x0

Table 16. HOURS_REG

Address Offset	0x02		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for hours		
Type	RW		

7	6	5	4	3	2	1	0
PM_NAM	Reserved	HOUR1		HOUR0			

Bits	Field Name	Description	Type	Reset
7	PM_NAM	Only used in PM_AM mode (otherwise it is set to 0) 0 is AM 1 is PM	RW	0
6	Reserved	Reserved bit	RO R returns 0s	0
5:4	HOUR1	Second digit of hours(range is 0 up to 2)	RW	0x0
3:0	HOUR0	First digit of hours (range is 0 up to 9)	RW	0x0

Table 17. DAYS_REG

Address Offset	0x03		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for days		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		DAY1		DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5:4	DAY1	Second digit of days (range is 0 up to 3)	RW	0x0
3:0	DAY0	First digit of days (range is 0 up to 9)	RW	0x1

Table 18. MONTHS_REG

Address Offset	0x04		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for months		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			MONTH1	MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	MONTH1	Second digit of months (range is 0 up to 1)	RW	0
3:0	MONTH0	First digit of months (range is 0 up to 9)	RW	0x1

Table 19. YEARS_REG

Address Offset	0x05		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for day of the week		
Type	RW		

7	6	5	4	3	2	1	0
YEAR1				YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	YEAR1	Second digit of years (range is 0 up to 9)	RW	0x0
3:0	YEAR0	First digit of years (range is 0 up to 9)	RW	0x0

Table 20. WEEKS_REG

Address Offset	0x06		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for day of the week		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						WEEK	

Bits	Field Name	Description	Type	Reset
7:3	Reserved	Reserved bit	RO R returns 0s	0x00
2:0	WEEK	First digit of day of the week (range is 0 up to 6)	RW	0

Table 21. ALARM_SECONDS_REG

Address Offset	0x08		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for alarm programmation for seconds		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		ALARM_SEC1			ALARM_SEC0		

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	ALARM_SEC1	Second digit of alarm programmation for seconds (range is 0 up to 5)	RW	0x0
3:0	ALARM_SEC0	First digit of alarm programmation for seconds (range is 0 up to 9)	RW	0x0

Table 22. ALARM_MINUTES_REG

Address Offset	0x09		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for alarm programmation for minutes		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		ALARM_MIN1			ALARM_MIN0		

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	ALARM_MIN1	Second digit of alarm programmation for minutes (range is 0 up to 5)	RW	0x0
3:0	ALARM_MIN0	First digit of alarm programmation for minutes (range is 0 up to 9)	RW	0x0

Table 23. ALARM_HOURS_REG

Address Offset	0x0A		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for alarm programmation for hours		
Type	RW		

7	6	5	4	3	2	1	0
ALARM_PM_NAM	Reserved	ALARM_HOUR1		ALARM_HOUR0			

Bits	Field Name	Description	Type	Reset
7	ALARM_PM_NAM	Only used in PM_AM mode for alarm programmation (otherwise it is set to 0) 0 is AM 1 is PM	RW	0
6	Reserved	Reserved bit	RO R returns 0s	0
5:4	ALARM_HOUR1	Second digit of alarm programmation for hours(range is 0 up to 2)	RW	0x0
3:0	ALARM_HOUR0	First digitof alarm programmation for hours (range is 0 up to 9)	RW	0x0

Table 24. ALARM_DAYS_REG

Address Offset	0x0B		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for alarm programmation for days		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		ALARM_DAY1		ALARM_DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R Special	0x0
5:4	ALARM_DAY1	Second digit of alarm programmation for days (range is 0 up to 3)	RW	0x0
3:0	ALARM_DAY0	First digit of alarm programmation for days (range is 0 up to 9)	RW	0x1

Table 25. ALARM_MONTHS_REG

Address Offset	0x0C		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for alarm programmation for months		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ALARM_MONTH1	ALARM_MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	ALARM_MONTH1	Second digit of alarm programmation for months (range is 0 up to 1)	RW	0

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Bits	Field Name	Description	Type	Reset
3:0	ALARM_MONTH0	First digit of alarm programmation for months (range is 0 up to 9)	RW	0x1

Table 26. ALARM_YEARS_REG

Address Offset	0x0D		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for alarm programmation for years		
Type	RW		

7	6	5	4	3	2	1	0
ALARM_YEAR1				ALARM_YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	ALARM_YEAR1	Second digit of alarm programmation for years (range is 0 up to 9)	RW	0x0
3:0	ALARM_YEAR0	First digit of alarm programmation for years (range is 0 up to 9)	RW	0x0

Table 27. RTC_CTRL_REG

Address Offset	0x10		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC control register: NOTES: A dummy read of this register is necessary before each I^2C read in order to update the ROUND_30S bit value.		
Type	RW		

7	6	5	4	3	2	1	0
RTC_V_OPT	GET_TIME	SET_32_COUNTER	TEST_MODE	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC

Bits	Field Name	Description	Type	Reset
7	RTC_V_OPT	RTC date/time register selection: 0: Read access directly to dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG, WEEKS_REG) 1: Read access to static shadowed registers: (see GET_TIME bit).	RW	0
6	GET_TIME	When writing a 1 into this register, the content of the dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG and WEEKS_REG) is transferred into static shadowed registers. Each update of the shadowed registers needs to be done by re-asserting GET_TIME bit to 1 (i.e.: reset it to 0 and then re-write it to 1)	RW	0
5	SET_32_COUNTER	0: No action 1: set the 32-kHz counter with COMP_REG value. It must only be used when the RTC is frozen.	RW	0
4	TEST_MODE	0: functional mode 1: test mode (Auto compensation is enable when the 32-kHz counter reaches at its end)	RW	0
3	MODE_12_24	0: 24 hours mode 1: 12 hours mode (PM-AM mode) It is possible to switch between the two modes at any time without disturbed the RTC, read or write are always performed with the current mode.	RW	0

Bits	Field Name	Description	Type	Reset
2	AUTO_COMP	0: No auto compensation 1: Auto compensation enabled	RW	0
1	ROUND_30S	0: No update 1: When a one is written, the time is rounded to the closest minute. This bit is a toggle bit, the micro-controller can only write one and RTC clears it. If the micro-controller sets the ROUND_30S bit and then read it, the micro-controller will read one until the rounded to the closet.	RW	0
0	STOP_RTC	0: RTC is frozen 1: RTC is running	RW	0

Table 28. RTC_STATUS_REG

Address Offset	0x11		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC status register: NOTES: A dummy read of this register is necessary before each I^2C read in order to update the status register value.		
Type	RW		

7	6	5	4	3	2	1	0
POWER_UP	ALARM	EVENT_1D	EVENT_1H	EVENT_1M	EVENT_1S	RUN	Reserved

Bits	Field Name	Description	Type	Reset
7	POWER_UP	Indicates that a reset occurred (bit cleared to 0 by writing 1). POWER_UP is set by a reset, is cleared by writing one in this bit.	RW	1
6	ALARM	Indicates that an alarm interrupt has been generated (bit clear by writing 1). The alarm interrupt keeps its low level, until the micro-controller write 1 in the ALARM bit of the RTC_STATUS_REG register. The timer interrupt is a low-level pulse (15 µs duration).	RW	0
5	EVENT_1D	One day has occurred	RO	0
4	EVENT_1H	One hour has occurred	RO	0
3	EVENT_1M	One minute has occurred	RO	0
2	EVENT_1S	One second has occurred	RO	0
1	RUN	0: RTC is frozen 1: RTC is running This bit shows the real state of the RTC, indeed because of STOP_RTC signal was resynchronized on 32-kHz clock, the action of this bit is delayed.	RO	0
0	Reserved	Reserved bit	RO R returns 0s	0

Table 29. RTC_INTERRUPTS_REG

Address Offset	0x12		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC interrupt control register		
Type	RW		

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7	6	5	4	3	2	1	0
Reserved			IT_SLEEP_MASK_EN	IT_ALARM	IT_TIMER	EVERY	

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	IT_SLEEP_MASK_EN	1: Mask periodic interrupt while the TPS65911 device is in SLEEP mode. Interrupt event is back up in a register and occurred as soon as the TPS65911 device is no more in SLEEP mode. 0: Normal mode, no interrupt masked	RW	0
3	IT_ALARM	Enable one interrupt when the alarm value is reached (TC ALARM registers) by the TC registers	RW	0
2	IT_TIMER	Enable periodic interrupt 0: interrupt disabled 1: interrupt enabled	RW	0
1:0	EVERY	Interrupt period 00: every second 01: every minute 10: every hour 11: every day	RW	0x0

Table 30. RTC_COMP_LSB_REG

Address Offset	0x13	
Physical Address	**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC compensation register (LSB) Notes: This register must be written in 2-complement. This means that to add one 32-kHz oscillator period every hour, micro-controller needs to write FFFF into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG. To remove one 32-kHz oscillator period every hour, micro-controller needs to write 0001 into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG. The 7FFF value is forbidden.	
Type	RW	

7	6	5	4	3	2	1	0
RTC_COMP_LSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_LSB	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [LSB]	RW	0x00

Table 31. RTC_COMP_MSB_REG

Address Offset	0x14	
Physical Address	**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC compensation register (MSB) Notes: See RTC_COMP_LSB_REG Notes.	
Type	RW	

7	6	5	4	3	2	1	0
RTC_COMP_MSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_MSB	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [MSB]	RW	0x00

Table 32. RTC_RES_PROG_REG

Address Offset	0x15		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register containing oscillator resistance value		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		SW_RES_PROG					

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5:0	SW_RES_PROG	Value of the oscillator resistance	RW	0x27

Table 33. RTC_RESET_STATUS_REG

Address Offset	0x16		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for reset status		
Type	RW		

7	6	5	4	3	2	1	0
Reserved							RESET_STATUS

Bits	Field Name	Description	Type	Reset
7:1	Reserved	Reserved bit	RO R returns 0s	0x0
0	RESET_STATUS	This bit can only be set to one and is cleared when a manual reset or a POR (VBAT < 2.1)occur. If this bit is reset it means that the RTC has lost its configuration.	RW	0

Table 34. BCK1_REG

Address Offset	0x17		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.		
Type	RW		

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7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 35. BCK2_REG

Address Offset	0x18		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.		
Type	RW		

7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 36. BCK3_REG

Address Offset	0x19		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.		
Type	RW		

7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 37. BCK4_REG

Address Offset	0x1A		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.		
Type	RW		

7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 38. BCK5_REG

Address Offset	0x1B		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.		
Type	RW		

7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 39. PUADEN_REG

Address Offset	0x1C		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Pullup/pulldown control register.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	I2CCTLP	I2CSRP	PWRONP	SLEEPP	PWRHOLDP	HDRSTP	NRESPWRON2P

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	I2CCTLP	SDACTL and SCLCTL pullup control: 1: Pullup is enabled 0: Pullup is disabled	RW	0
5	I2CSRP	SDASR and SCLSR pullup control: 1: Pullup is enabled 0: Pullup is disabled	RW	0
4	PWRONP	PWRON pad pullup control: 1: Pullup is enabled 0: Pullup is disabled	RW	1
3	SLEEPP	SLEEP pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	PWRHOLDP	PWRHOLD pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
1	HDRSTP	HDRST pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
0	NRESPWRON2P	NRESPWRON2 pad control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1

Table 40. REF_REG

Address Offset	0x1D		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	Reference control register		
Type	RO		

7	6	5	4	3	2	1	0
Reserved						ST	

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Bits	Field Name	Description	Type	Reset
7:2	Reserved	Reserved bit	RO R returns 0s	0x00
1:0	ST	Reference state: ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Reserved ST[1:0] = 11: On low power (SLEEP) (Write access available in test mode only)	RO	0x1

Table 41. VRTC_REG

Address Offset	0x1E		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	VRTC internal regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				VRTC_OFFMASK	Reserved	ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3	VRTC_OFFMASK	VRTC internal regulator off mask signal: when 1, the regulator keeps its full-load capability during device OFF state. when 0, the regulator will enter in low-power mode during device OFF state. Note that VRTC is put in low-power mode when the device is on backup even if this bit is set to 1 (Default value: See boot configuration)	RW	0
2	Reserved	Reserved bit	RO R returns 0s	0
1:0	ST	Reference state: ST[1:0] = 00: Reserved ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Reserved ST[1:0] = 11: On low power (SLEEP) (Write access available in test mode only)	RO	0x1

Table 42. VIO_REG

Address Offset	0x20		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VIO control register		
Type	RW		

7	6	5	4	3	2	1	0
ILMAX		Reserved		SEL		ST	

Bits	Field Name	Description	Type	Reset
7:6	ILMAX	Select maximum load current: when 00: 0.6 A when 01: 1.0 A when 10: 1.5 A when 11: > 1.5 A	RW	0x0
5:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Output voltage selection (EEPROM bits): SEL[1:0] = 00: 1.5 V SEL[1:0] = 01: 1.8 V SEL[1:0] = 10: 2.5 V SEL[1:0] = 11: 3.3 V (Default value: see boot configuration)	RW	0x0
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 43. VDD1_REG

Address Offset	0x21		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD1 control register		
Type	RW		

7	6	5	4	3	2	1	0
VGAIN_SEL		ILMAX	TSTEP			ST	

Bits	Field Name	Description	Type	Reset
7:6	VGAIN_SEL	Select output voltage multiplication factor: G (EEPROM bits): when 00: x1 when 01: TBD when 10: x2 when 11: x3 (Default value:see boot configuration)	RW	0x0
5:4	ILMAX	Select maximum load current: when 0: 1.0 A when 1: > 1.5 A	RW	0
3:2	TSTEP	Time step: when changing the output voltage, the new value is reached through successive 12.5 mV voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is then: TSTEP[2:0] = 000: step duration is 0, step function is bypassed TSTEP[2:0] = 001: 12.5 mV/µs (sampling 3 Mhz) TSTEP[2:0] = 010: 9.4 mV/µs (sampling 3 Mhz × 3/4) TSTEP[2:0] = 011: 7.5 mV/µs (sampling 3 Mhz × 3/5) (default) TSTEP[2:0] = 100: 6.25 mV/µs(sampling 3 Mhz/2) TSTEP[2:0] = 101: 4.7 mV/µs(sampling 3 Mhz/3) TSTEP[2:0] = 110: 3.12 mV/µs(sampling 3 Mhz/4) TSTEP[2:0] = 111: 2.5 mV/µs(sampling 3 Mhz/5)	RW	0x3
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On, high-power mode ST[1:0] = 10: Off ST[1:0] = 11: On, low-power mode	RW	0x0

Table 44. VDD1_OP_REG

Address Offset	0x22		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)

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Table 44. VDD1_OP_REG (continued)

Description	VDD1 voltage selection register. This register can be accessed by both control and coltage scaling I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.
Type	RW

7	6	5	4	3	2	1	0
CMD	SEL						

Bits	Field Name	Description	Type	Reset
7	CMD	when 0: VDD1_OP_REG voltage is applied when 1: VDD1_SR_REG voltage is applied	RW	0
6:0	SEL	Output voltage (4 EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111: 1.5 V ... SEL[6:0] = 0111111: 1.35 V ... SEL[6:0] = 0110011: 1.2 V ... SEL[6:0] = 0000001 to 0000011: 0.6 V SEL[6:0] = 0000000: Off (0.0 V) Note: from SEL[6:0] = 3 to 75 (dec) Vout = (SEL[6:0] × 12.5 mV + 0.5625 V) × G (Default value: See boot configuration)	RW	0x00

Table 45. VDD1_SR_REG

Address Offset	0x23		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD1 voltage selection register. This register can be accessed by both control and voltage scaling dedicated I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL						

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:0	SEL	Output voltage selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111: 1.5 V ... SEL[6:0] = 0111111: 1.35 V ... SEL[6:0] = 0110011: 1.2 V ... SEL[6:0] = 0000001 to 0000011: 0.6 V SEL[6:0] = 0000000: Off (0.0 V) Note: from SEL[6:0] = 3 to 75 (dec) Vout = (SEL[6:0] × 12.5 mV + 0.5625 V) × G (Default value: See boot configuration)	RW	0x00

Table 46. VDD2_REG

Address Offset	0x24		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD2 control register		

Table 46. VDD2_REG (continued)

Type	RW

7	6	5	4	3	2	1	0
VGAIN_SEL		ILMAX	TSTEP			ST	

Bits	Field Name	Description	Type	Reset
7:6	VGAIN_SEL	Select output voltage multiplication factor (x1, x3 included in EEPROM bits): G when 00: x1 when 01: TBD when 10: x2 when 11: x3	RW	0x0
5:4	ILMAX	Select maximum load current: when 0: 1.0 A when 1: > 1.5 A	RW	0
3:2	TSTEP	Time step: when changing the output voltage, the new value is reached through successive 12.5 mV voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is then: TSTEP[2:0] = 000: step duration is 0, step function is bypassed TSTEP[2:0] = 001: 12.5 mV/µs (sampling 3 Mhz) TSTEP[2:0] = 010: 9.4 mV/µs (sampling 3 Mhz × 3/4) TSTEP[2:0] = 011: 7.5 mV/µs (sampling 3 Mhz × 3/5) (default) TSTEP[2:0] = 100: 6.25 mV/µs(sampling 3 Mhz/2) TSTEP[2:0] = 101: 4.7 mV/µs(sampling 3 Mhz/3) TSTEP[2:0] = 110: 3.12 mV/µs(sampling 3 Mhz/4) TSTEP[2:0] = 111: 2.5 mV/µs(sampling 3 Mhz/5)	RW	0x1
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On, high-power mode ST[1:0] = 10: Off ST[1:0] = 11: On, low-power mode	RW	0x0

Table 47. VDD2_OP_REG

Address Offset	0x25		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD2 voltage selection register. This register can be accessed by both control and voltage scaling dedicated I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
CMD	SEL						

Bits	Field Name	Description	Type	Reset
7	CMD	Command: when 0: VDD2_OP_REG voltage is applied when 1: VDD2_SR_REG voltage is applied	RW	0
6:0	SEL	Output voltage (4 EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111: 1.5 V ... SEL[6:0] = 0111111: 1.35 V ... SEL[6:0] = 0110011: 1.2 V ... SEL[6:0] = 0000001 to 0000011: 0.6 V SEL[6:0] = 0000000: Off (0.0 V) Note: from SEL[6:0] = 3 to 75 (dec) Vout= (SEL[6:0] × 12.5 mV + 0.5625 V) × G	RW	0x00

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Table 48. VDD2_SR_REG

Address Offset	0x26		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD2 voltage selection registe. This register can be accessed by both control and voltage scaling dedicated I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL						

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:0	SEL	Output voltage (EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111: 1.5 V ... SEL[6:0] = 0111111: 1.35V ... SEL[6:0] = 0110011: 1.2V ... SEL[6:0] = 0000001 to 0000011: 0.6V SEL[6:0] = 0000000: Off (0.0V) Note: from SEL[6:0] = 3 to 75 (dec) Vout= (SEL[6:0] × 12.5 mV + 0.5625 V) × G	RW	0x00

Table 49. VDDCRTL_REG

Address Offset	0x27		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDDCtrl, external FET controller		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						ST	

Bits	Field Name	Description	Type	Reset
7:2	Reserved	Reserved bit	RO R returns 0s	0x00
1:0	ST	Supply state (EEPROM dependent): ST[1:0] = 00: Off ST[1:0] = 01: On ST[1:0] = 10: Off ST[1:0] = 11: On	RW	0x0

Table 50. VDDCRTL_OP_REG

Address Offset	0x28		
Physical Address		**Instance**	(RESET DOMAIN: TURN OFF RESET)
Description	VDDCtrl voltage selection register. This register can be accessed by both control and voltage scaling dedicated I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
CMD	SEL						

Bits	Field Name	Description	Type	Reset
7	CMD	Command: when 0: VDDctrl_OP_REG voltage is applied when 1: VDDctrl_SR_REG voltage is applied	RW	0
6:0	SEL	Output voltage (4 EEPROM bits) selection: SEL[6:0] = 1000011 to 1111111: 1.4 V ... SEL[6:0] = 0110001: 1.2 V ... SEL[6:0] = 0010001: 0.8 V ... SEL[6:0] = 0000001: 0000011 0.6 V SEL[6:0] = 0000000: Off (0.0 V) Note: from SEL[6:0] = 3 to 64 (dec) Vout= (SEL[6:0] × 12.5 mV + 0.5625 V) (Default value: See boot configuration)	RW	0x00

Table 51. VDDCRTL_SR_REG

Address Offset	0x29		
Physical Address		**Instance**	(RESET DOMAIN: TURN OFF RESET)
Description	VDDCtrl voltage selection register. This register can be accessed by both control and voltage scaling dedicated I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL						

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:0	SEL	Output voltage (4 EEPROM bits) selection: SEL[6:0] = 1000011 to 1111111: 1.4 V ... SEL[6:0] = 0110001: 1.2 V ... SEL[6:0] = 0010001: 0.8 V ... SEL[6:0] = 0000001: 0000011: 0.6 V SEL[6:0] = 0000000: Off (0.0 V) Note: from SEL[6:0] = 3 to 64 (dec) Vout= (SEL[6:0] × 12.5 mV + 0.5625 V) (Default value:See boot configuration)	RW	0x03

Table 52. LDO1_REG

Address Offset	0x30		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO1 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
SEL						ST	

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Bits	Field Name	Description	Type	Reset
7:2	SEL	Supply voltage (EEPROM bits): SEL[7:2] = 00000: 000011: 1 V SEL[7:2] = 000100: 1 V SEL[7:2] = 000101: 1.05 V ... SEL[7:2] = 110001: 3.25 V SEL[7:2] = 110010: 3.3 V (Default value: See boot configuration)	RW	0x0
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 53. LDO2_REG

Address Offset	0x31		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO2 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
SEL						ST	

Bits	Field Name	Description	Type	Reset
7:2	SEL	Supply voltage (EEPROM bits): SEL[7:2] = 00000: 000011: 1 V SEL[7:2] = 000100: 1 V SEL[7:2] = 000101: 1.05 V ... SEL[7:2] = 110001: 3.25 V SEL[7:2] = 110010: 3.3 V (Default value: See boot configuration)	RW	0x0
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 54. LDO5_REG

Address Offset	0x32		
Physical Address		**Instance**	(RESET DOMAIN: TUROFF RESET)
Description	LDO5 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

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Bits	Field Name	Description	Type	Reset
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 55. LDO8_REG

Address Offset	0x33		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO8 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 56. LDO7_REG

Address Offset	0x34		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO7 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

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Bits	Field Name	Description	Type	Reset
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 57. LDO6_REG

Address Offset	0x35		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO6 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 58. LDO4_REG

Address Offset	0x36		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO4 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
SEL						ST	

Bits	Field Name	Description	Type	Reset
7:2	SEL	Supply voltage (EEPROM bits): SEL[7:2] = 00000: 00000: 0.8 V SEL[7:2] = 00000: 000001: 0.85 V SEL[7:2] = 00000: 000010: 0.9 V SEL[7:2] = 000100: 1 V SEL[7:2] = 000101: 1.05 V ... SEL[7:2] = 110001: 3.25 V SEL[7:2] = 110010: 3.3 V Applicable voltage selection TRACK LDO 0: 1 V to 3.3 V TRACK LDO 1: 0.8 V to 1.5 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 59. LDO3_REG

Address Offset	0x37		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO3 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 60. Therm_REG

Address Offset	0x38		
Physical Address		**Instance**	(RESET DOMAIN:
Description	Thermal control register		bits[5:2}: GENERAL RESET
Type	RW		bit[0] TURNOFF OFF RESET)

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7	6	5	4	3	2	1	0
Reserved		THERM_HD	THERM_TS	THERM_HDSEL		Reserved	THERM_STATE

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5	THERM_HD	Hot die detector output: when 0: the hot die threshold is not reached when 1: the hot die threshold is reached	RO	0
4	THERM_TS	Thermal shutdown detector output: when 0: the thermal shutdown threshold is not reached when 1: the thermal shutdown threshold is reached	RO	0
3:2	THERM_HDSEL	Temperature selection for hot-die detector: when 00: Low temperature threshold … when 11: High temperature threshold	RW	0x3
1	Reserved		RO R returns 0s	0
0	THERM_STATE	Thermal shutdown module enable signal: when 0: thermal shutdown module is disable when 1: thermal shutdown module is enable	RW	1

Table 61. BBCH_REG

Address Offset	0x39		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Back-up battery charger control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved					BBSEL		BBCHEN

Bits	Field Name	Description	Type	Reset
7:3	Reserved	Reserved bit	RO R returns 0s	0x00
2:1	BBSEL	Back up battery charge voltage selection: BBSEL[1:0] = 00: 3.0 V BBSEL[1:0] = 01: 2.52 V BBSEL[1:0] = 10: 3.15 V BBSEL[1:0] = 11: VBAT	RW	0x0
0	BBCHEN	Back up battery charge enable	RW	0

Table 62. DCDCCTRL_REG

Address Offset	0x3E		
Physical Address		**Instance**	RESET DOMAIN: bits [7:3]: TURNOFF OFF RESET bits [2:0]: GENERAL RESET
Description	DCDC control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	TRACK	VDD2_PSKIP	VDD1_PSKIP	VIO_PSKIP	DCDCCKEXT	DCDCCKSYNC	

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6	TRACK	1: Tracking mode: LDO4 output follows VDD1 setting when VDD1 active. See appendix for more information. 0: Normal LDO operation without tracking	RW	0
5	VDD2_PSKIP	VDD2 pulse skip mode enable (EEPROM bit) Default value: See boot configuration	RW	1
4	VDD1_PSKIP	VDD1 pulse skip mode enable (EEPROM bit) Default value: See boot configuration	RW	1
3	VIO_PSKIP	VIO pulse skip mode enable (EEPROM bit) Default value: See boot configuration	RW	1
2	DCDCCKEXT	This signal control the muxing of the GPIO2 pad: When 0: this pad is a GPIO When 1: this pad is used as input for an external clock used for the synchronisation of the DCDCs	RW	0
1:0	DCDCCKSYNC	DCDC clock configuration: DCDCCKSYNC[1:0] = 00: no synchronization of DCDC clocks DCDCCKSYNC[1:0] = 01: DCDC synchronous clock with phase shift DCDCCKSYNC[1:0] = 10: no synchronization of DCDC clocks DCDCCKSYNC[1:0] = 11: DCDC synchronous clock	RW	0x1

Table 63. DEVCTRL_REG

Address Offset	0x3F		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Device control register		
Type	RW		

7	6	5	4	3	2	1	0
PWR_OFF_SEQ	RTC_PWDN	CK32K_CTRL	SR_CTL_I2C_SEL	DEV_OFF_RST	DEV_ON	DEV_SLP	DEV_OFF

Bits	Field Name	Description	Type	Reset
7	PWR_OFF_SEQ	When 1, power-off will be sequencial, reverse of power-on sequence (first resource to power on will be the last to power off). When 0, all resources disabled at the same time	RW	0
6	RTC_PWDN	When 1, disable the RTC digital domain (clock gating and reset of RTC registers and logic). This register bit is not reset in BACKUP state.	RW	0
5	CK32K_CTRL	Internal 32-kHz clock source control bit (EEPROM bit): when 0, the internal 32-kHz clock source is the crystal oscillator or an external 32-kHz clock in case the crystal oscillator is used in bypass mode when 1, the internal 32-kHz clock source is the RC oscillator.	RW	0
4	SR_CTL_I2C_SEL	Voltage scaling registers access control bit: when 0: access to registers by voltage scaling I^2C when 1: access to registers by control I^2C. The voltage scaling registers are: VDD1_OP_REG, VDD1_SR_REG, VDD2_OP_REG, VDD2_SR_REG, VDDCtrl_OP_REG, and VDDCtrl_SR_REG.	RW	1

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Bits	Field Name	Description	Type	Reset
3	DEV_OFF_RST	Write 1 will start an ACTIVE-to-OFF or SLEEP-to-OFF device state transition (switch-off event) and activate reset of the digital core. This bit is cleared in OFF state.	RW	0
2	DEV_ON	Write 1 will maintain the device on (ACTIVE or SLEEP device state) (if DEV_OFF = 0 and DEV_OFF_RST = 0). EEPROM bit (Default value:See boot configuration)	RW	0
1	DEV_SLP	Write 1 allows SLEEP device state (if DEV_OFF = 0 and DEV_OFF_RST = 0). Write '0' will start an SLEEP-to-ACTIVE device state transition (wake-up event) (if DEV_OFF = 0 and DEV_OFF_RST = 0). This bit is cleared in OFF state.	RW	0
0	DEV_OFF	Write 1 will start an ACTIVE-to-OFF or SLEEP-to-OFF device state transition (switch-off event). This bit is cleared in OFF state.	RW	0

Table 64. DEVCTRL2_REG

Address Offset	0x40		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Device control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	DCDC_SLEEP_LVL	TSLOT_LENGTH		SLEEPSIG_POL	PWON_LP_OFF	PWON_LP_RST	IT_POL

Bits	Field Name	Description	Type	Reset
7	Reserved		RO R returns 0s	0
6	DCDC_SLEEP_LVL	When 1, DCDC output level in SLEEP mode is VDDx_SR_REG, to be other than 0 V. When 0, no effect	RW	0
5:4	TSLOT_LENGTH	Time slot duration programming (EEPROM bit): When 00: 0 µs When 01: 200 µs When 10: 500 µs When 11: 2 ms (Default value: See boot configuration)	RW	0x3
3	SLEEPSIG_POL	When 1, SLEEP signal active-high When 0, SLEEP signal active-low	RW	0
2	PWON_LP_OFF	When 1, allows device turn-off after a PWON Long Press (signal low) (EEPROM bits). (Default value: See boot configuration)	RW	1
1	PWON_LP_RST	When 1, allows digital core reset when the device is OFF (EEPROM bit). (Default value: See boot configuration)	RW	0
0	IT_POL	INT1 interrupt pad polarity control signal (EEPROM bit): When 0, active low When 1, active high (Default value: See boot configuration)	RW	0

Table 65. SLEEP_KEEP_LDO_ON_REG

Address Offset	0x41		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	When corresponding control bit = 0 in EN1_ LDO_ASS register (default setting): Configuration Register keeping the full load capability of LDO regulator (ACTIVE mode) during the SLEEP state of the device. When control bit = 1, LDO regulator full load capability (ACTIVE mode) is maintained during device SLEEP state. When control bit = 0, the LDO regulator is set or stay in low-power mode during device SLEEP state(but then supply state can be overwritten programming ST[1:0]). Control bit value has no effect if the LDO regulator is off. When corresponding control bit = 1 in EN1_ LDO_ASS register: Configuration Register setting the LDO regulator state driven by SCLSR_EN1 signal low level (when SCLSR_EN1 is high the regulator is on, full power): - the regulator is set off if its corresponding Control bit = 0 in SLEEP_KEEP_LDO_ON register (default) - the regulator is set in low-power mode if its corresponding control bit = 1 in SLEEP_KEEP_LDO_ON register		
Type	RW		

7	6	5	4	3	2	1	0
LDO3_KEEPON	LDO4_KEEPON	LDO7_KEEPON	LDO8_KEEPON	LDO5_KEEPON	LDO2_KEEPON	LDO1_KEEPON	LDO6_KEEPON

Bits	Field Name	Description	Type	Reset
7	LDO3_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
6	LDO4_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
5	LDO7_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
4	LDO8_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
3	LDO5_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
2	LDO2_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
1	LDO1_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
0	LDO6_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0

Table 66. SLEEP_KEEP_RES_ON_REG

Address Offset	0x42	
Physical Address		**Instance**
Description	Configuration Register keeping, during the SLEEP state of the device (but then supply state can be overwritten programming ST[1:0]): - the full load capability of LDO regulator (ACTIVE mode), - The PWM mode of DCDC converter - 32-kHz clock output - Register access though I^2C interface (keeping the internal high speed clock on) - Die Thermal monitoring on Control bit value has no effect if the resource is off.	
Type	RW	

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7	6	5	4	3	2	1	0
THERM_KEEPON	CLKOUT32K_KEEPON	VRTC_KEEPON	I2CHS_KEEPON	Reserved	VDD2_KEEPON	VDD1_KEEPON	VIO_KEEPON

Bits	Field Name	Description	Type	Reset
7	THERM_KEEPON	When 1, thermal monitoring is maintained during device SLEEP state. When 0, thermal monitoring is turned off during device SLEEP state.	RW	0
6	CLKOUT32K_KEEPON	When 1, CLK32KOUT output is maintained during device SLEEP state. When 0, CLK32KOUT output is set low during device SLEEP state.	RW	0
5	VRTC_KEEPON	When 1, LDO regulator full load capability (ACTIVE mode) is maintained during device SLEEP state. When 0, the LDO regulator is set or stays in low-power mode during device SLEEP state.	RW	0
4	I2CHS_KEEPON	When 1, high speed internal clock is maintained during device SLEEP state. When 0, high speed internal clock is turned off during device SLEEP state.	RW	0
3	Reserved		RO	0
2	VDD2_KEEPON	When 1, VDD2 SMPS PWM mode is maintained during device SLEEP state. No effect if VDD2 working mode is PFM. When 0, VDD2 SMPS PFM mode is set during device SLEEP state.	RW	0
1	VDD1_KEEPON	When 1, VDD1 SMPS PWM mode is maintained during device SLEEP state. No effect if VDD1 working mode is PFM. When 0, VDD1 SMPS PFM mode is set during device SLEEP state.	RW	0
0	VIO_KEEPON	When 1, VIO SMPS PWM mode is maintained during device SLEEP state. No effect if VIO working mode is PFM. When 0, VIO SMPS PFM mode is set during device SLEEP state.	RW	0

Table 67. SLEEP_SET_LDO_OFF_REG

Address Offset	0x43		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Configuration Register turning-off LDO regulator during the SLEEP state of the device. Corresponding *_KEEP_ON control bit in SLEEP_KEEP_RES_ON register should be 0 to make this *_SET_OFF control bit effective		
Type	RW		

7	6	5	4	3	2	1	0
LDO3_SETOFF	LDO4_SETOFF	LDO7_SETOFF	LDO8_SETOFF	LDO5_SETOFF	LDO2_SETOFF	LDO1_SETOFF	LDO6_SETOFF

Bits	Field Name	Description	Type	Reset
7	LDO3_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
6	LDO4_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
5	LDO7_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0

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Bits	Field Name	Description	Type	Reset
4	LDO8_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
3	LDO5_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
2	LDO2_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
1	LDO1_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
0	LDO6_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0

Table 68. SLEEP_SET_RES_OFF_REG

Address Offset	0x44		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Configuration Register turning-off SMPS regulator during the SLEEP state of the device. Corresponding *_KEEP_ON control bit in SLEEP_KEEP_RES_ON2 register should be 0 to make this *_SET_OFF control bit effective. Supplies voltage expected after their wake-up (SLEEP-to-ACTIVE state transition) can also be programmed.		
Type	RW		

7	6	5	4	3	2	1	0
DEFAULT_VOLT	Reserved		SPARE_SETOFF	VDDCTRL_SETOFF	VDD2_SETOFF	VDD1_SETOFF	VIO_SETOFF

Bits	Field Name	Description	Type	Reset
7	DEFAULT_VOLT	When 1, default voltages (register value after switch-on) will be applied to all resources during SLEEP-to-ACTIVE transition. When 0, voltages programmed before the ACTIVE-to-SLEEP state transition will be used to turned-on supplies during SLEEP-to-ACTIVE state transition.	RW	0
6:5	Reserved		RO R returns 0s	0x0
4	SPARE_SETOFF	Spare bit	RW	0
3	VDDCTRL_SETOFF	When 1, SMPS is turned off during device SLEEP state. When 0, No effect.	RW	0
2	VDD2_SETOFF	When 1, SMPS is turned off during device SLEEP state. When 0, No effect.	RW	0
1	VDD1_SETOFF	When 1, SMPS is turned off during device SLEEP state. When 0, No effect.	RW	0
0	VIO_SETOFF	When 1, SMPS is turned off during device SLEEP state. When 0, No effect.	RW	0

Table 69. EN1_LDO_ASS_REG

Address Offset	0x45		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF RESET)

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Table 69. EN1_LDO_ASS_REG (continued)

Description	Configuration Register setting the LDO regulators, driven by the multiplexed SCLSR_EN1 signal. When control bit = 1, LDO regulator state is driven by the SCLSR_EN1 control signal and is also defined though SLEEP_KEEP_LDO_ON register setting: When SCLSR_EN1 is high the regulator is on, When SCLSR_EN1 is low: - the regulator is off if its corresponding Control bit = 0 in SLEEP_KEEP_LDO_ON register - the regulator is working in low-power mode if its corresponding control bit = 1 in SLEEP_KEEP_LDO_ON register When control bit = 0 no effect: LDO regulator state is driven though registers programming and the device state Any control bit of this register set to 1 will disable the I^2C SR Interface functionality
Type	RW

7	6	5	4	3	2	1	0
LDO3_EN1	LDO4_EN1	LDO7_EN1	LDO8_EN1	LDO5_EN1	LDO2_EN1	LDO1_EN1	LDO6_EN1

Bits	Field Name	Description	Type	Reset
7	LDO3_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
6	LDO4_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
5	LDO7_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
4	LDO8_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
3	LDO5_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
2	LDO2_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
1	LDO1_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
0	LDO6_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0

Table 70. EN1_SMPS_ASS_REG

Address Offset	0x46		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF RESET)
Description	Configuration Register setting the SMPS Supplies driven by the multiplexed SCLSR_EN1 signal. When control bit = 1, SMPS Supply state and voltage is driven by the SCLSR_EN1 control signal and is also defined though SLEEP_KEEP_RES_ON register setting. When control bit = 0 no effect: SMPS Supply state is driven though registers programming and the device state. Any control bit of this register set to 1 will disable the I^2C SR Interface functionality		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			SPARE_EN1	VDDCTRL_EN1	VDD2_EN1	VDD1_EN1	VIO_EN1

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO R returns 0s	0x0
4	SPARE_EN1	Spare bit	RW	0

Bits	Field Name	Description	Type	Reset
3	VDDCTRL_EN1	When control bit = 1: When EN1 is high the supply voltage is programmed though VDDCtrl_OP_REG register, and it can also be programmed off. When EN1 is low the supply voltage is programmed though VDDCtrl_SR_REG register, and it can also be programmed off. When control bit = 0: No effect: Supply state is driven though registers programming and the device state	RW	0
2	VDD2_EN1	When control bit = 1: When SCLSR_EN1 is high the supply voltage is programmed though VDD2_OP_REG register, and it can also be programmed off. When SCLSR_EN1 is low the supply voltage is programmed though VDD2_SR_REG register, and it can also be programmed off. When SCLSR_EN1 is low and SLEEP_KEEP_RES_ON = 1 the SMPS is working in low-power mode, if not tuned off through VDD2_SR_REG register. When control bit = 0 No effect: Supply state is driven though registers programming and the device state	RW	0
1	VDD1_EN1	When 1: When SCLSR_EN1 is high the supply voltage is programmed though VDD1_OP_REG register, and it can also be programmed off. When SCLSR_EN1 is low the supply voltage is programmed though VDD1_SR_REG register, and it can also be programmed off. When SCLSR_EN1 is low and SLEEP_KEEP_RES_ON = 1 the SMPS is working in low-power mode, if not tuned off though VDD1_SR_REG register. When control bit = 0 no effect: supply state is driven though registers programming and the device state	RW	0
0	VIO_EN1	When control bit = 1, supply state is driven by the SCLSR_EN1 control signal and is also defined though SLEEP_KEEP_RES_ON register setting: When SCLSR_EN1 is high the supply is on, When SCLSR_EN1 is low: - the supply is off (default) or the SMPS is working in low-power mode if its corresponding control bit = 1 in SLEEP_KEEP_RES_ON register When control bit = 0 No effect: SMPS state is driven though registers programming and the device state	RW	0

Table 71. EN2_LDO_ASS_REG

Address Offset	0x47		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF RESET)
Description	Configuration Register setting the LDO regulators, driven by the multiplexed SDASR_EN2 signal. When control bit = 1, LDO regulator state is driven by the SDASR_EN2 control signal and is also defined though SLEEP_KEEP_LDO_ON register setting: When SDASR_EN2 is high the regulator is on, When SCLSR_EN2 is low: - the regulator is off if its corresponding Control bit = 0 in SLEEP_KEEP_LDO_ON register - the regulator is working in low-power mode if its corresponding control bit = 1 in SLEEP_KEEP_LDO_ON register When control bit = 0 no effect: LDO regulator state is driven though registers programming and the device state Any control bit of this register set to 1 will disable the I^2C SR Interface functionality		
Type	RW		

7	6	5	4	3	2	1	0
LDO3_EN2	LDO4_EN2	LDO7_EN2	LDO8_EN2	LDO5_EN2	LDO2_EN2	LDO1_EN2	LDO6_EN2

Bits	Field Name	Description	Type	Reset
7	LDO3_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
6	LDO4_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
5	LDO7_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
4	LDO8_EN2	Setting supply state control though SDASR_EN2 signal	RW	0

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Bits	Field Name	Description	Type	Reset
3	LDO5_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
2	LDO2_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
1	LDO1_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
0	LDO6_EN2	Setting supply state control though SDASR_EN2 signal	RW	0

Table 72. EN2_SMPS_ASS_REG

Address Offset	0x48		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF RESET)
Description	Configuration Register setting the SMPS Supplies driven by the multiplexed SDASR_EN2 signal. When control bit = 1, SMPS Supply state and voltage is driven by the SDASR_EN2 control signal and is also defined though SLEEP_KEEP_RES_ON register setting. When control bit = 0 no effect: SMPS Supply state is driven though registers programming and the device state Any control bit of this register set to 1 will disable the I^2C SR Interface functionality		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			SPARE_EN2	VDDCTRL_EN2	VDD2_EN2	VDD1_EN2	VIO_EN2

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO R returns 0s	0x0
4	SPARE_EN2	Spare bit	RW	0
3	VDDCTRL_EN2	When control bit = 1: When EN2 is high the supply voltage is programmed though VDDCtrl_OP_REG register, and it can also be programmed off.. When EN2 is low the supply voltage is programmed though VDDCtrl_SR_REG register, and it can also be programmed off. When EN2 is low and and VDDCtrl_KEEPON = 1 the SMPS is working in low-power mode, if not tuned off though VDDCtrl_SR_REG register. When control bit = 0 no effect: Supply state is driven though registers programming and the device state	RW	0
2	VDD2_EN2	When control bit = 1: When SDASR_EN2 is high the supply voltage is programmed though VDD2_OP_REG register, and it can also be programmed off. When SDASR_EN2 is low the supply voltage is programmed though VDD2_SR_REG register, and it can also be programmed off. When SDASR_EN2 is low and and SLEEP_KEEP_RES_ON = 1 the SMPS is working in low-power mode, if not tuned off though VDD2_SR_REG register. When control bit = 0 no effect: Supply state is driven though registers programming and the device state	RW	0
1	VDD1_EN2	When control bit = 1: When SDASR_EN2 is high the supply voltage is programmed though VDD1_OP_REG register, and it can also be programmed off. When SDASR_EN2 is low the supply voltage is programmed though VDD1_SR_REG register, and it can also be programmed off. When SDASR_EN2 is low and and SLEEP_KEEP_RES_ON = 1 the SMPS is working in low-power mode, if not tuned off though VDD1_SR_REG register. When control bit = 0 no effect: supply state is driven though registers programming and the device state	RW	0

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Bits	Field Name	Description	Type	Reset
0	VIO_EN2	When control bit = 1, supply state is driven by the SCLSR_EN2 control signal and is also defined though SLEEP_KEEP_RES_ON register setting: When SDASR _EN2 is high the supply is on, When SDASR _EN2 is low : - the supply is off (default) or the SMPS is working in low-power mode if its corresponding control bit = 1 in SLEEP_KEEP_RES_ON register When control bit = 0 no effect: SMPS state is driven though registers programming and the device state	RW	0

Table 73. INT_STS_REG

Address Offset	0x50		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Interrupt status register: The interrupt status bit is set to 1 when the associated interrupt event is detected. Interrupt status bit is cleared by writing 1.		
Type	RW		

7	6	5	4	3	2	1	0
RTC_PERIOD_IT	RTC_ALARM_IT	HOTDIE_IT	PWRHOLD_R_IT	PWRON_LP_IT	PWRON_IT	VMBHI_IT	PWRHOLD_F_IT

Bits	Field Name	Description	Type	Reset
7	RTC_PERIOD_IT	RTC period event interrupt status.	RW W1 to Clr	0
6	RTC_ALARM_IT	RTC alarm event interrupt status.	RW W1 to Clr	0
5	HOTDIE_IT	Hot-die event interrupt status.	RW W1 to Clr	0
4	PWRHOLD_R_IT	Rising PWRHOLD event interrupt status.	RW W1 to Clr	0
3	PWRON_LP_IT	PWRON Long Press event interrupt status.	RW W1 to Clr	0
2	PWRON_IT	PWRON event interrupt status.	RW W1 to Clr	0
1	VMBHI_IT	VBAT > VMHI event interrupt status	RW W1 to Clr	0
0	PWRHOLD_F_IT	Falling PWRHOLD event interrupt status.	RW W1 to Clr	0

Table 74. INT_MSK_REG

Address Offset	0x51		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Interrupt mask register: When *_IT_MSK is set to 1, the associated interrupt is masked: INT1 signal is not activated, but *_IT interrupt status bit is updated. When *_IT_MSK is set to 0, the associated interrupt is enabled: INT1 signal is activated, *_IT is updated.		
Type	RW		

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7	6	5	4	3	2	1	0
RTC_PERIOD_IT_MSK	RTC_ALARM_IT_MSK	HOTDIE_IT_MSK	PWRHOLD_R_IT_MSK	PWRON_LP_IT_MSK	PWRON_IT_MSK	VMBHI_IT_MSK	PWRHOLD_F_IT_MSK

Bits	Field Name	Description	Type	Reset
7	RTC_PERIOD_IT_MSK	RTC period event interrupt mask.	RW	1
6	RTC_ALARM_IT_MSK	RTC alarm event interrupt mask.	RW	1
5	HOTDIE_IT_MSK	Hot die event interrupt mask.	RW	1
4	PWRHOLD_R_IT_MSK	PWRHOLD rising-edge event interrupt mask.	RW	1
3	PWRON_LP_IT_MSK	PWRON Long Press event interrupt mask.	RW	1
2	PWRON_IT_MSK	PWRON event interrupt mask.	RW	1
1	VMBHI_IT_MSK	VBAT > VMBHI event interrupt mask. When 0, enable the device automatic switch on at BACKUP-to-OFF or NO SUPPLY-to-OFF device state transition (EEPROM bit) (Default value: See boot configuration)	RW	1
0	PWRHOLD_F_IT_MSK	PWRHOLD falling-edge event interrupt mask.	RW	1

Table 75. INT_STS2_REG

Address Offset	0x52		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Interrupt status register: The interrupt status bit is set to 1 when the associated interrupt event is detected. Interrupt status bit is cleared by writing 1.		
Type	RW		

7	6	5	4	3	2	1	0
GPIO3_F_IT	GPIO3_R_IT	GPIO2_F_IT	GPIO2_R_IT	GPIO1_F_IT	GPIO1_R_IT	GPIO0_F_IT	GPIO0_R_IT

Bits	Field Name	Description	Type	Reset
7	GPIO3_F_IT	GPIO3 falling-edge detection interrupt status	RW W1 to Clr	0
6	GPIO3_R_IT	GPIO3 rising-edge detection interrupt status	RW W1 to Clr	0
5	GPIO2_F_IT	GPIO2 falling-edge detection interrupt status	RW W1 to Clr	0
4	GPIO2_R_IT	GPIO2 rising-edge detection interrupt status	RW W1 to Clr	0
3	GPIO1_F_IT	GPIO1 falling-edge detection interrupt status	RW W1 to Clr	0
2	GPIO1_R_IT	GPIO1 rising-edge detection interrupt status	RW W1 to Clr	0
1	GPIO0_F_IT	GPIO0 falling-edge detection interrupt status	RW W1 to Clr	0
0	GPIO0_R_IT	GPIO0 rising-edge detection interrupt status	RW W1 to Clr	0

Table 76. INT_MSK2_REG

Address Offset	0x53		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Interrupt mask register: When *_IT_MSK is set to 1, the associated interrupt is masked: INT1 signal is not activated, but *_IT interrupt status bit is updated. When *_IT_MSK is set to 0, the associated interrupt is enabled: INT1 signal is activated, *_IT is updated.		
Type	RW		

7	6	5	4	3	2	1	0
GPIO3_F_IT_MSK	GPIO3_R_IT_MSK	GPIO2_F_IT_MSK	GPIO2_R_IT_MSK	GPIO1_F_IT_MSK	GPIO1_R_IT_MSK	GPIO0_F_IT_MSK	GPIO0_R_IT_MSK

Bits	Field Name	Description	Type	Reset
7	GPIO3_F_IT_MSK	GPIO3 falling-edge detection interrupt mask.	RW	1
6	GPIO3_R_IT_MSK	GPIO3 rising-edge detection interrupt mask.	RW	1
5	GPIO2_F_IT_MSK	GPIO2 falling-edge detection interrupt mask.	RW	1
4	GPIO2_R_IT_MSK	GPIO2 rising-edge detection interrupt mask.	RW	1
3	GPIO1_F_IT_MSK	GPIO1 falling-edge detection interrupt mask.	RW	1
2	GPIO1_R_IT_MSK	GPIO1 rising-edge detection interrupt mask.	RW	1
1	GPIO0_F_IT_MSK	GPIO0 falling-edge detection interrupt mask.	RW	1
0	GPIO0_R_IT _MSK	GPIO0 rising-edge detection interrupt mask.	RW	1

Table 77. INT_STS3_REG

Address Offset	0x54		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Interrupt status register: The interrupt status bit is set to 1 when the associated interrupt event is detected. Interrupt status bit is cleared by writing 1.		
Type	RW		

7	6	5	4	3	2	1	0
PWRDN_IT	VMBCH2_L_IT	VMBCH2_H_IT	WTCHDG_IT	GPIO5_F_IT	GPIO5_R_IT	GPIO4_F_IT	GPIO4_R_IT

Bits	Field Name	Description	Type	Reset
7	PWRDN_IT	PWRDN reset input high detected	RW W1 to Clr	0
6	VMBCH2_L_IT	Comparator2 input below threshold detection interrupt status	RW W1 to Clr	0
5	VMBCH2_H_IT	Comparator2 input above threshold detection interrupt status	RW W1 to Clr	0
4	WTCHDG_IT	Watchdog interrupt status	RW W1 to Clr	0
3	GPIO5_F_IT	GPIO5 falling-edge detection interrupt status	RW W1 to Clr	0
2	GPIO5_R_IT	GPIO5 rising-edge detection interrupt status	RW W1 to Clr	0

Bits	Field Name	Description	Type	Reset
1	GPIO4_F_IT	GPIO4 falling-edge detection interrupt status	RW W1 to Clr	0
0	GPIO4_R_IT	GPIO4 rising-edge detection interrupt status	RW W1 to Clr	0

Table 78. INT_MSK3_REG

Address Offset	0x55		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Interrupt mask register: When *_IT_MSK is set to 1, the associated interrupt is masked: INT1 signal is not activated, but *_IT interrupt status bit is updated. When *_IT_MSK is set to 0, the associated interrupt is enabled: INT1 signal is activated, *_IT is updated.		
Type	RW		

7	6	5	4	3	2	1	0
PWRDN_IT_MSK	VMBCH2_L_IT_MSK	VMBCH2_H_IT_MSK	WTCHDG_IT_MSK	GPIO5_F_IT_MSK	GPIO5_R_IT_MSK	GPIO4_F_IT_MSK	GPIO4_R_IT_MSK

Bits	Field Name	Description	Type	Reset
7	PWRDN_IT_MSK	PWRDN interrupt mask	RW	1
6	VMBCH2_L_IT_MSK	Comparator2 input below threshold detection interrupt mask	RW	1
5	VMBCH2_H_IT_MSK	Comparator2 input above threshold detection interrupt mask	RW	1
4	WTCHDG_IT_MSK	Watchdog interrupt mask.	RW	1
3	GPIO5_F_IT_MSK	GPIO5 falling-edge detection interrupt mask.	RW	1
2	GPIO5_R_IT_MSK	GPIO5 rising-edge detection interrupt mask.	RW	1
1	GPIO4_F_IT_MSK	GPIO4 falling-edge detection interrupt mask.	RW	1
0	GPIO4_R_IT_MSK	GPIO4 rising-edge detection interrupt mask.	RW	1

Table 79. GPIO0_REG

Address Offset	0x60		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO0 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_SLEEP	Reserved	GPIO_ODEN	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7	GPIO_SLEEP	1: as GPO, force low 0: No impact, keep as in active mode	RW	0
6	Reserved	Reserved bit	RO R returns 0s	0

Bits	Field Name	Description	Type	Reset
5	GPIO_ODEN	Selection of output mode, EEPROM bit 0: Push-pull output 1: Open-drain output (Default value: See boot configuration) GPIO assigned to power-up sequence, this bit will be set to 1 by a TURNOFF reset	RW	0
4	GPIO_DEB	GPIO input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	0
2	GPIO_CFG	Configuration of the GPIO pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output (Default value: See boot configuration)	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode GPIO assigned to power-up sequence, this bit will be in TURNOFF reset	RW	0

Table 80. GPIO1_REG

Address Offset	0x61		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO1 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		GPIO_SEL	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO R returns 0s	0x0
5	GPIO_SEL	Select signal to be available at GPIO when configured as output: 0: GPIO_SET 1: LED1 out	RW	0
4	GPIO_DEB	GPIO input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

Table 81. GPIO2_REG

Address Offset	0x62		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO2 configuration register		
Type	RW		

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7	6	5	4	3	2	1	0
GPIO_SLEEP	Reserved		GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7	GPIO_SLEEP	1: as GPO, force low 0: no impact, keep as in active mode	RW	0
6:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled GPIO assigned to power-up sequence, this bit will be set to 0 by a TURNOFF reset	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output (Default value: See boot configuration) GPIO assigned to power-up sequence, this bit will be set to 1 by a TURNOFF reset	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode GPIO assigned to power-up sequence, this bit will be in TURNOFF reset	RW	0

Table 82. GPIO3_REG

Address Offset	0x63		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO3 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	GPIO_SEL		GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7	Reserved		RO R returns 0s	0
6:5	GPIO_SEL	Select signal to be available at GPIO when configured as output: 00: GPIO_SET 01: LED2 out 10: PWM out	RW	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

Table 83. GPIO4_REG

Address Offset	0x64		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO4 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

Table 84. GPIO5_REG

Address Offset	0x65		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO5 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

Table 85. GPIO6_REG

Address Offset	0x66		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO6 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_SLEEP	Reserved		GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7	GPIO_SLEEP	1: as GPO, force low 0: no impact, keep as in active mode	RW	0
6:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled GPIO assigned to power-up sequence, this bit will be set to 0 by a TURNOFF reset	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output (Default value: See boot configuration) GPIO assigned to power-up sequence, this bit will be set to 1 by a TURNOFF reset	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode GPIO assigned to power-up sequence, this bit will be in TURNOFF reset	RW	0

Table 86. GPIO7_REG

Address Offset	0x67		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO7 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_SLEEP	Reserved		GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7	GPIO_SLEEP	1: as GPO, force low 0: no impact, keep as in active mode	RW	0
6:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled GPIO assigned to power-up sequence, this bit will be set to 0 by a TURNOFF reset	RW	1

Bits	Field Name	Description	Type	Reset
2	GPIO_CFG	Configuration of the GPIO pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output (Default value: See boot configuration) GPIO assigned to power-up sequence, this bit will be set to 1 by a TURNOFF reset	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode GPIO assigned to power-up sequence, this bit will be in TURNOFF reset	RW	0

Table 87. GPIO8_REG

Address Offset	0x68		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO8 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		GPIO_SEL	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO R returns 0s	0x0
5	GPIO_SEL	Select signal to be available at GPIO when configured as output: 0: GPIO_SET 1: LED1 out	RW	0
4	GPIO_DEB	GPIO input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

Table 88. WATCHDOG_REG

Address Offset	0x69		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Watchdog		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				WTCHDG_MODE	WTCHDG_TIME		

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Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO R returns 0s	0x0
3	WTCHDG_MODE	0: Periodic operation: A periodical interrupt is generated based on WTCHDG_TIME setting. IC will generate WTCHDOG shutdown if interrupt is not cleared during the period. 1: Interrupt mode: IC will generate WTCHDOG shutdown if an interrupt is pending (no cleared) more than WTCHDG_TIME s.	RW	0
2:0	WTCHDG_TIME	000: Watchdog disabled 001: 5 seconds 010: 10 seconds 011: 20 Seconds 100: 40 seconds 101: 60 seconds 110: 80 seconds 111: 100 seconds (EEPROM bit) (Default value: See boot configuration)	RW	0x0

Table 89. VMBCH_REG

Address Offset	0x6A		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Comparator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		VMBCH_SEL					Reserved

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO R returns 0s	0x0
5:1	VMBCH_SEL	Battery voltage comparator threshold (EEPROM) 11000 to 11111: 3.5 V 10111: 3.45 V ... 01110: 3 V (default) ... 00101: 2.55 V 00001 to 00100: 2.5 V 00000: Bypass (Default value: See boot configuration)	RW	0x00
0	Reserved		RO R returns 0s	0

Table 90. VMBCH2_REG

Address Offset	0x6B		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Comparator for detecting battery discharge below threshold level		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		VMBDCH2_SEL					VMBDCH2_DEB

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO R returns 0s	0x0
5:1	VMBDCH2_SEL	Battery voltage comparator threshold 11000 to 11111: 3.5 V 10111: 3.45 V ... 00101: 2.55 V 00001 to 00100: 2.5 V 00000: Bypass	RW	0x00
0	VMBDCH2_DEB	Comp2 input debouncing time configuration: When 0, the debouncing is 91.5 µs using a 30.5 µs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0

Table 91. LED_CTRL1_REG

Address Offset	0x6C		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	LED ON/OFF control register.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			LED2_PERIOD			LED1_PERIOD	

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO R returns 0s	0x0
5:3	LED2_PERIOD	Period of LED2 signal: 000: LED2 OFF 001: 0.125 s 010: 0.25 s ... 110: 4 s 111: 8 s	RW	0x0
2:0	LED1_PERIOD	Period of LED1 signal: 000: LED1 OFF 001: 0.125 s 010: 0.25 s ... 10: 2 s 110: 4 s 111: 8 s	RW	0x0

Table 92. LED_CTRL2_REG1

Address Offset	0x6D		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	LED ON/OFF control register.		
Type	RW		

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7	6	5	4	3	2	1	0
Reserved		LED2_SEQ	LED1_SEQ	LED2_ON_TIME		LED1_ON_TIME	

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO R returns 0s	0x0
5	LED2_SEQ	When 1, LED2 will repeat 2 pulse sequence: ON (ON_TIME) - OFF (ON TIME) - ON (ON TIME) - OFF remainder of the period When 0, LED2 will generate 1 pulse: ON (ON_TIME) - OFF (ON TIME))	RW	0
4	LED1_SEQ	When 1, LED1 will repeat 2 pulse sequence: ON (ON_TIME) - OFF (ON TIME) - ON (ON TIME) - OFF remainder of the period. When 0, LED1 will generate 1 pulse: ON (ON_TIME) - OFF (ON TIME))	RW	0
3:2	LED2_ON_TIME	LED2 ON time: 00: 62.5 ms 01: 125 ms 10: 250 ms 11: 500 ms	RW	0x0
1:0	LED1_ON_TIME	LED1 ON time: 00: 62.5 ms 01: 125 ms 10: 250 ms 11: 500 ms	RW	0x0

Table 93. PWM_CTRL1_REG

Address Offset	0x6E		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	PWM frequency		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						PWM_FREQ	

Bits	Field Name	Description	Type	Reset
7:2	Reserved	Reserved bit	RO R returns 0s	0x00
1:0	PWM_FREQ	Frequency of PWM: 00: 500 Hz 01: 250 Hz 10: 125 Hz 11: 62.5 Hz	RW	0x0

Table 94. PWM_CTRL2_REG

Address Offset	0x6F		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	PWM duty cycle.		
Type	RW		

7	6	5	4	3	2	1	0
FREQ_DUTY_CYCLE							

Bits	Field Name	Description	Type	Reset
7:0	FREQ_DUTY_CYCLE	Duty cycle of PWM: 00000000: 0/256 ... 11111111: 255/256	RW	0x00

Table 95. SPARE_REG

Address Offset	0x70		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Spare functional register		
Type	RW		

7	6	5	4	3	2	1	0
SPARE							

Bits	Field Name	Description	Type	Reset
7:0	SPARE	Spare bits	RW	0x00

Table 96. VERNUM_REG

Address Offset	0x80		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Silicon version number		
Type	RW		

7	6	5	4	3	2	1	0
READ_BOOT	Reserved			VERNUM			

Bits	Field Name	Description	Type	Reset
7	READ_BOOT	To enable the read of the BOOT mode if you want to enter JTAG mode, this be must set to 1.	RW	0
6:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:0	VERNUM	Value depending on silicon version number 0000 - Revision 1.0	RO	0x0

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GLOSSARY

ACRONYMS, ABBREVIATIONS, AND DEFINITIONS

ACRONYM	DEFINITION
DDR	Dual-Data Rate (memory)
ES	Engineering Sample
ESD	Electrostatic Discharge
FET	Field Effect Transistor
EPC	Embedded Power Controller
FSM	Finite State Machine
GND	Ground
GPIO	General-Purpose I/O
HBM	Human Body Model
HD	Hot-Die
HS-I^2C	High-Speed I^2C
I^2C	Inter-Integrated Circuit

ACRONYM	DEFINITION
IC	Integrated Circuit
ID	Identification
IDDQ	Quiescent supply current
IEEE	Institute of Electrical and Electronics Engineers
IR	Instruction Register
I/O	Input/Output
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LBC7	Lin Bi-CMOS 7 (360 nm)
LDO	Low Drop Output voltage linear regulator
LP	Low-Power application mode
LSB	Least Significant Bit
MMC	Multimedia Card
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NVM	Nonvolatile Memory
OD	Open Drain
OMAP™	Open Multimedia Application Platform™
RTC	Real-Time Clock
SMPS	Switched Mode Power Supply
SPI	Serial Peripheral Interface
POR	Power-On Reset

Table 97. REVISION HISTORY

VERSION	DATE	NOTES
*	03/2010	See (1).

(1) Initial release

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp
PTPS659110A2ZRC	PREVIEW	BGA	ZRC	98	250	Green (RoHS & no Sb/Br)	Call TI	Call TI
PTPS659110A2ZRCR	PREVIEW	BGA	ZRC	98	2000	Green (RoHS & no Sb/Br)	Call TI	Call TI
PTPS659112A2ZRC	PREVIEW	BGA	ZRC	98	250	Green (RoHS & no Sb/Br)	Call TI	Call TI
PTPS659112A2ZRCR	PREVIEW	BGA	ZRC	98	2000	Green (RoHS & no Sb/Br)	Call TI	Call TI
PTPS659113A2ZRC	PREVIEW	BGA	ZRC	98	250	Green (RoHS & no Sb/Br)	Call TI	Call TI
PTPS659113A2ZRCR	PREVIEW	BGA	ZRC	98	2000	Green (RoHS & no Sb/Br)	Call TI	Call TI

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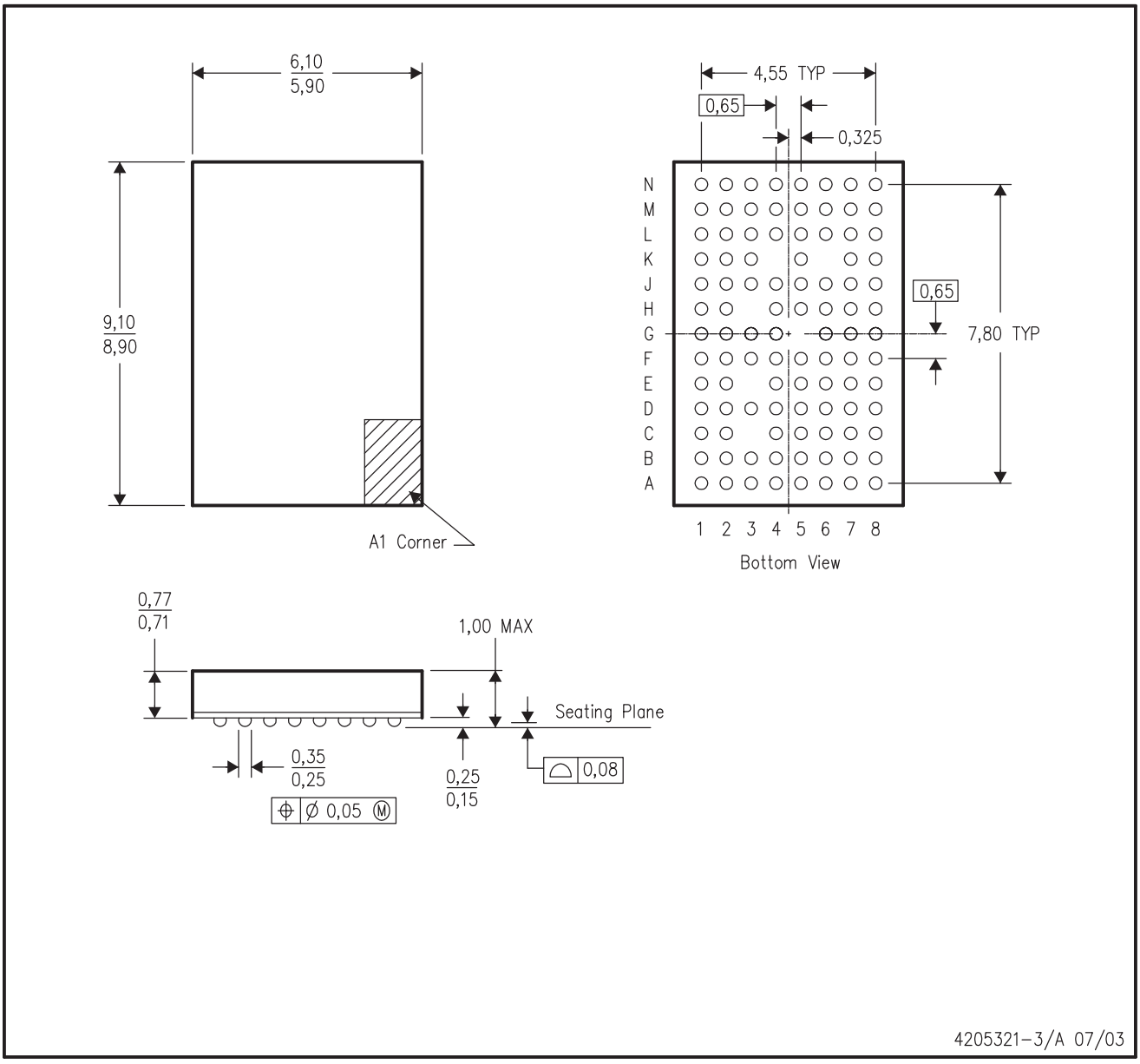
PACKAGE MECHANICAL DATA

ZRC (S–PBGA–N98) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

SWCS049-018

Figure 22. PACKAGE MECHANICAL DATA

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Table 98. REVISION HISTORY

Version	Literature Number	Date	Notes
*	SWCS049	June 2010	See (1)
A	SWCS049A	February 2011	See (2)
B	SWCS049B	February 2011	See (3).

(1) *TPS65911 Data Manual*, SWCS049 - Initial release.
(2) *TPS65911 Data Manual*, SWCS049A - Version A:
  (a) Update Figure 1: LDO1, LDO2, LDO3, LDO6, and LDO7.
  (b) Remove table, *SUPPORTED PROCESSORS AND CORRESPONDING PART NUMBERS*
  (c) Update RECOMMENDED OPERATING CONDITIONS: Adjust pin names and add exception.
  (d) Update EXTERNAL COMPONENT RECOMMENDATION: VDDCtrl SMPS, update FET part number.
  (e) Update: DIGITAL I/O VOLTAGE ELECTRICAL CHARACTERISTICS: Add updated BOOT1 characteristics.
  (f) Update: LDO1 AND LDO2: Update LDO1 and LDO2 characteristics.
  (g) Update LDO5: Update LDO5.
  (h) Update LDO6, LDO7, AND LDO8: Update LDO6, LOD7, and LDO8.
  (i) Update Table 8: Update LDO1, LDO2, LDO3, LOD7, and LDO8
  (j) Update Table 9: Remove SEL [6:0] selection bits.
  (k) Update PWRON: Add more explanation and reorganize section.
  (l) Add explanation to: PWRON, GPIO0–8, HDRST Input, and PWRDN.
  (m) Update I^2C INTERFACE: Add ACCESS PROTOCOLS.
  (n) Update Table 13, Register Rest values.
  (o) Update Register Table: Table 50, Table 51, Table 60, and Table 62.
  (p) Update Table 7: BGA Pin column.
  (q) Upate PACKAGING INFORMATION.
(3) *TPS65911 Data Manual*, SWCS049B - Version B:
  (a) Update VCC6 in ABSOLUTE MAXIMUM RATINGS.

PRODUCT PREVIEW

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