Below are the changes done in EZSDK\_05\_02 code as per below link:  
  
<http://e2e.ti.com/support/dsp/davinci_digital_media_processors/f/717/t/149505.aspx>  
  
The things highlighted under red colour are the final changes present in the files.  
  
**1. $(ezsdk\_install\_dir)/component-sources/c6accel\_2\_01\_00\_09/soc/packages/ti/c6accel\_unitservers/TI816X/serverplatforms.xs**  
  
Commented below highlighted lines. Also updated addresses as per EZSDK new memory map.  
  
var TI816X\_DSP\_MemoryMap = [  
//            ["DDR3\_HOST", {  
//                comment: "DDR3 Memory reserved for use by the A8",  
//                name: "DDR3\_HOST",  
//                base: 0x80000000,  
//                len:  0x16C00000    /\* 364 MB (Linux Kernel occupies 166MB so the 10MB can also be used for CMEM)\*/  
//            }],  
//            ["DDR3\_CMEM", {  
//                comment: "DDR3 Memory reserved for use by the C674/ARM for CMEM",  
//                name: "DDR3\_CMEM",  
//                base: 0x96C00000,  
//                len: 0x01400000       /\* 20MB (CMEM region defined based on application requirement) \*/  
//            }],  
            ["DDR3\_DSP", {  
                comment: "DDR3 Memory reserved for use by the C674",  
                name: "DDR3\_DSP",  
                base: 0x99500000,  
                len:  0x00C00000    /\* 12 MB (Default memory reserved for c674x changed based on size of the DSP code)\*/  
            }],  
            ["DDRALGHEAP", {  
                comment: "DDR3 Memory reserved for use by algorithms on the C674",  
                name: "DDRALGHEAP",  
                base: 0x98000000,  
                len:  0x01400000    /\* 20 MB (Region used by algs and codec engine for memory allocations)\*/  
            }],  
            ["DDR3\_SR1", {  
                comment: "DDR3 Memory reserved for use by SharedRegion 1",  
                name: "DDR3\_SR1",  
                base: 0x99400000,  
                len:  0x00100000    /\* 1 MB (Reserved)\*/  
            }],  
//            ["DDR3\_HDVPSS", {  
//                comment: "DDR3 Memory reserved for use by HDVPSS",  
//                name: "DDR3\_HDVPSS",  
//                base: 0xBF900000,  
//                len:  0x00200000    /\* 2 MB (Reserved)\*/  
//            }],  
//            ["DDR3\_V4L2", {  
//                comment: "DDR3 Memory reserved for use by V4L2",  
//                name: "DDR3\_V4L2",  
//                base: 0xBFB00000,  
//                len:  0x00200000    /\* 2 MB (Reserved)\*/  
//            }],  
            ["DDR3\_SR0", {  
                comment: "DDR3 Memory reserved for use by SharedRegion 0",                                                                        
                name: "DDR3\_SR0",  
                base: 0x9F700000,  
                len:  0x00200000    /\* 2 MB (Reserved)\*/  
            }],  
            ["DDR3\_REST", {  
                comment: "DDR3 Memory reserved for use by the M3 core",  
                name: "DDR3\_REST",  
                base: 0x9F900000,  
                len:  0x01000000    /\* 16 MB \*/  
            }],  
  
];  
/\*  
 \*  @(#) ti.sdo.ce.examples.servers.all\_codecs; 1, 0, 0,207; 10-11-2010 15:13:47; /db/atree/library/trees/ce/ce-s01x/src/ xlibrary  
  
 \*/  
  
**2. $(ezsdk\_install\_dir)/component-sources/c6accel\_2\_01\_00\_09/soc/packages/ti/c6accel\_unitservers/TI816X/ti816x.cfg**  
Commented below highlighted lines.  
  
    var entry2 = new SharedRegion.Entry();  
  
    entry2.base = ipcSharedMem.base;  
    entry2.len = ipcSharedMem.len;  
    entry2.ownerProcId = MultiProc.getIdMeta("HOST");  
    entry2.isValid = true;  
    entry2.createHeap = true;  
    entry2.cacheEnable = true;  
    entry2.name = "IpcShared";  
  
//    SharedRegion.setEntryMeta(  
//            common.SharedRegion\_map["Ipc"],  /\* index \*/  
//            entry2  
//    );  
  
  
**3. $(ezsdk\_install\_dir)/component-sources/c6accel\_2\_01\_00\_09/soc/app/c6accel\_opencv\_testapp/TI816X/c6accel\_opencv\_testapp.cfg**  
Changed highlighted values.  
  
Proc.sharedRegionId = 0;  
Proc.heapId = 3;  
  
  
**4. $(ezsdk\_install\_dir)/component-sources/c6accel\_2\_01\_00\_09/soc/app/c6accel\_opencv\_testapp/TI816X/loadmodules\_ti8168\_c6accel.sh**  
Commented below lines and also updated address.  
  
#rmmod cmemk.ko  
#rmmod syslink.ko  
  
insmod cmemk.ko phys\_start=0x96C00000 phys\_end=0x98000000 pools=20x4096  
  
  
**Now changes under codec\_engine code**  
  
**1. $(ezsdk\_install\_dir)/component-sources/codec\_engine\_3\_21\_00\_19/examples/ti/sdo/ce/examples/apps/universal\_copy/remote.cfg**  
  
Changed highlighted values for heapId and sharedRegionID:  
  
Processor.heapId = 3;  
Processor.sharedRegionId = 0;  
  
// Set up logging  
xdc.loadCapsule('ti/sdo/ce/examples/buildutils/common\_log.cfg');  
/\*  
 \*  @(#) ti.sdo.ce.examples.apps.universal\_copy; 1, 0, 0,115; 8-17-2011 12:05:31; /db/atree/library/trees/ce/ce-s19x/src/ xlibrary  
  
 \*/  
  
  
**2. $(ezsdk\_install\_dir)/component-sources/codec\_engine\_3\_21\_00\_19/examples/ti/sdo/ce/examples/servers/all\_codecs/package.bld**  
  
Added following two Highlighted portions.  
  
  
Pkg.otherFiles = [  
    "main.c", "setid.c", "all\_mc.cfg", "all\_syslink.cfg", "heaps.cfg",  
    "link.cmd", "package.bld", "\_config.bld", "makefile",  
    "ti\_platforms\_evm3530.cfg", "ti\_platforms\_evm6472.cfg",  
    "ti\_platforms\_evmDM8148.cfg",  
    "ti\_platforms\_evmTI814X.cfg", "ti\_platforms\_evmTI816X.cfg",  
    "serverplatforms.xs", "package/info"  
    ];  
  
var TI816X\_DSP\_ExtMemMap = {  
            DDR3\_DSP: {  
                comment: "DDR3 Memory reserved for use by the C674",  
                name: "DDR3\_DSP",  
                base: 0x99500000,  
                len:  0x00C00000    /\* 12 MB \*/  
            },  
            DDRALGHEAP: {  
                comment: "DDR3 Memory reserved for use by algorithms on the C674",  
                name: "DDRALGHEAP",  
                base: 0x98000000,  
                len:  0x01400000    /\* 20 MB \*/  
            },  
            DDR3\_SR1: {  
                comment: "DDR3 Memory reserved for use by SharedRegion 1",  
                name: "DDR3\_SR1",  
                base: 0x99400000,  
                len:  0x00100000    /\* 1 MB \*/  
            },  
            DDR3\_SR0: {  
                comment: "DDR3 Memory reserved for use by SharedRegion 0",  
                name: "DDR3\_SR0",  
                base: 0x9F700000,  
                len:  0x00200000    /\* 2 MB \*/  
            },  
};  
  
  
  
// set'theProf' to 'debug' for faster builds (with lower performance)  
var theProf = 'debug';//'whole\_program\_debug';  
  
.....  
  
  
for (var i = 0; i < Build.targets.length; i++) {  
  
    if ((programs != undefined) && (!programs.match(/DSP\_SERVER/))) {  
        break;  
    }  
  
    var targ = Build.targets[i];  
  
    /\* only build for BIOS-based targets \*/  
    if (targ.os == undefined) {  
  
        /\* No A8 Server yet \*/  
        if (targ.isa == "v7A") {  
            continue;  
        }  
  
//        print("building for target " + targ + " ...");  
  
        /\* Platforms were added to targ.platforms[] in config.bld \*/  
        for (var j = 0; j < targ.platforms.length; j++) {  
            var platform = targ.platforms[j];  
  
//            print("  platform:  " + platform);  
  
            var platInst = Build.usePlatform(platform);  
            var platMod = platInst.$module;  
  
            if (platform.match(/simTesla/) || platform.match(/sdp4430/)) {  
//                print("   skipping unsupported platform");  
                continue;  
            }  
  
            if (platform.match(/evm6472|evm6474|6608|6616|6670|6678/)) {  
                          addExe(targ, platform, "all\_mc");  
            }  
            else {  
                /\* heterogeneous multicore, syslink-based Server \*/  
  
                /\* platform instances used by this package \*/  
                Build.platformTable["ti.platforms.evmTI816X:DSP"] = {  
                l1DMode:"32k",  
                l1PMode:"32k",  
                l2Mode:"0k",  
                externalMemoryMap: [  
                [ "DDR3\_DSP",   TI816X\_DSP\_ExtMemMap.DDR3\_DSP ],  
                [ "DDRALGHEAP", TI816X\_DSP\_ExtMemMap.DDRALGHEAP ],  
                [ "DDR3\_SR1",   TI816X\_DSP\_ExtMemMap.DDR3\_SR1 ],  
                [ "DDR3\_SR0",   TI816X\_DSP\_ExtMemMap.DDR3\_SR0 ]  
                ],  
                codeMemory: "DDR3\_DSP",  
                dataMemory: "DDR3\_DSP",  
                stackMemory: "DDR3\_DSP"  
                };  
  
                addExe(targ, platform, "all\_syslink");  
            }  
        }  
    }  
}     /\* homogeneous multicore, IPC-based Server \*/  
  
  
(3) $(ezsdk\_install\_dir)/component-sources/codec\_engine\_3\_21\_00\_19/examples/ti/sdo/ce/examples/servers/all\_codecs/ti\_platforms\_evmTI816X.cfg  
  
Commented below highlighted lines:  
  
  
var entry2 = new SharedRegion.Entry();  
  
entry2.base = ipcSharedMem.base;  
entry2.len = ipcSharedMem.len;  
entry2.ownerProcId = MultiProc.getIdMeta("HOST");  
entry2.isValid = true;  
entry2.createHeap = true;  
entry2.cacheEnable = true;  
entry2.name = "IpcShared";  
  
//SharedRegion.setEntryMeta(  
//    common.SharedRegion\_map["Ipc"],  /\* index \*/  
//    entry2  
//);  
  
/\*  
 \*  @(#) ti.sdo.ce.examples.servers.all\_codecs; 1, 0, 0,251; 8-17-2011 12:06:37; /db/atree/library/trees/ce/ce-s19x/src/ xlibrary  
  
 \*/  
  
(4) $(ezsdk\_install\_dir)/component-sources/codec\_engine\_3\_21\_00\_19/examples/ti/sdo/ce/examples/servers/all\_codecs/serverplatforms.xs  
  
Updated addresses as highlighted below to sync up with new memory map as per EZSDK\_05\_02 version and above  
  
       var TI816X\_DSP\_ExtMemMap = {  
            DDR3\_HOST: {  
                comment: "DDR3 Memory reserved for use by the A8",  
                name: "DDR3\_HOST",  
                base: 0x80000000,  
                len:  0x16C00000    /\* 364 MB \*/  
            },  
            DDR3\_DSP: {  
                comment: "DDR3 Memory reserved for use by the C674",  
                name: "DDR3\_DSP",  
                base: 0x99500000,  
                len:  0x00C00000    /\* 12 MB \*/  
            },  
            DDRALGHEAP: {  
                comment: "DDR3 Memory reserved for use by algorithms on the C674",  
                name: "DDRALGHEAP",  
                base: 0x98000000,  
                len:  0x01400000    /\* 20 MB \*/  
            },  
            DDR3\_SR1: {  
                comment: "DDR3 Memory reserved for use by SharedRegion 1",  
                name: "DDR3\_SR1",  
                base: 0x99400000,  
                len:  0x00100000    /\* 1 MB \*/  
            },  
            DDR3\_HDVPSS: {  
                comment: "DDR3 Memory reserved for use by HDVPSS",  
                name: "DDR3\_HDVPSS",  
                base: 0xBF900000,  
                len:  0x00200000    /\* 2 MB \*/  
            },  
            DDR3\_V4L2: {  
                comment: "DDR3 Memory reserved for use by V4L2",  
                name: "DDR3\_V4L2",  
                base: 0xBFB00000,  
                len:  0x00200000    /\* 2 MB \*/  
            },  
            DDR3\_SR0: {  
                comment: "DDR3 Memory reserved for use by SharedRegion 0",  
                name: "DDR3\_SR0",  
                base: 0x9F700000,  
                len:  0x00200000    /\* 2 MB \*/  
            },  
            DDR3\_M3: {  
                comment: "DDR3 Memory reserved for use by the M3 core",  
                name: "DDR3\_M3",  
                base: 0x8F000000,  
                len:  0x01000000    /\* 16 MB \*/  
            },  
};  
  
  
**5.  $(ezsdk\_install\_dir)/component-sources/codec\_engine\_3\_21\_00\_19/examples/ti/sdo/ce/examples/buildutils/remote.cfg**  
  
Changed below Highlighted portion:   
  
  
    /\* first set module defaults ... \*/  
  
    Processor.heapId = 3;  
    Processor.sharedRegionId = 0;  
  
    /\* ... then add per-processor settings \*/  
    var coreComm = {};  
    coreComm.numMsgs = 64;  
    coreComm.msgSize = 4 \* 1024;  
    coreComm.heapId = 3;  
    coreComm.userCreatedHeap = false;  
    coreComm.sharedRegionId = 0;  
  
    if (platform.match("TI814X") || platform.match("TI816X") ||  
            platform.match("DM8148") || platform.match("DM8168")) {  
        Processor.coreComm.$add(coreComm);  
        Processor.coreComm.$add(coreComm);  
//        Processor.coreComm.$add(coreComm);  
//        Processor.coreComm.$add(coreComm);  
    }  
    else {  
        Processor.coreComm.$add(coreComm);  
        Processor.coreComm.$add(coreComm);  
    }