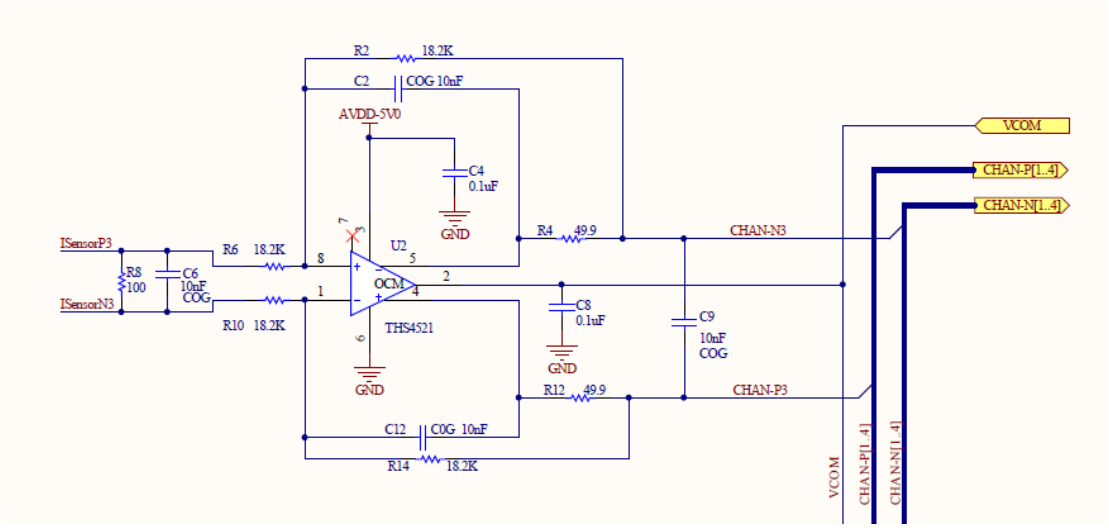

Figure 1. Differential amplifier before ADS1278. There are 8 such amplifiers. VCOM comes from the ADC 2.5V reference output. CHAN-P and CHAN-N go to the analog input of the ADC.

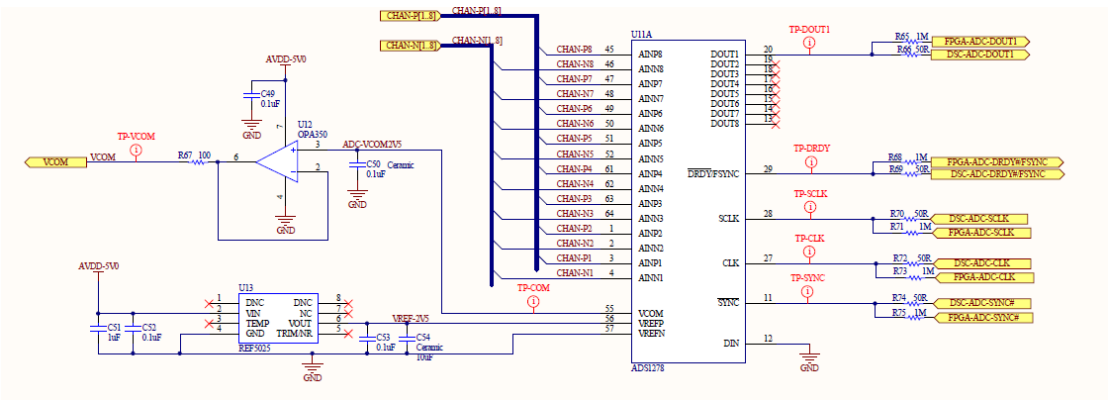

Figure2. ADS1278 input and output. By 0 ohm resistor selection, the default setting for reading the ADC is by DSC TMS32028335 through its McBSP port. Since we choose CLK to be 150MHZ/4/4, SCLK is slow enough so that the extra latch between the ADC and TMS320F28335 as suggested by ADS1278 datasheet is ignored.

==========》 continue on to next page

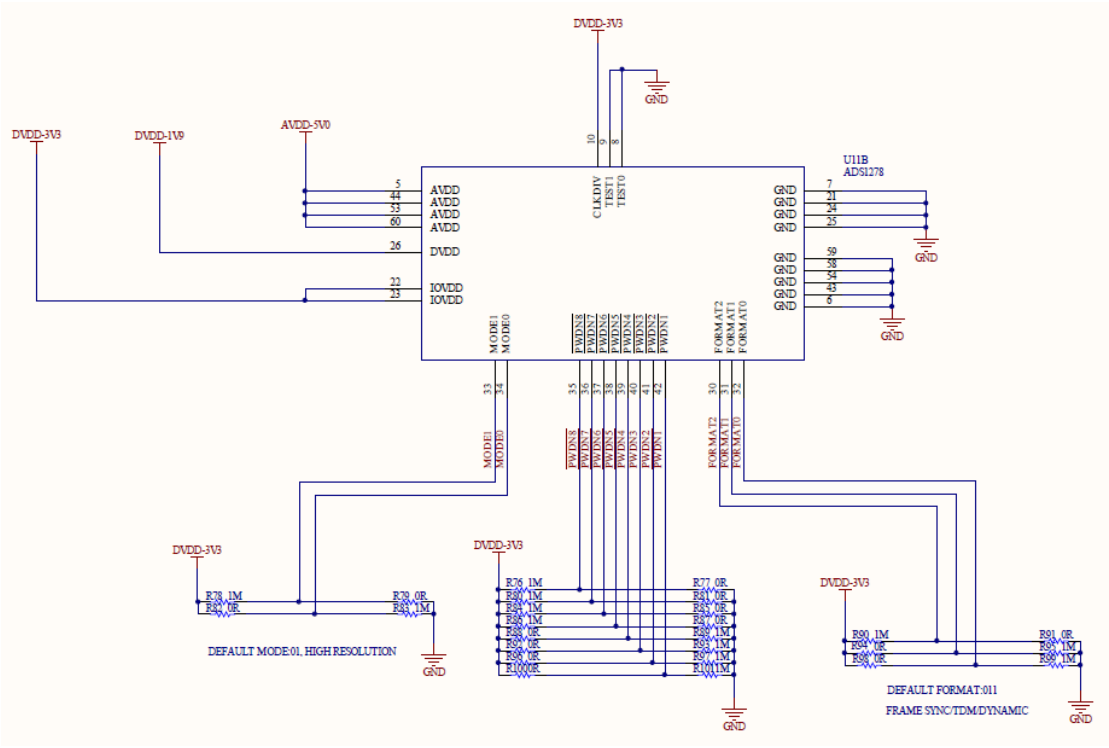

Figure3. ADS1278 mode and Format selection.

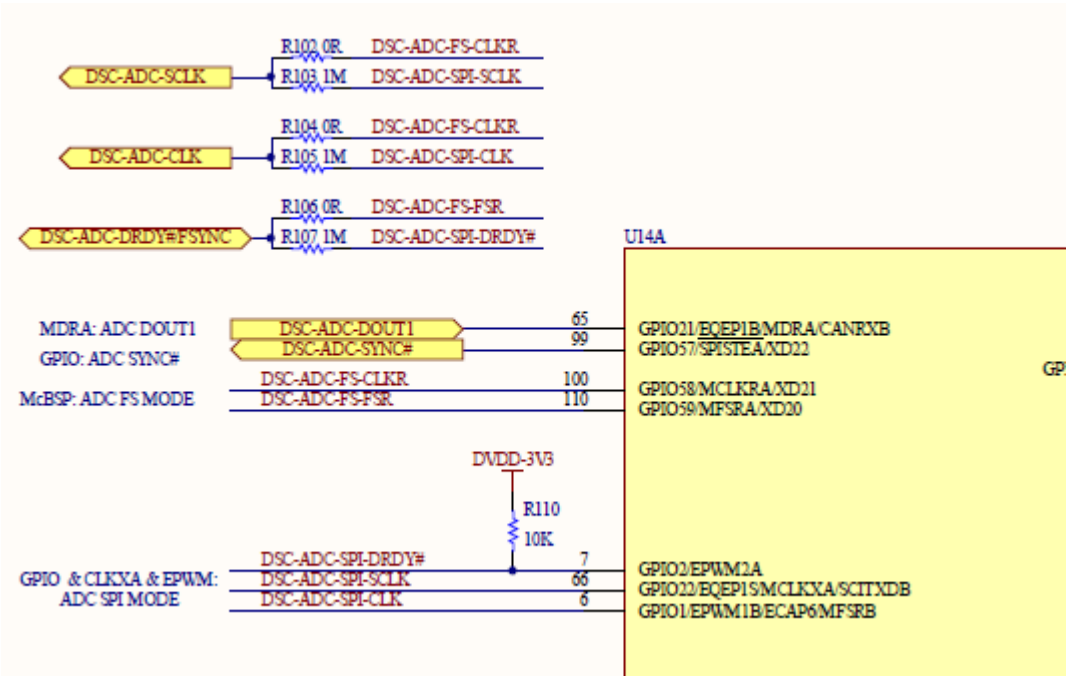

Figure4. TMS320F28335 McBSP connection. By default, Frame Sync mode is used, and CLKR and CLK are connected together, just as the ADS1278 datasheet suggests.

McBSP init function:

```
void mcbsp_init_dlb()
{
```

```
//**************** RESET MCBSP
    McbspaRegs.SPCR2.bit.FRST=0; // Frame Sync generator reset
    McbspaRegs.SPCR2.bit.GRST=0; // Sample Rate generator Reset
    McbspaRegs.SPCR2.bit.XRST=0; // Transmitter reset
    McbspaRegs.SPCR1.bit.RRST=0; // Receiver reset

//**************** Initialize McBSP Registers
// McBSP register settings for Digital loop back
    McbspaRegs.SPCR1.bit.DLB=0;           // DLB disbled
    McbspaRegs.SPCR1.bit.CLKSTP=0;      // Non-SPI, normal frame sync
    McbspaRegs.SPCR1.bit.RINTM=0;       //RRDY directly drives RINT

    McbspaRegs.RCR2.bit.RPHASE=0;    // only 1 phase
    McbspaRegs.RCR2.bit.RDATDLY=0;    // RDATDLY = 0
    McbspaRegs.RCR1.bit.RFRLEN1=ADC_CHANNELS-1; //current setting ADC_Channels=4
    McbspaRegs.RCR1.bit.RWDLEN1=4;       //4 for 24bits per Rx channel
                                         // no need to set XCR as we don't use transmitter

    McbspaRegs.SRGR2.bit.CLKSM = 1;
                                    // CLKSM=1 (If SCLKME=0, i/p clock to SRG is LSPCLK)
                  // no need to set FSGM as it is only for FSX. FSR only needs FSRM and DLB
    McbspaRegs.SRGR2.bit.FPER = 511;           \
// FPER = 512 CLKG periods (ADC high resolution mode), sample rate = 9MHZ/512 = 18KHZ

    McbspaRegs.SRGR1.bit.FWID = 1;           // Frame Width = 2 CLKG period
    McbspaRegs.SRGR1.bit.CLKGDV = 3;

    McbspaRegs.PCR.bit.FSRM = 1;           // FSR generated internally, output
    McbspaRegs.PCR.bit.CLKRM = 1; // CLKR generated internally, output
    McbspaRegs.PCR.bit.CLKRP = 1;
// falling CLKR pin makes ADC to output data as opposed to default rising edge.



    McbspaRegs.MFFINT.bit.RINT = 1; // Enable Receive Interrupts

//************** Enable Sample rate generator
    McbspaRegs.SPCR2.bit.GRST=1;

    delay_loop();                          // Wait at least 2 SRG clock cycles

//************* Enable RX unit, disable TX unit as we don't need to output data
    McbspaRegs.SPCR2.bit.XRST=0;
    McbspaRegs.SPCR1.bit.RRST=1;
```

```
//************* Frame Sync generator reset
    McbspaRegs.SPCR2.bit.FRST=1;
}
```

ADC SYNC signal is always set to be 1.

All inputs to the op amps are grounded.
RINT interrupt triggers a read. After over 1200 triggers, supposedly being in the stable state, the following reads are obtained, with one code per trigger,

00FF8D25 00000D8F 0000627D 00002445 00FF8D0C 00000DAD 0000629C 00002445
00FF8CFF 00000D8F 00006285 0000244E 00FF8CFE 00000D88 00006295 0000245F
00FF8CF5 00000DB2 0000628E 0000244D 00FF8CD9 00000D87 00006226 0000247C
00FF8CF3 00000DA4 00006278 00002447 00FF8D15 00000DAC 0000628D 0000243E
00FF8CFC 00000D9F 00006270 00002459 00FF8CE2 00000D88 00006289 0000245D
00FF8CFE 00000DAF 00006294 00002470 00FF8CD4 00000D9E 00006296 0000246E
00FF8CF5 00000D68 000062A7 0000246A 00FF8CEB 00000D88 000062A6 00002462
00FF8CFF 00000D9E 0000629D 00002459 00FF8CDA 00000D9A 0000629B 0000244B
00FF8D04 00000D6C 0000629F 00002471 00FF8CD6 00000D75 000062A7 00002473
00FF8CEE 00000D69 000062A2 00002452 00FF8D06 00000D9E 000062AD 00002455
00FF8CF3 00000D9F 000062BA 0000243A 00FF8D1D 00000D51 000062A3 0000241B
00FF8CF4 00000D7F 0000629F 00002421 00FF8D06 00000D88 0000628F 00002424
00FF8D1D 00000D81 000062A1