3 Signal Integrity

3.1 Clock Signal

The CLK terminal is implemented with an input/output buffer, which always is an input to the local VLYNQ logic. The CLK terminal also is capable of sourcing the VLYNQ clock when the clkdir bit in the VLYNQ Control register is set high.

Using the CLK terminal simultaneously as an input and output creates a signal-integrity issue at the CLK terminal. The source impedance of the output buffer and transmission-line impedance of the circuit-board etch creates a voltage divider at the CLK terminal during rising and falling edges of the VLYNQ clock. The voltage at the CLK terminal changes by $(VDD \times (Z_L/(Z_L + R_S)))$ when the output buffer toggles and remains at that voltage until it propagates to the load and the reflection returns. During this time, the amplitude of the CLK terminal is close to the switching threshold of the input buffer. Noise can cause the input buffer to generate glitches or invalid transitions of the VLYNQ clock. This causes problems for the local VLYNQ logic. Figure 2 is provided to help visualize the circuit topology that creates a voltage divider and resultant voltage waveform.

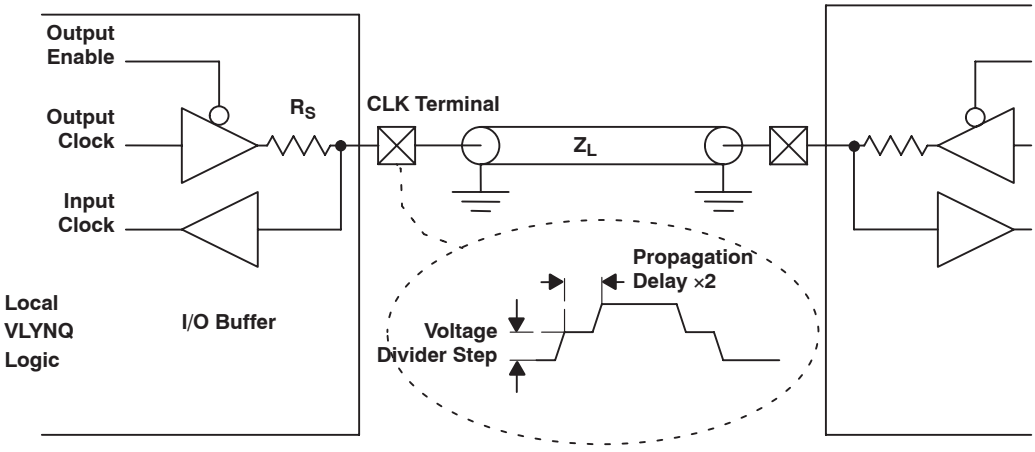

Figure 2. VLYNQ Clock Integrity

This problem can be resolved by placing a series-termination resistor between the CLK terminal and the transmission line. This increases the amplitude of the CLK terminal voltage divider step above the switching threshold so noise will not generate any glitches. This resistor always should be placed as close as possible to the CLK terminal that is sourcing the VLYNQ clock. The value recommended for this resistor is between 22 Ω and 50 Ω. As the resistor value increases, the amplitude of the voltage-divider step increases. However, the maximum VLYNQ clock speed decreases. The actual value may need to be determined after the circuit board is fabricated.

The circuit board should be designed using point-to-point connections without stubs and with enough bandwidth to support the maximum clock rate that can be sourced by the VLYNQ device sourcing the VLYNQ clock.