

# TMS320DM6446 594 MHz to 810 MHz Migration Guide

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## ABSTRACT

This application report is intended to provide an overview of changes necessary to upgrade a DM6446-based design from the 513 MHz or 594 MHz device to an 810 MHz device. The changes listed below are required by the 810 MHz device for proper operation; other system changes may be required to accommodate new speeds or capabilities in the system.

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## 1 Board Hardware Changes

**Table 1** summarizes the minimum changes required for the 810 MHz operation. These changes are required in all systems, unless the current design already meets or exceeds the new requirement.

**Table 1. Minimum Required Changes**

Component	Change To	Comments
CV <sub>DD</sub> Power Supply	Need 1.3 V instead of 1.2 V. Furthermore, the core power will nearly double (former 1.5W applications will now be in the 2.5W range), so the power supply design needs to account for the additional current	<p>810 MHz operation will have higher CV<sub>DD</sub> power demands than the 513 or 594 MHz parts. In systems where the power supply was barely adequate to supply 513 or 594 MHz parts, a larger power supply is required for 810 MHz operation.</p> <p>810 MHz maximum power consumption is estimated at 2.5W. Until the final power data can be obtained, designers should allow a large capacity (&gt;2 A) for the CV<sub>DD</sub> supply.</p> <p>Note that the VDAC requires a 1.2 V power supply; a level shifter might be required to convert the 1.3 V to 1.2 V if no additional power supply (1.2 V) is placed on the board when the CV<sub>DD</sub> power supply is changed to 1.3 V.</p>

[Table 2](#) summarizes other changes that may be required in some systems. These changes are not required in all systems; therefore, they should be evaluated to determine if they are necessary for any given design.

**Table 2. Other Potentially Required Changes**

Component	Change To	Comments
Heat Sink	Larger capacity heat sink	Systems where the heat sink was barely adequate to cool a 594 MHz device will require a larger heat sink for 810 MHz operation.  For more information, see <i>TMS320DM644x Thermal Considerations</i> ( <a href="#">SPRAAE4</a> ).

**NOTE:** Video processing back end (VPBE) pixel clock for HDTV output has always been sourced externally for DM644x devices; therefore, no additional hardware modification is needed.

## 2 Software/Firmware Changes

[Table 3](#) summarizes the minimum changes required for the 810 MHz operation. These changes are required in all systems, unless the current design already meets or exceeds the new requirement.

**Table 3. Minimum Required Changes**

Component	Change To	Comments
UBL	Correct PLL1 and PLL2 multipliers	TI will supply a new UBL with the correct programming for the 810 MHz DSP and 189 MHz DDR, as well as keeping the VPBE digital-analog converter (DAC) system clock set at 54 MHz.  Users of other frequencies need to change the phase-locked loop (PLL) multiply, divide, and DDR timing parameters as appropriate.

## 3 References

- *TMS320DM644x Thermal Considerations* ([SPRAAE4](#))

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