Class-D Audio Power Amplifiers: PCB Layout For Audio Quality, EMC & Thermal Success (Home Entertainment Devices)

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Contents

- Principles of Effective PCB Layout
- Successful EVM PCB Layout
- PCB Layout for Audio Quality and EMC
- PCB Layout for Thermal Effectiveness
- Appendix: PCB Trace & Via Impedances

Principles of Effective PCB Layout

- Effective PCB layouts follow a number of common principles.
- We will examine the principles used in a layout for a successful EVM.

- These principles can be used in other PCB layouts to make them effective.

Class-D and Class-AB Amplifiers

- We will focus on PCB layout for Class-D audio power amplifiers.
- However, except for EMC filtering, these principles also apply generally to Class-AB amplifiers.

- Apply these principles to layouts for Class-AB amplifiers as well.

Successful EVM PCB Layout

ICs With & Without PowerPAD

- We will focus on TPA3110D2, a medium power amplifier for home theater and large-screen TV.
- This IC includes a PowerPAD, a thermal pad for electrical and thermal conduction.
- HOWEVER, the principles we will discuss are NOT limited to ICs with PowerPADs – these principles will also produce success when they are applied to ICs that do NOT have PowerPADs.

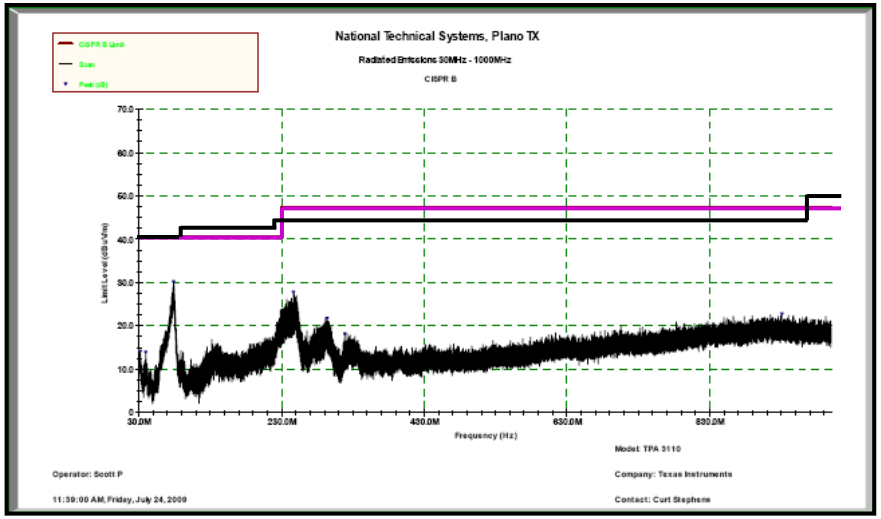
TPA3110D2: PowerPAD Layout

- Stereo 15W per channel EVM with PowerPAD for effective circuit grounding and PCB copper heatsinking.
  - Excellent audio quality (distortion, noise, crosstalk).
  - Excellent margin to requirements of FCC Class-B and CISPR22 Class-B.
    - Unshielded output cables 24” (~61cm) long
    - Power supply 12V
    - Loads 8Ω + 68µH
    - EMC filters using ferrite beads and capacitors (no inductors).
  - Excellent thermal performance, full rated output with PCB copper heatsink.

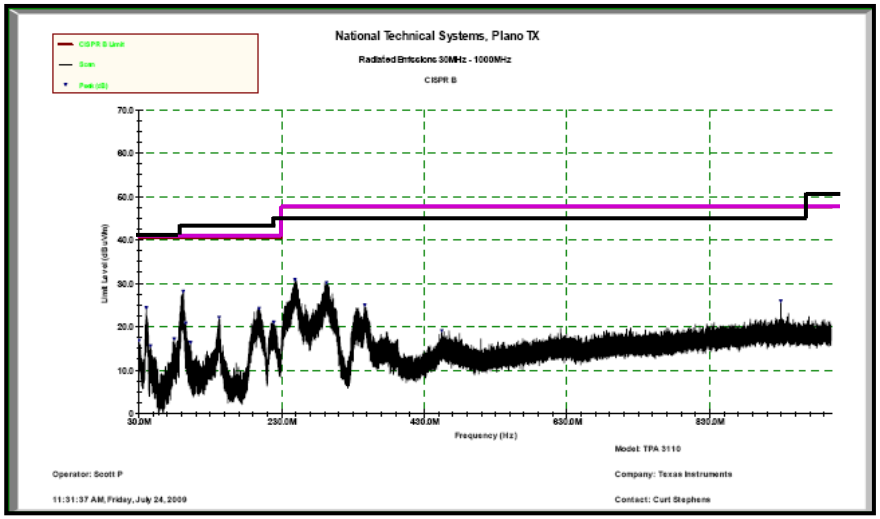
TPA3110D2: EMC Test Results

Final Test Margin was 10dB minimum.

Peak-reading graphs from an FCC Class-B test report are shown here with CISPR22 limits added.



Antenna Horizontal

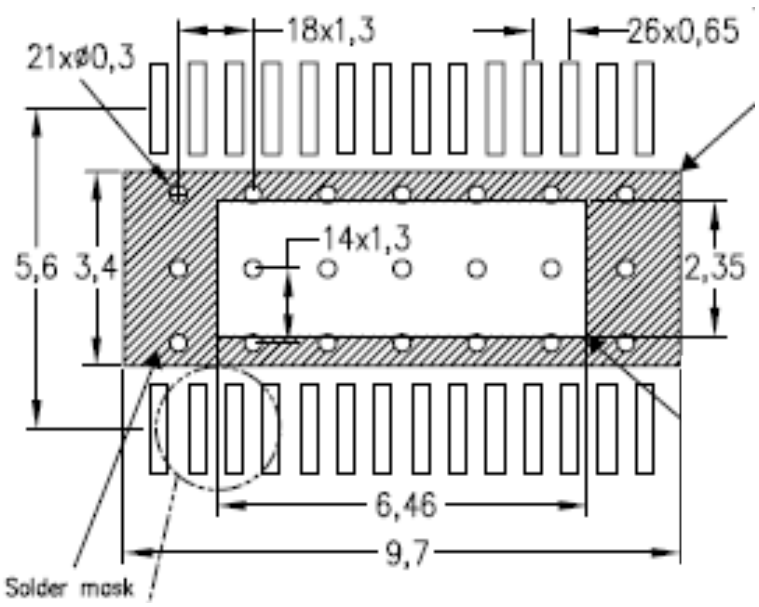


Antenna Vertical

FCC Class-B Limit
CISPR22 Class-B Limit

PowerPAD Solder Land Layout

- TPA3110D2 data sheet provides drawings of packages, PowerPAD land pattern (shown at right) and solder stencils.
- The PowerPAD is a VITAL electrical and thermal path.



- It must be included in the PCB layout and soldered to achieve rated performance.

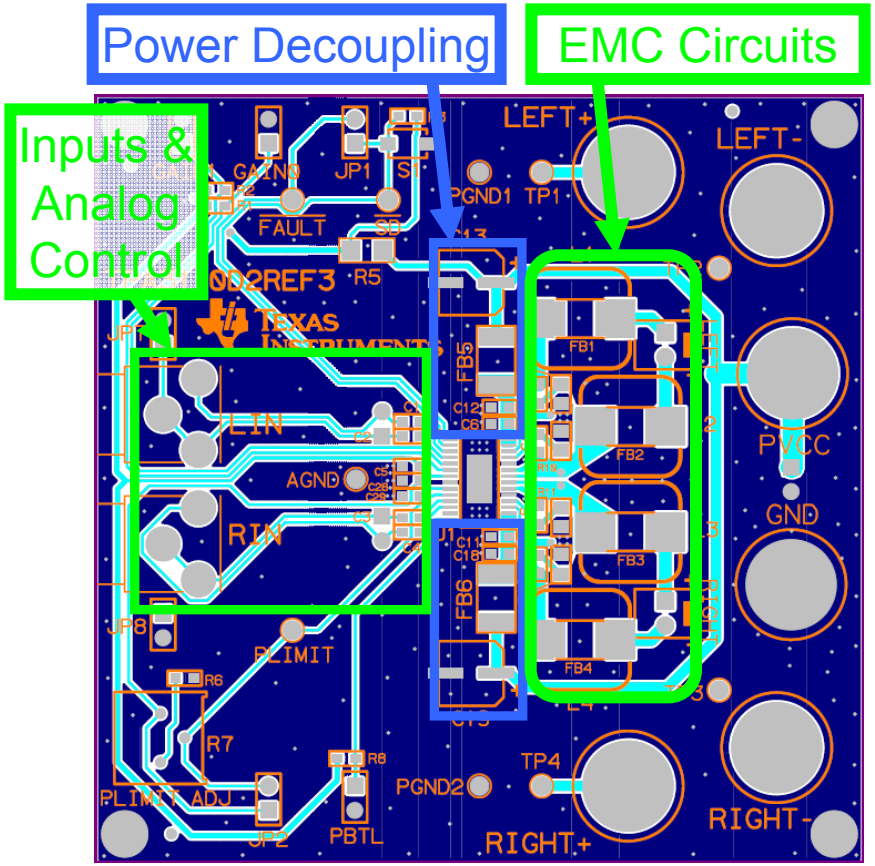
PCB Layout for Audio Quality and EMC

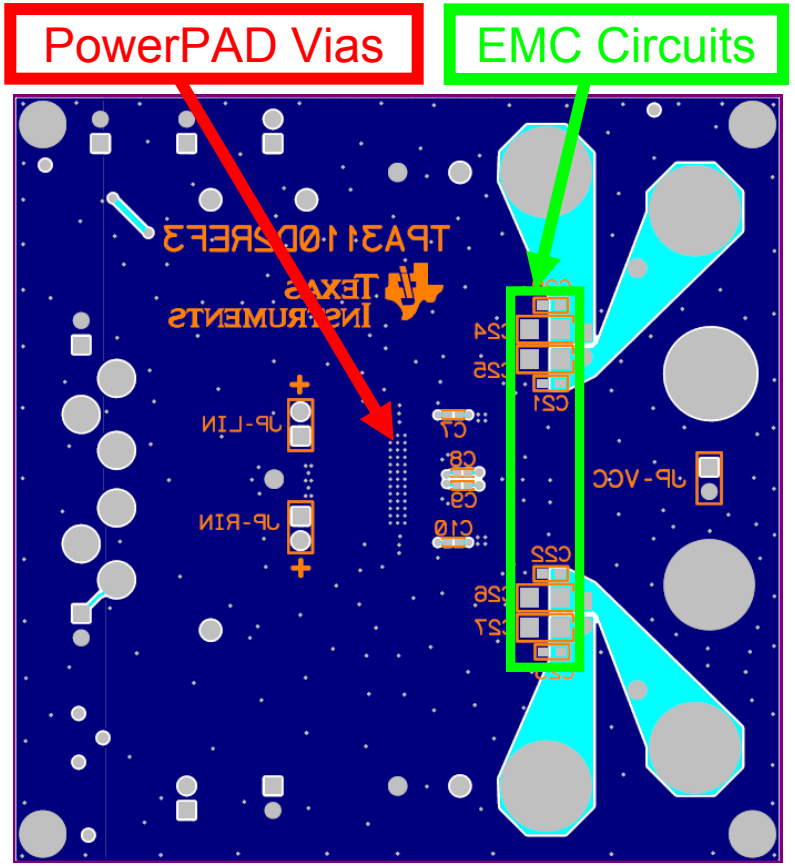
TPA3110D2: Critical Circuits

EVM PCB Layout Details

Top Layer

Bottom Layer (top view)



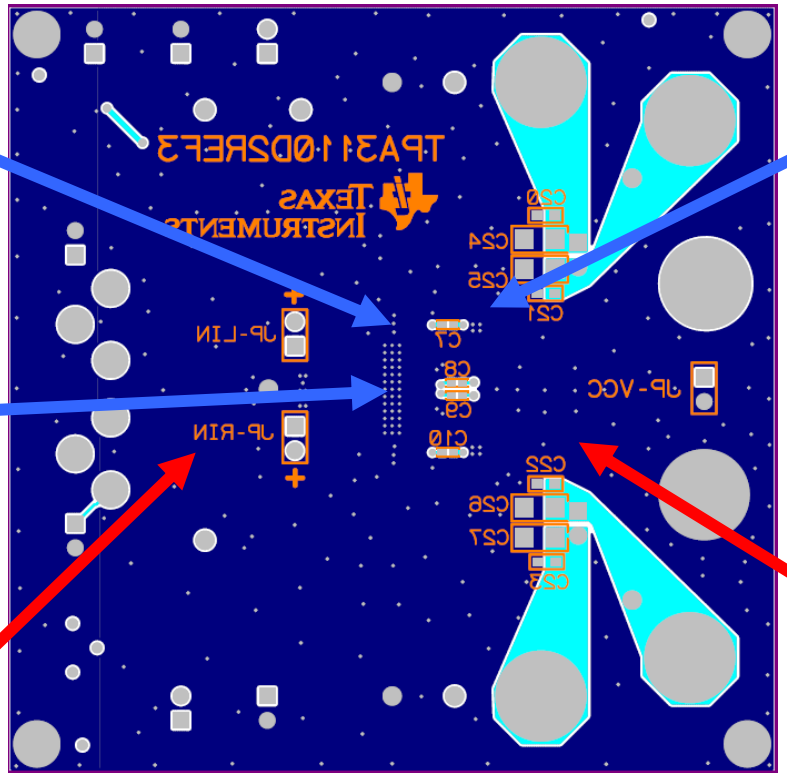


PCB Electrical: Order of Priority

- Ground Plane
- Decoupling Placement and Connection
- EMC Circuit Placement and Connection
- Input and Analog Control Routing
- System Integration
- Additional Notes

TPA3110D2: Ground Plane

- Use ground plane to connect all critical circuits.



Ground Plane Connects Decoupling Caps to IC

39 Thermal Vias Connect IC PowerPAD to Ground Plane

Inputs are Placed on “Quiet” Side of Ground Plane

Ground Plane Connects EMC Components to IC

Power and Outputs are on “Noisy” Side to Isolate Inputs from Their Currents

- This minimizes ground impedance, especially parasitic inductance.

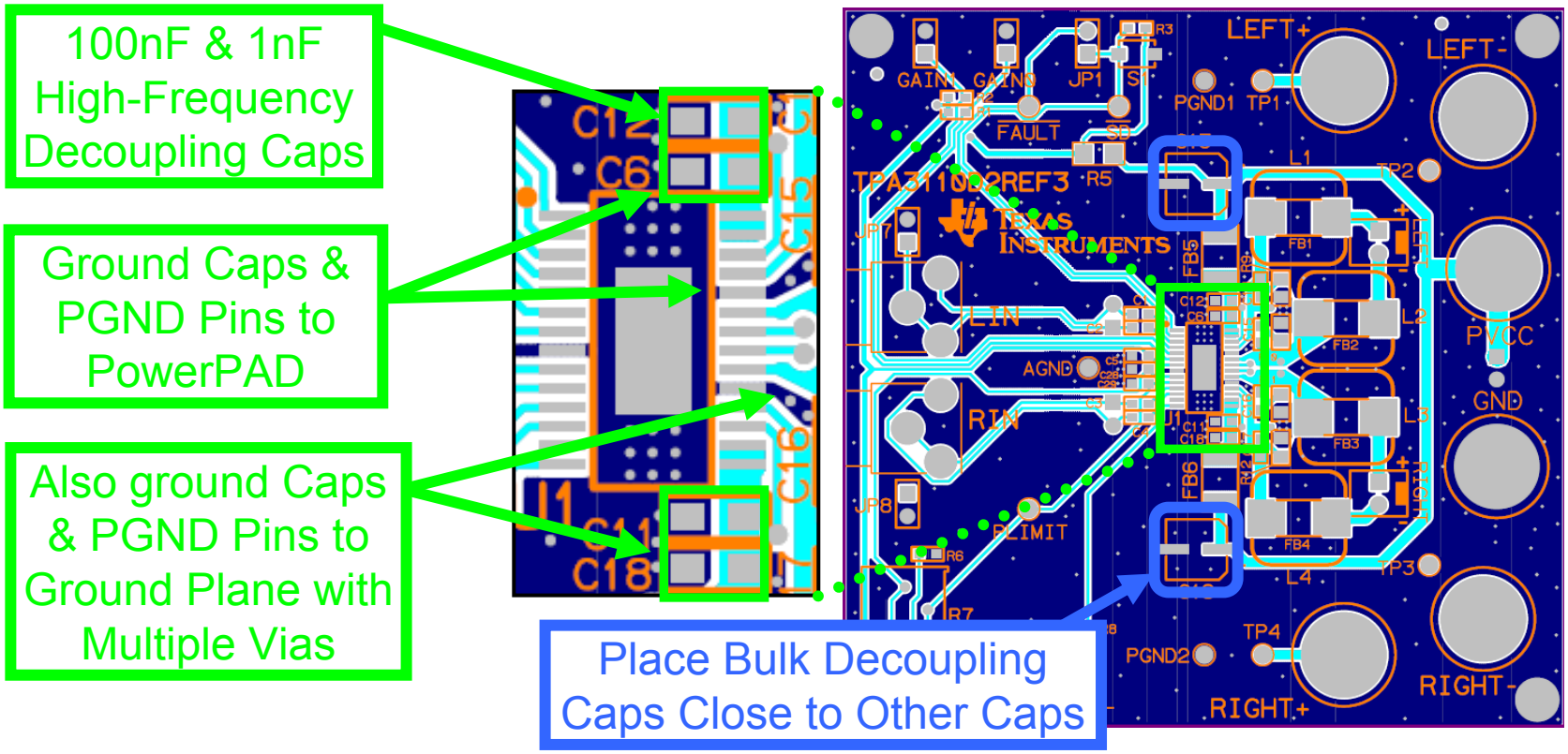
TPA3110D2: Ground Plane

- Place the IC at the center of the ground plane and ground the PowerPAD with thermal vias (0.33mm diameter on 1.0mm centers).
- Ground decoupling caps and EMC components to the PowerPAD area through ground plane.
- Place inputs on one side of the circuit and power and outputs on another to separate the currents.

- This approach minimizes interference that could reduce audio quality and makes decoupling and EMC filters and snubbers work best.

TPA3110D2: Decoupling Caps

- Place high-frequency caps within 1mm of the IC.



- This minimizes impedance and inductance in series with these capacitors.

TPA3110D2: Decoupling Caps

- Place high-frequency decoupling caps within 1mm of the IC, and place bulk decoupling caps as close as possible to them.
- Ground high-frequency decoupling caps and PGND pins to the PowerPAD.
- Also ground decoupling caps and PGND pins to the ground plane through multiple vias.

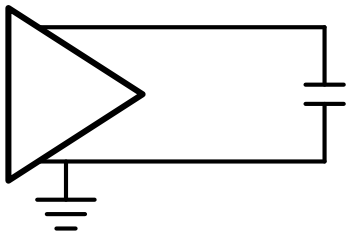
- This approach stabilizes power supply voltage and improves EMC by minimizing ringing.

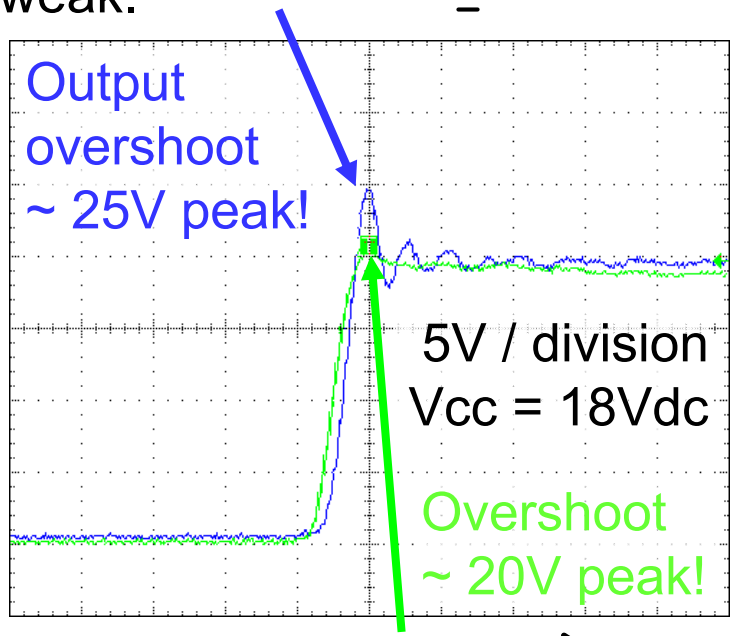
- **THIS IS VITAL FOR SUCCESS.**

Poor vs. Proper Decoupling

- Poor decoupling causes overshoot and ringing, which reduce EMC.
- Overshoot may activate short-circuit protection or even damage an IC in very bad cases.

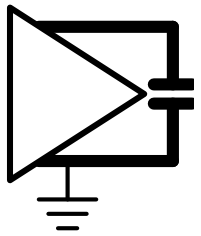
Decoupling cap 15mm from IC, cap connections weak.





- Proper decoupling minimizes overshoot and ringing and the problems they cause.

Cap only 1mm from IC, strong connections to power & ground plane.



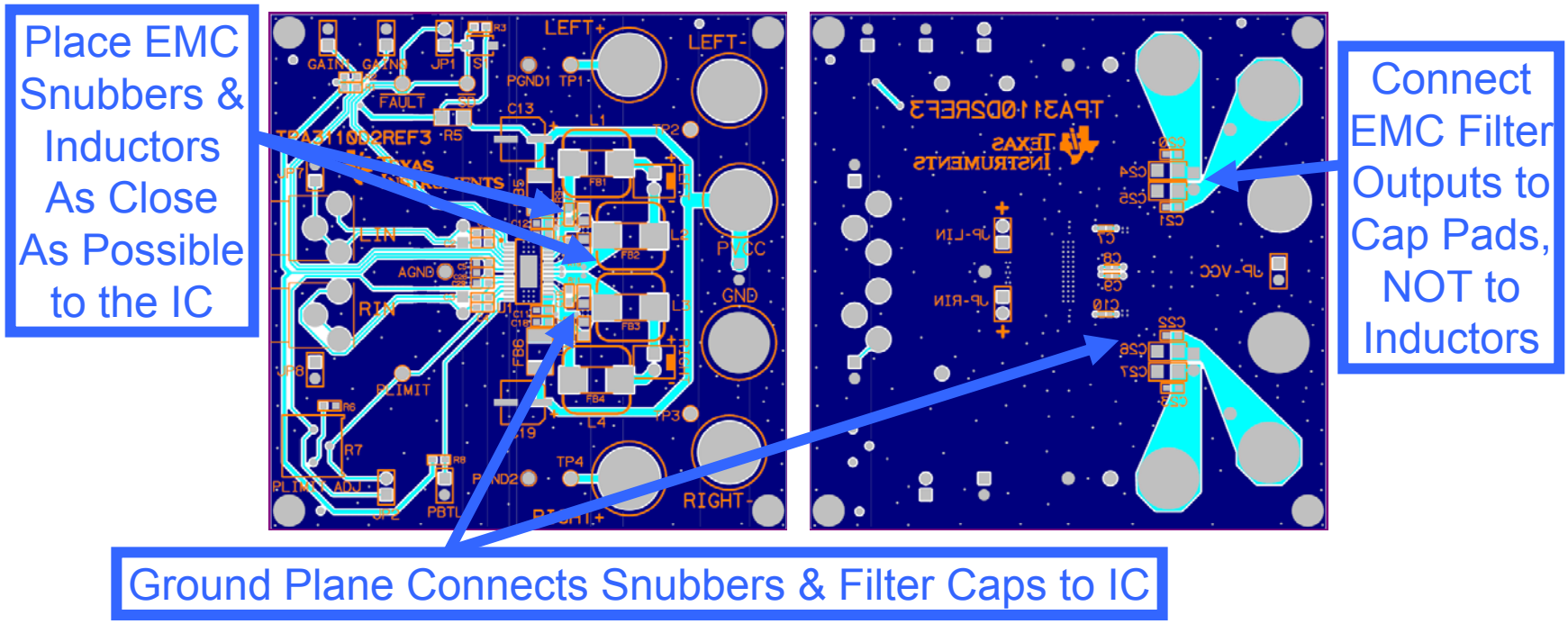
TPA3110D2 EMC Filtering

- The graphs of radiated emissions shown earlier were taken with ferrite bead EMC filters, not inductors, typical in TPA3110D2 applications.
- However, TPA3110D2 can be used with higher voltage and longer speaker leads, and then inductors would be required. For this reason, the TPA3110D2 EVM is laid out to accept either inductors or ferrite beads.

- For simplicity, we will refer to both inductors and ferrite beads as “inductors” in pages that follow.

TPA3110D2: EMC Snubbers & Filters

- Place EMC snubbers & filters very near the IC.



- Ground through ground plane & connect outputs to cap pads, directly or through broad copper, & not to inductors, to minimize stray inductance.

TPA3110D2: EMC Snubbers & Filters

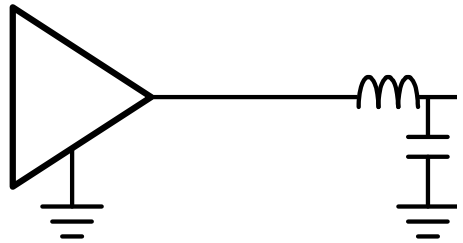
- Place EMC snubbers very near the IC.
- Place EMC filter caps as close to the IC as possible on the ground plane layer and ground them to the IC through the ground plane.
- Connect output terminals to pads of filter caps, directly or with broad copper, & not to inductors.

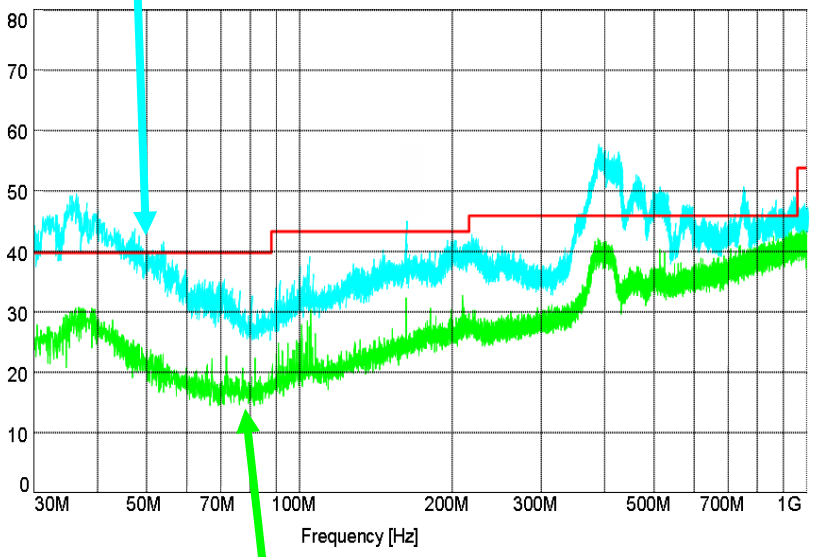
- This approach minimizes unfiltered loops and trace lengths as well as stray inductance.
- **This makes EMC components function best & gives the widest possible filter bandwidth.**

Poor vs. Proper Filter Placement

- Poor placement of EMC filters reduces filter attenuation & reduces EMC!

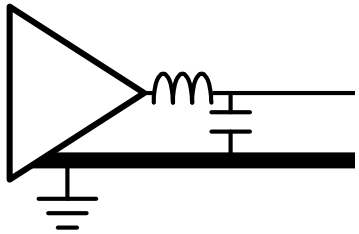
Filter far away from IC, ground connection poor.





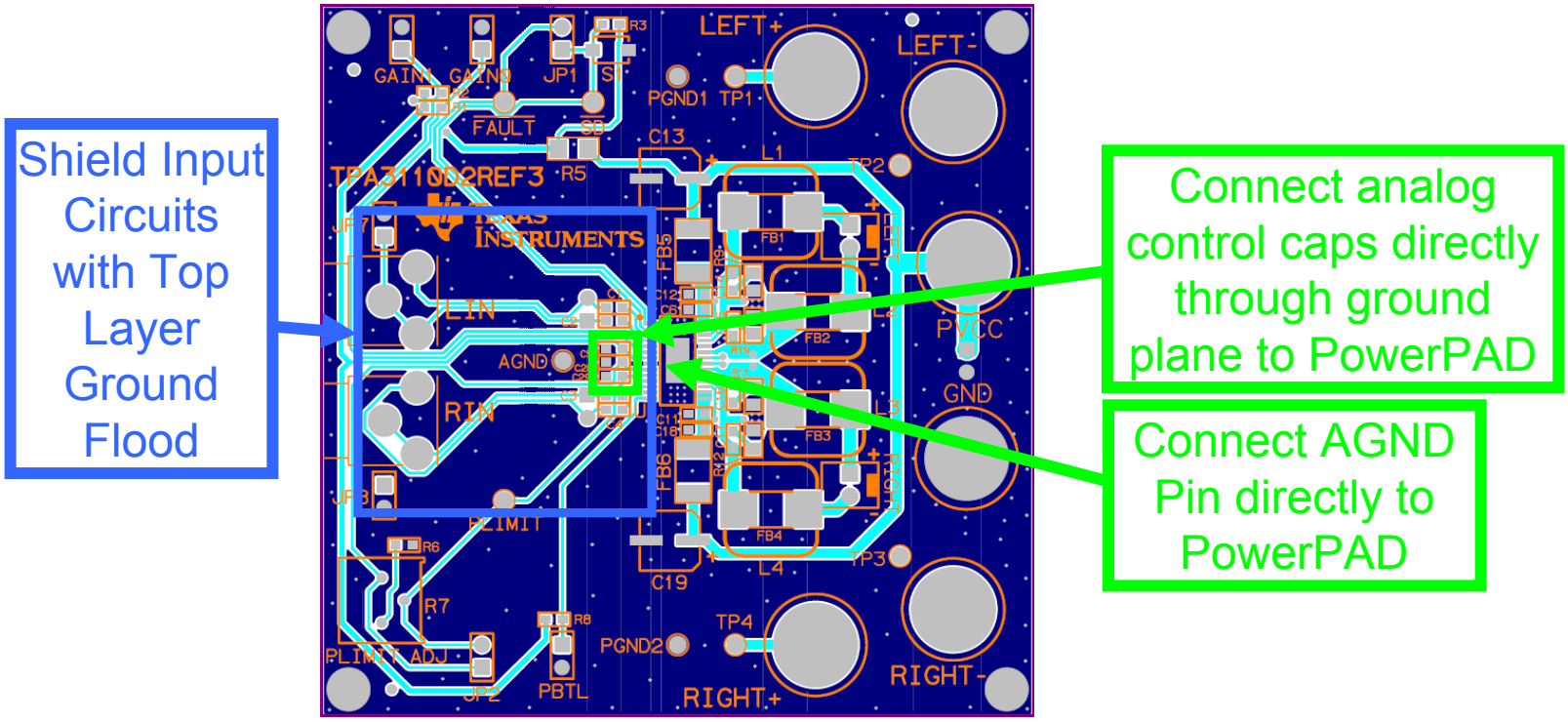
- Proper EMC filter placement gives good attenuation, improves EMC.

Filter very close to IC, strong ground plane connection.



TPA3110D2: Inputs, Analog Control

- Shield inputs with top layer ground flood.



- Ground analog control caps (GVDD, PLIMIT & AVCC) through ground plane with multiple vias.
- Ground AGND pin directly to PowerPAD.

TPA3110D2: Inputs, Analog Control

- Place inputs on the “quiet” side of the PCB and shield them with top and bottom ground floods.
- Ground analog control caps (GVDD, PLIMIT & AVCC) through ground plane with multiple vias.
- Ground the AGND pin to the PowerPAD, the center of the ground system.

- This prevents power voltages and currents from interfering in inputs and analog control circuits.
- (TPA3110D2 does not use an oscillator resistor or cap. In chips that do, they are very sensitive.)

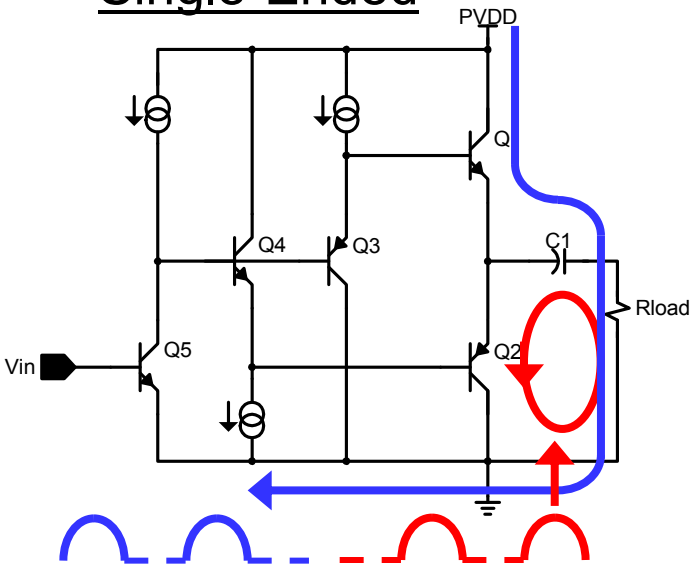
System Integration Issues

- We have talked mostly about APAs without considering their interaction with other circuits.
- Integrating an APA into a PCB layout requires understanding where load and power supply currents will flow.
- If this flow is controlled properly the layout will succeed, but if it is not there can be interference that creates problems.

System Integration: Load Currents

- All power amplifiers draw rectified images of load currents from power supplies and ground.

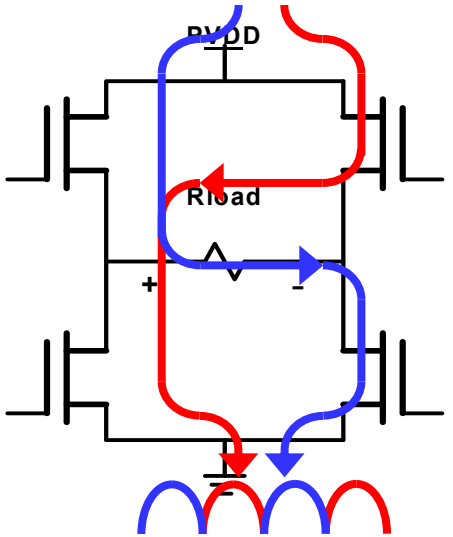
Single-Ended



Positive current flows to ground

Negative current circulates locally

Differential (BTL)

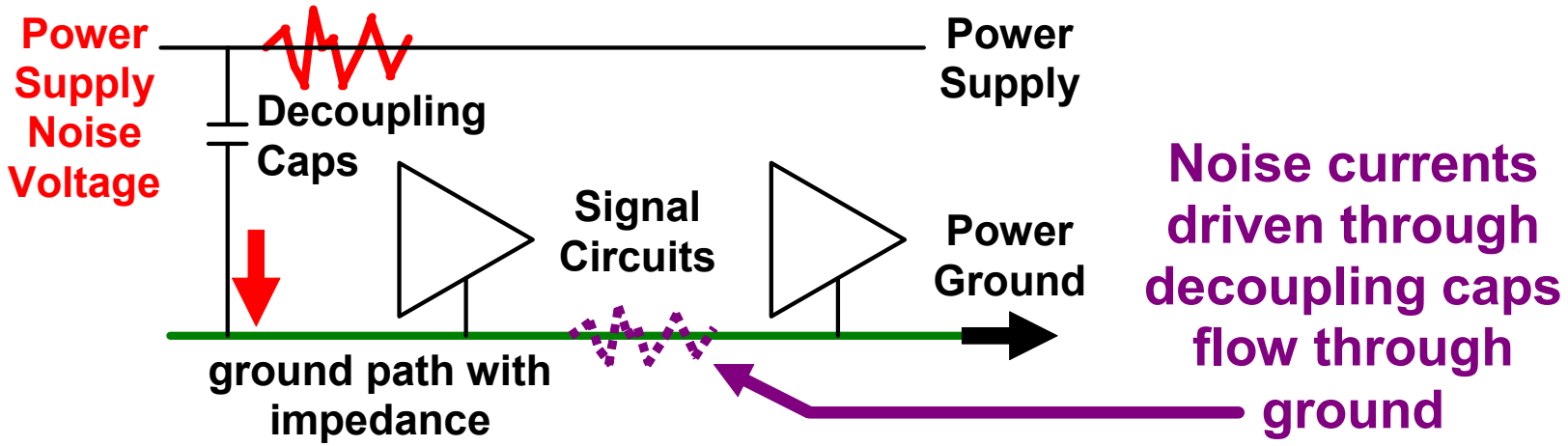


Negative AND positive currents flow to ground

- High frequencies flow partially in the decoupling, but audio currents must flow back to the supply.

System Integration: Supply Currents

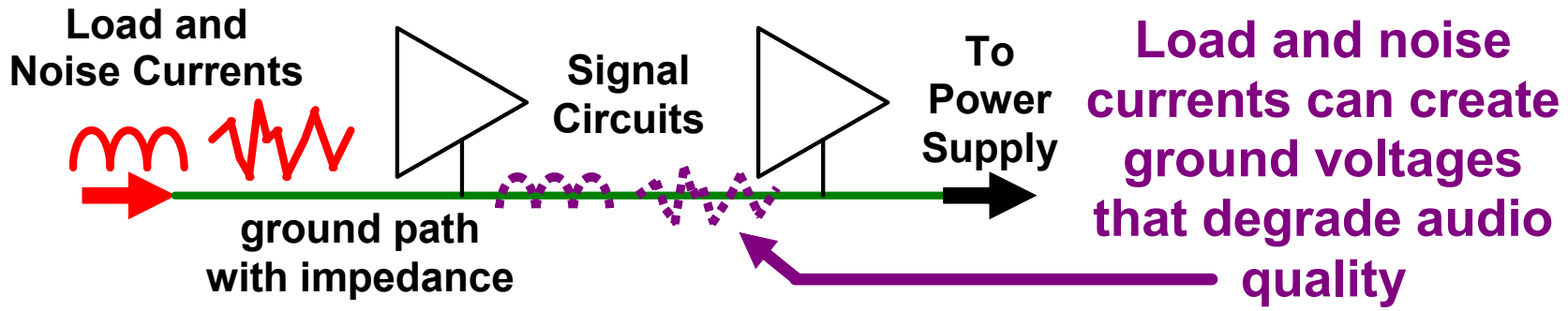
- Power supply noise voltages produce currents in ground paths through decoupling caps.



- Here currents at all frequencies must flow back to the power supply.

System Integration: Current Flow

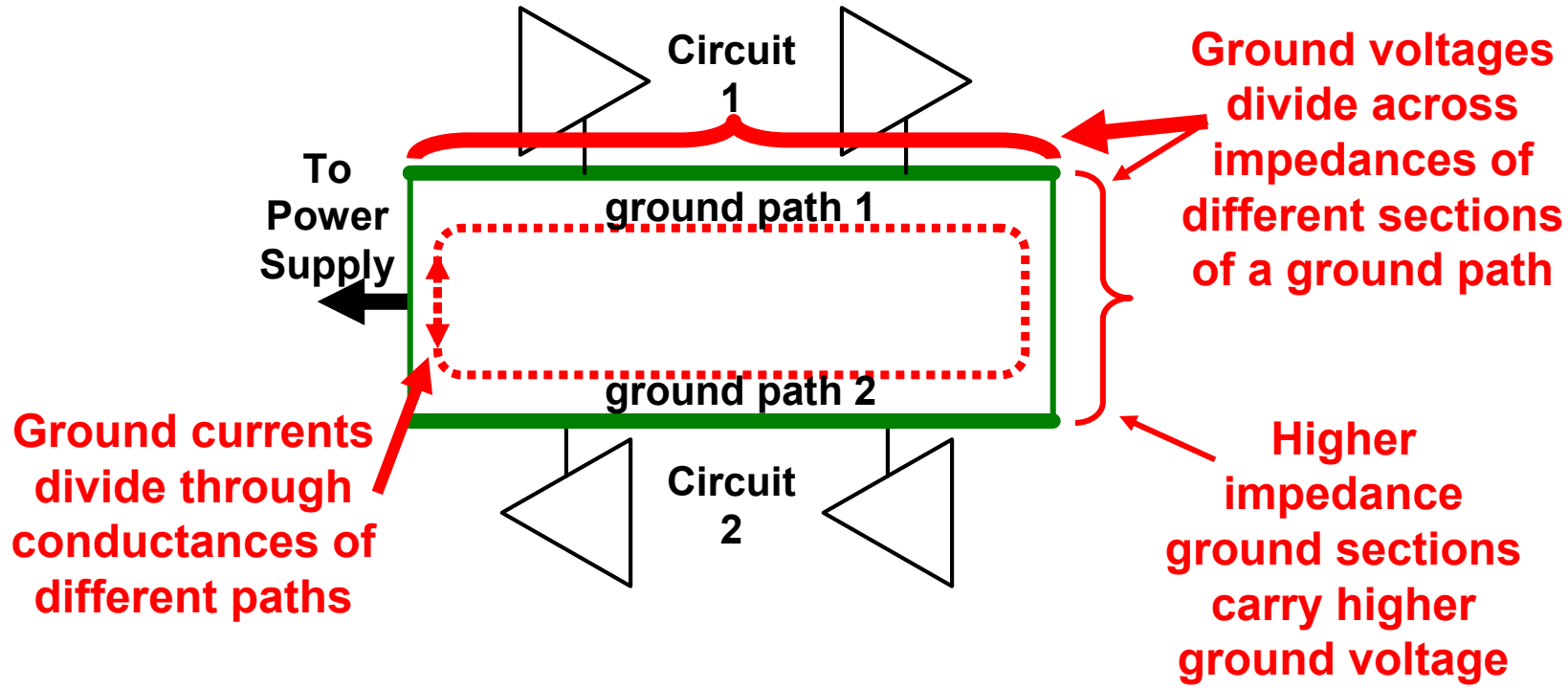
- These currents include noise and harmonics and can produce voltages in weak grounds that cause interference, crosstalk and distortion.



- Our best defense against this is our first priority, a ground plane, with low enough impedance to avoid voltages high enough to interfere.
- Still, high-frequency currents from switching circuits can produce unexpected interference.

Parallel Grounds (Ground Loops)

- It is easy to make ground loops with parallel paths carrying interfering currents, especially in system wiring among PCB assemblies.

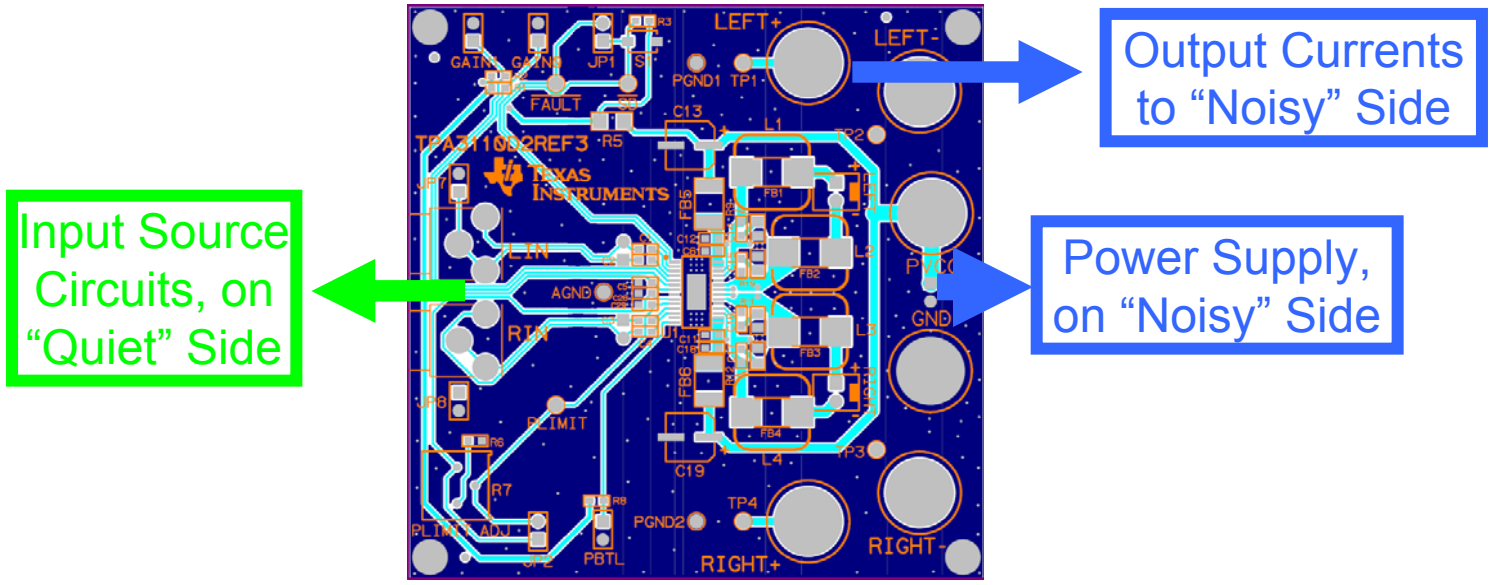


Ground Loops Cont'd.

- Interference in a single-ended input with high ground impedance to its source can be high.
- One way to avoid this is to separate ground currents so they cannot interfere.
- If this is not possible make the impedance of the ground path between a single-ended input and its source very low so ground currents produce only a small ground voltage across it.

System Integration

- Connect APA “noisy” side directly to the power supply and keep output leads on that side.
- Place input circuits on the other side, the “quiet” side, to keep APA ground currents out of them.



- This keeps APA power and output currents away from other circuits to prevent interference.

System Integration Cont'd.

- Place the APA at the power supply and connect its "noisy" side directly to the supply.
- Keep outputs on the APA "noisy" side away from other circuits.
- Place other circuits on the APA "quiet" side.

- This approach keeps APA power and output currents away from other circuits and prevents them from degrading signals in other circuits with interference, crosstalk and distortion.

System Integration Cont'd.

- With single-ended inputs, be careful to separate ground currents between circuits.
- If this is not possible make input ground impedance very low.

- This approach keeps ground currents from interfering in single-ended inputs.

System Integration Cont'd.

- Sometimes other constraints like mechanical height requirements make it impossible to follow these rules exactly.
- In cases like these make sure the switching currents in outputs and power supply lines are routed away from susceptible circuits.

- This will still help keep APA power and output currents away from other circuits and avoid interference, crosstalk and distortion.

System Integration Cont'd.

- Placing the APA at the power supply and connecting directly to the supply has another advantage.

- This minimizes losses in PCB copper traces and eliminates long, wide runs for power and ground, making PCB layout simpler.

PCB Layout Without a PowerPAD

- IC's without PowerPADs can still follow the same rules.
- For IC's without PowerPADs, use a ground plane and connect the power grounds of the IC directly to the ground plane with multiple vias.
- Otherwise treat the layout the same way as for TPA3110D2.

Additional Notes for PCB Layout

- Treat the ground area under the APA as the center point of the ground system for the IC.

  (This controls currents so they do not flow into unwanted areas and create interference.)

- Avoid PCB trace lengths that are closely related to wavelengths of primary power frequencies – these can cause interference with reflections.

  (A 4cm trace can pick up a high voltage at the GSM frequency 1.9GHz, wavelength ~16cm.)

Additional Notes for PCB Layout

- Try to avoid vias in traces for high currents and for decoupling and EMC filter caps. Double them where they must be used in these traces.

  (Via impedance carries some uncertainty.)

PCB Layout with Digital Inputs

- Circuits with digital inputs are still vulnerable to interference.
- Switching waveforms can cause glitches that interfere with data and clock lines. Interference with clocks is worst.

- Interference like this can cause clock jitter, which produces extra noise and distortion.

PCB Layout with Digital Inputs

- Apply the same rules for digital input circuits as for analog input circuits.
- Keep power and output traces on the “noisy” side of the PCB.
- Keep inputs on the “quiet” side of the PCB and shield them with top and bottom ground floods.

PCB Layout for Thermal Effectiveness

TPA3110D2: Thermal Features

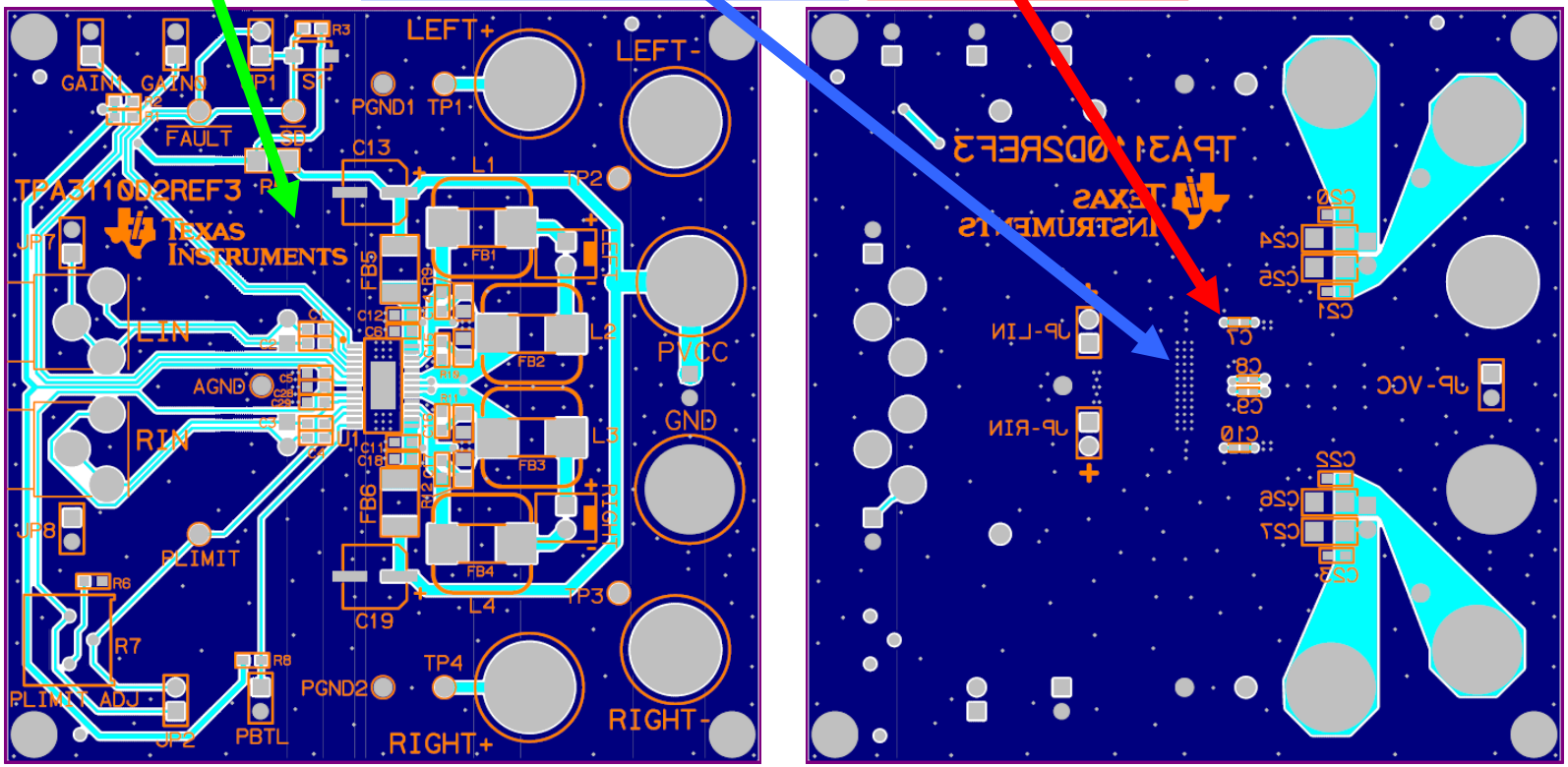
Top Layer

Bottom Layer (from top)

Vias Connect Top Flood to Ground Plane

PowerPAD Centered in Ground Plane & Connected with Vias

Ground Plane Cuts Radial, Not Circular



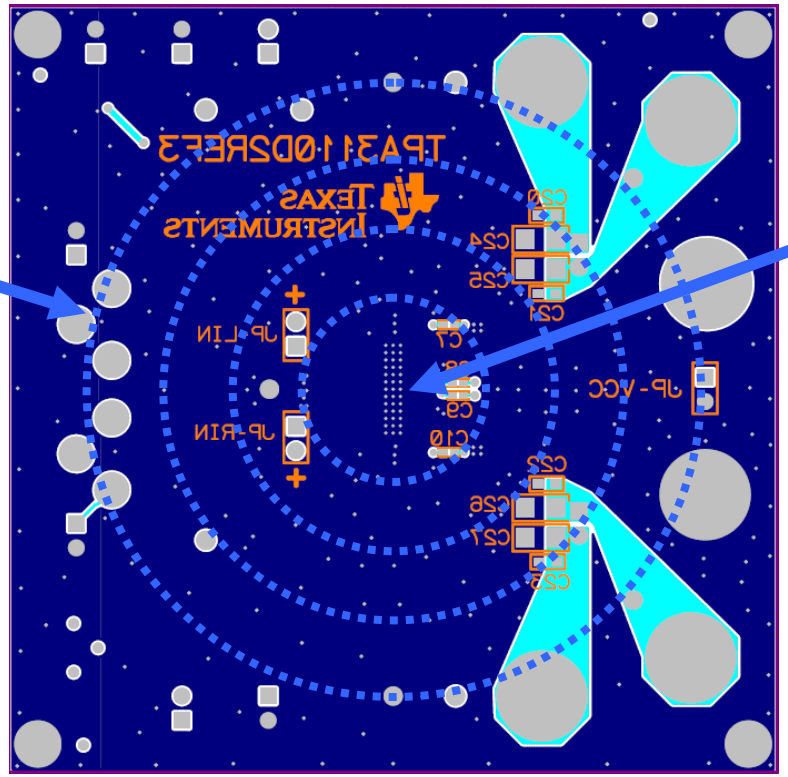
PCB Thermal: Order of Priority

- Copper Heatsink (Ground Plane)
- IC Placement on Copper Heatsink
- Ground Plane Cuts
- Top Ground Flood and Vias

Horizontal Copper Heatsink

- With a horizontal PCB, center the IC in the ground plane and ground the PowerPAD with thermal vias (0.33mm diameter, 1.0mm centers).

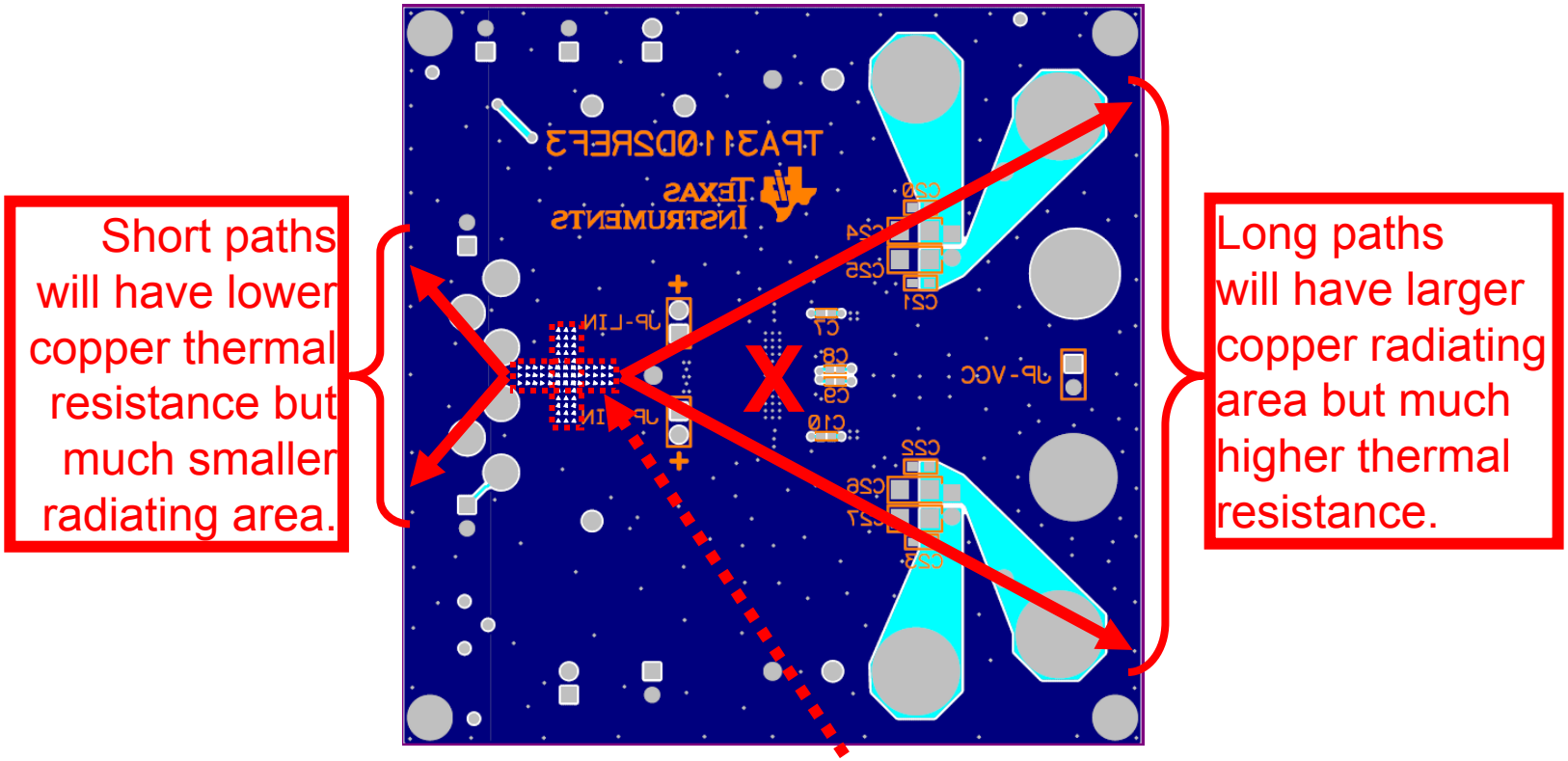
With the IC centered, all paths through PCB copper for heat have reasonably low thermal resistance and good thermal radiating area. This configuration is optimal.



The thermal vias create low thermal resistance from the PowerPAD to the ground plane for best heat transfer.

Horizontal Copper Heatsink Cont'd.

- If the IC is not placed at ground plane center, total thermal resistance from IC to air increases.

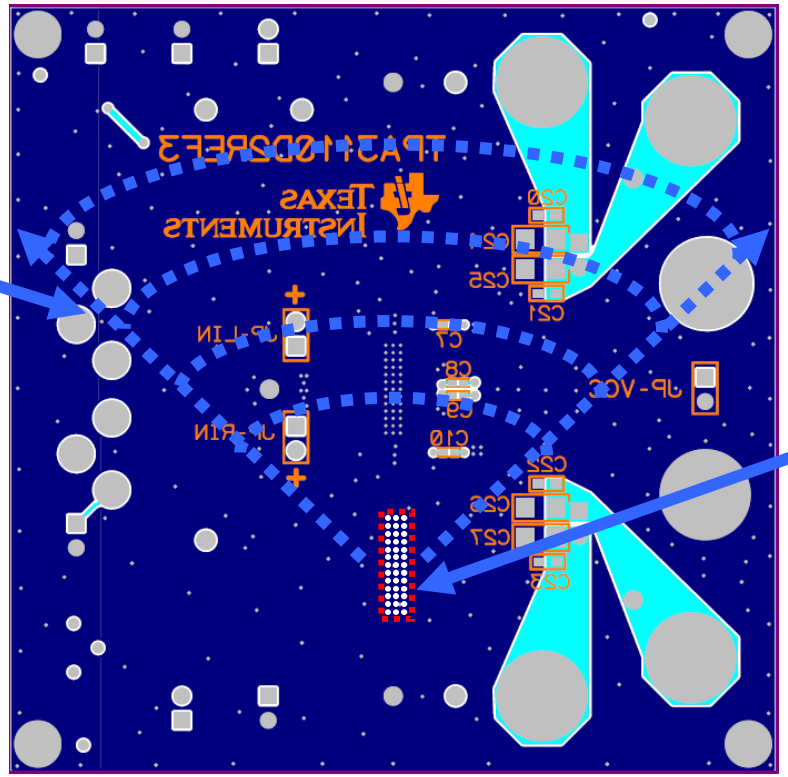


- PCB orientation matters; IC orientation does not.

Vertical Copper Heatsink

- A vertical PCB has greater airflow and is cooler.
- With a vertical PCB, place the IC near the bottom edge of the PCB for best heat flow.

With the PCB vertical, heat flows more strongly up the copper heatsink than down. This configuration is optimal.

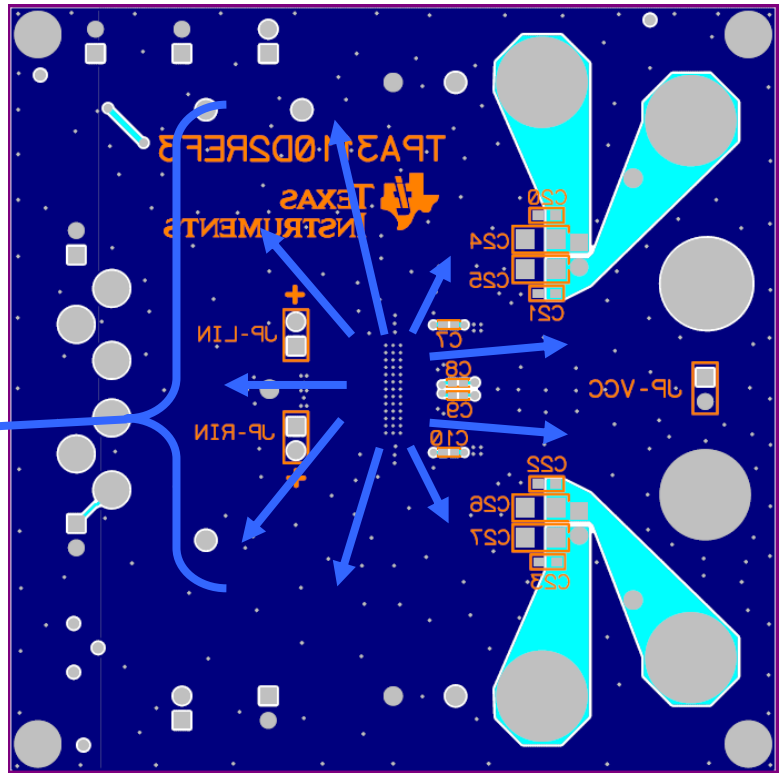


Vertical mounting can reduce IC junction temperature 5 to 10 C with the same copper area.

Radial Ground Plane Cuts

- Radial or nearly radial cuts allow heat to flow.

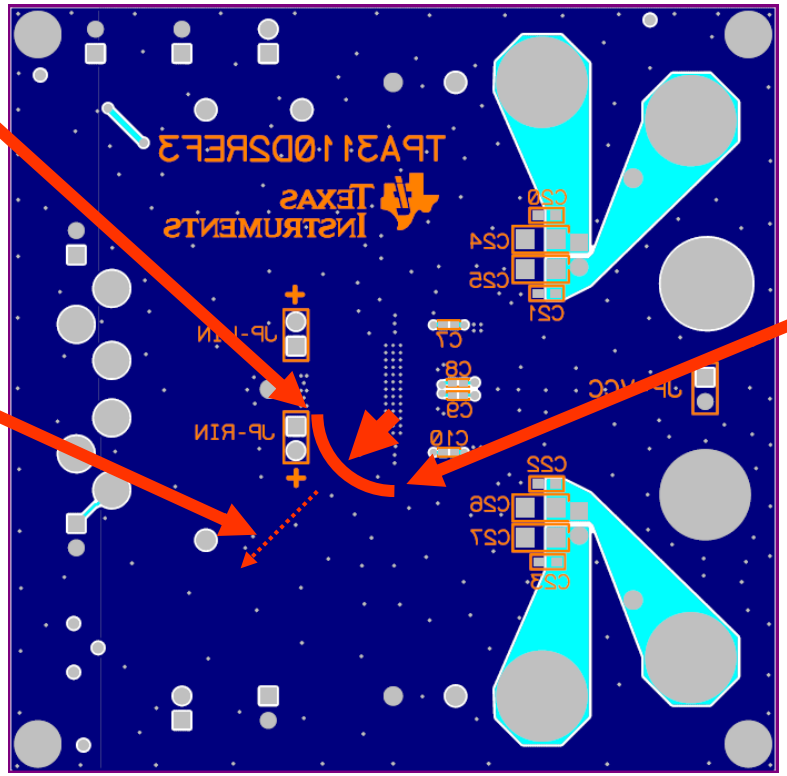
Radial or nearly radial cuts do not block paths for heat – they let heat flow between them, away from the IC.



Circular Ground Plane Cuts

- Circular cuts block paths for heat to flow.

A circular cut disconnects the copper inside the cut from the copper outside the cut.



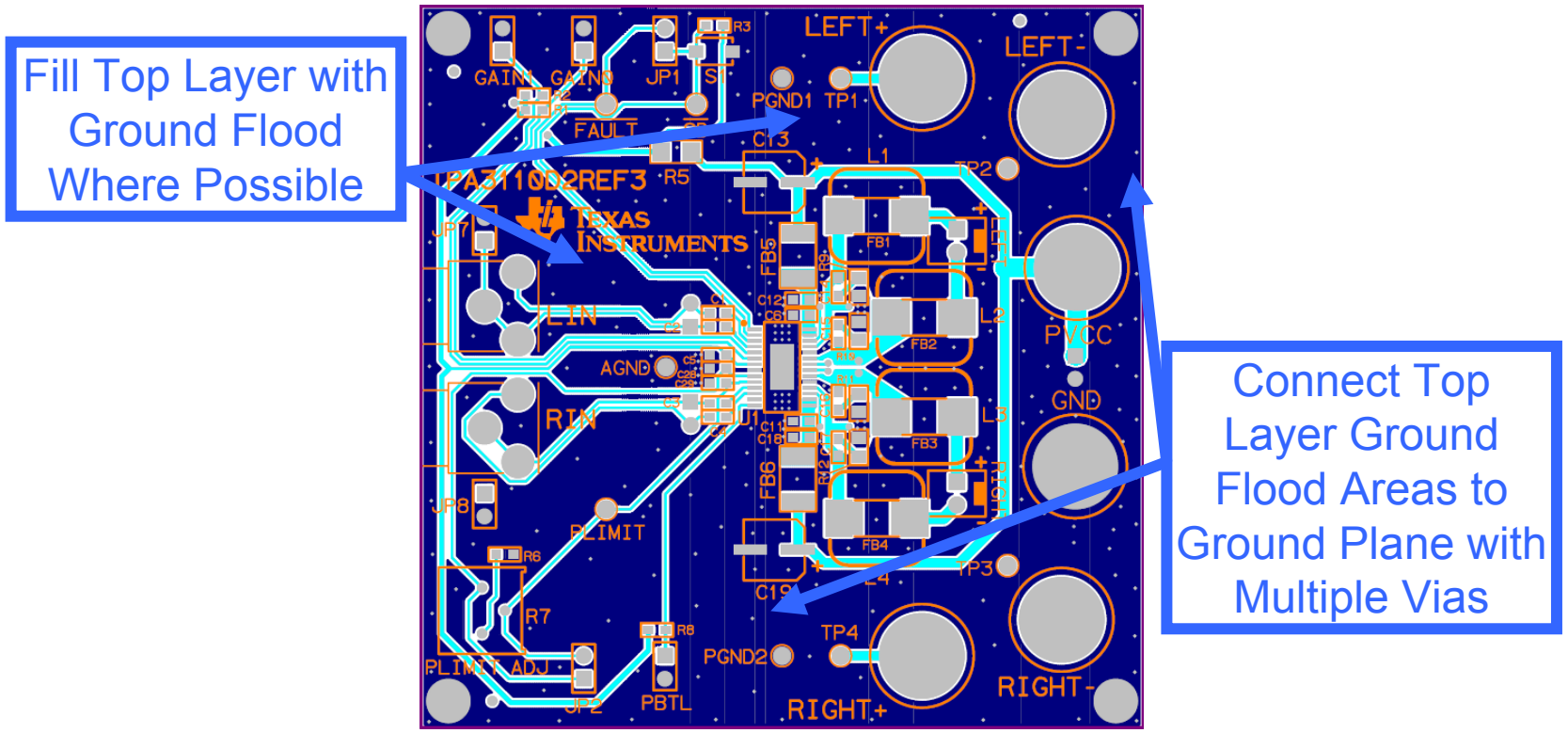
Heat flow to the copper outside the circular cut is reduced, so the copper outside cannot conduct much heat.

So a circular cut increases thermal resistance of the PCB and makes the IC run hotter.

- Avoid circular ground plane cuts – make any necessary cuts radial.

Top Ground Flood Vias

- Flood unused areas of the top layer with copper.



- Connect these areas to the ground plane with vias to allow heat to flow to them.

QUESTIONS?

APPENDIX:
PCB Trace & Via Impedances

PCB Parasitic Resistance

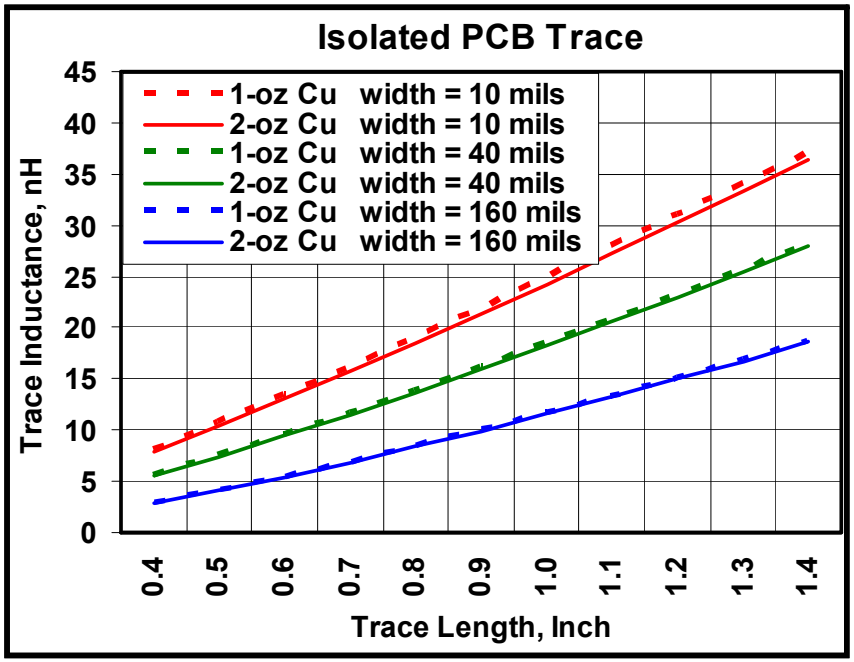
- Copper resistance is relatively easy to calculate.
- In 1-oz copper, resistivity is ~ 0.5mΩ per square.
  - Then resistance is ~0.5mΩ * length / area.
  - So resistance of a 1-oz trace 10 x 100 mils, ~0.25 x 2.5 mm, is only ~5 milliohms.
  - Even long traces will have low resistance if they are made wide enough.
- PCB copper also includes capacitance and inductance.

PCB Capacitance and Inductance

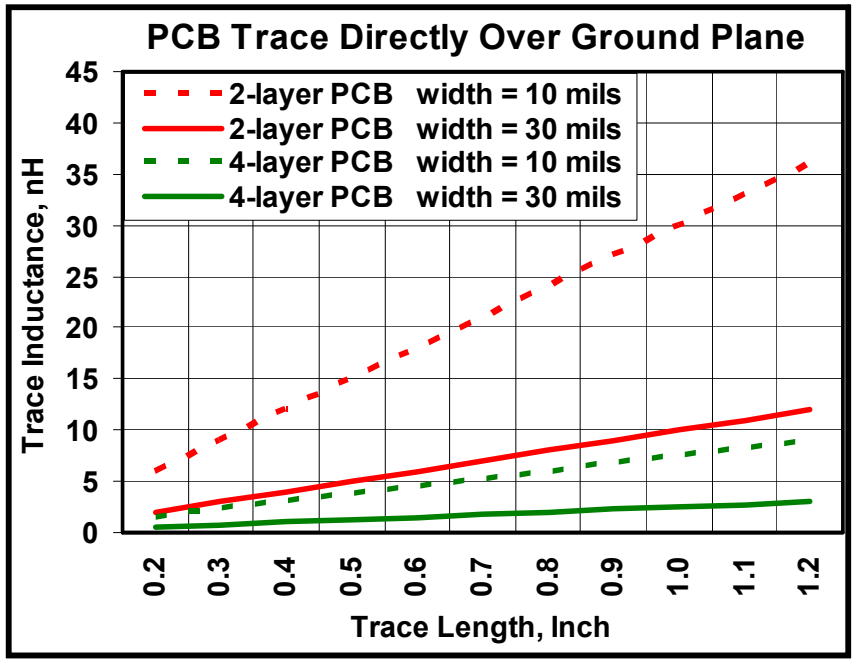
- PCB capacitance and inductance are generally worse parasitics than resistance.
- They can couple RF voltages and currents into nearby traces and degrade decoupling and EMC filter components.
- Inductances are almost always the greatest problem.

PCB Trace Inductance

- Low inductance requires wide traces, so we use ground planes. (Do not use power planes with Class-D – they distribute, not focus, currents.)



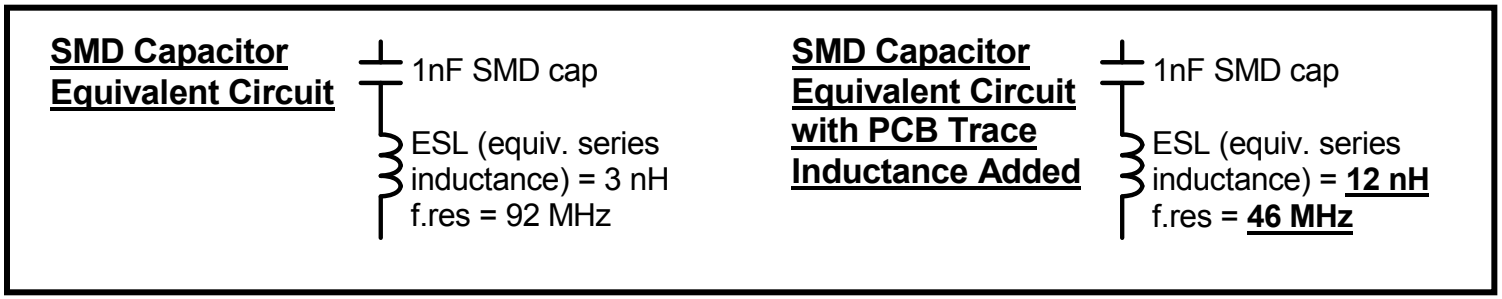
Inductance varies ~linearly with length but only by a factor of ~1/2 for a 16:1 increase in width!



Inductance varies directly with length and separation and inversely with width. (Trace layers are next to ground plane.)

Potential Impact On Components

- Inductance of a 0.3” long 10mil trace over a 2-layer PCB ground plane is greater than that of a typical SMD cap, 2 to 4 nH.
- That can degrade performance of the capacitor significantly!



- Circuit loops also add inductance. There is no easy measure here; smaller is better!

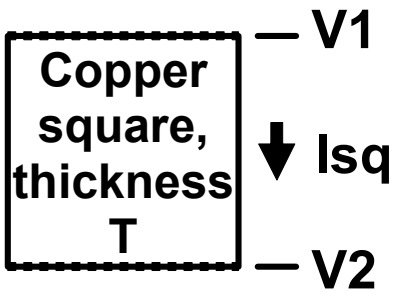
Via Impedance

- Impedance of typical vias is 1 to 5 milliohms plus 1 to 2 nH.
- Via impedance is less certain than impedance of copper traces.

(See pages that follow for equations for resistance and inductance.)

Equations: Copper Ohms per Square

- Resistance of a copper square, (V1-V2)/Isq, can be calculated from the equation



ρ.cu * length / (cross-sectional area), OR (ρ.cu/T) Ω/square, for ANY size square.

- (ρ.cu is copper resistivity, ~17nΩ*m, ~0.67μΩ*in. 1-oz copper is ~1.3mil (~0.033mm) thick, so its resistivity is ~= 0.5mΩ per square.)
- We can compute resistance of a PCB trace by treating it as a series of squares.
  - R.trace = (ρ.cu/T) * trace length / trace width.

Equations: PCB Trace Inductance

- Inductance of an isolated PCB trace can be computed as follows, for inches & cm.

  L ~= 5l (ln(l/(w+t))+1/2) nH (inches).

  L ~= 2l (ln(l/(w+t))+1/2) nH (cm).

  (l, w & t are trace length, width and thickness.)
- Inductance is roughly linear with length.
- However, because of the logarithmic factor, inductance is not very sensitive to trace width and thickness. (Thickness has very little effect.)

Equations: Trace Over Ground Plane

- Inductance of a PCB trace over a ground plane can be computed as follows, for inches & cm.

  L ~= 5lh/w nH/in (inches).

  L ~= 2lh/w nH/cm (cm).

  (l, w & h are trace length, width and separation from the ground plane.)
- L varies directly with length and separation from ground and inversely with width.
- It's possible to achieve much lower inductance in this configuration.

Inductance Equation Limitations

- The equations in the preceding 2 pages require the use of approximations to achieve results.
- Because of that, they become inaccurate for trace lengths shorter than those in the graphs.
- For shorter lengths the inductance is generally small, and it can be estimated by extrapolation .

Equations: Via Impedance

- Inductance (h & d = height and diameter).

  L ~= 5h [ln(4h/d)+1] nH/in (inches).

  L ~= 2h [ln(4h/d)+1] nH/cm (cm).

- Resistance (ρ.cu = copper resistivity, ~17nΩ*m, ~0.67μΩ*inch, l = via length & A = annular area of copper).

  R ~= ρ.cu*l/A Ω.

- 20-mil via, 1-oz plating, in 0.06” PCB:

  L ~= 5*0.06*(ln(4*0.06/0.019)+1) = 1.1nH.

  R ~= ρ.cu*0.06/(pi*(0.01^2-0.0087^2)) = 0.5mΩ.