Following are the steps to configure TPS65950 in JTAG mode:

- Force the Test Pin to '1' (PAD_IO_TEST1P8V).
- Table below will give the details about the 4 JTAG pins (Data in, Data out, TCK (Clock), TMS (Test Mode Select)

JTAG Signals	Dir	Triton2 PADS	Comment
JTAG			
JTAG.TDI	I	PAD_I_JTAG_TDI_BERDATA_1P8V	JTAG Data Input
JTAG.TDO	O	PAD_IO_GPIO0_CD1_JTAG_TDO_1P8V	JTAG Data Output
JTAG.TCK	I	PAD_I_JTAG_TCK_BERCLK_1P8V	JTAG Clock
JTAG.TMS	I	PAD_IO_GPIO1_CD2_JTAG_TMS_1P8V	JTAG Test Mode Select
Two Pads To Enter in TEST Modes			
TEST_RESET	I	PAD_I_TEST_RESET_1P8V	Reset the JTAG and all the Chip.Use as reset during ATPG
TEST	I	PAD_IO_TEST1P8V	0 : JTAG ports are not available 1 : JTAG ports available

- By Default JTAG is in TLR Mode (Test Logic Reset)
- Configure the JTAG in RTI Mode (Run Test Idle) (By Making TMS '0') TDI can have '0' at same time.
- Select the appropriate test mode (PRELOAD/SAMPLE, EXTEST, INTEST) by configuring the instruction register. First select IR scan path of JTAG controller state machine and shift in appropriate number of bits for instruction to be executed. (e.g PRELOAD can be 6 bit opcode which need to be shifted on TDI during SHIFT_IR state of tap controller).
- JTAG controller comes back in RTI state after completing IR scan and then you need to select DR scan path for shifting in actual boundary scan data.
- Select DR scan by toggling TMS as per JTAG controller state machine.Once JTAG state machine enters into SHIFT DR state you have to shift in actual number of data bits to be programmed into boundary scan register of TPS65950.For this you need to know exact length of boundary scan chain register inside TPS65950.

Then toggle the TMS to get jtag controller back into RTI state to be ready for any next operation.